【CLAIMS】

【Claim 1】

A smart IC substrate comprising:

a substrate including a first surface and a second surface opposite the first surface;

a bonding layer disposed on the first surface;

a buffer layer disposed on the bonding layer;

a metal layer disposed on the buffer layer; and

a plating layer disposed on a lower surface of the metal layer,

wherein the metal layer includes an alloy including nickel (Ni), iron (Fe), and chromium (Cr),

wherein the buffer layer includes a first buffer layer a second buffer layer,

wherein the first buffer layer is disposed between the second buffer layer and the metal layer,

wherein the second buffer layer comprises a second-first buffer layer disposed under the first buffer layer and a second-second buffer layer disposed under the second-first buffer layer,

wherein the second-first buffer layer is disposed between the first buffer layer and the second-second buffer layer, and

wherein a surface roughness of the second-second buffer layer is greater than a surface roughness of the second-first buffer layer.

【Claim 2】

The smart IC substrate of claim 1, wherein the first buffer layer and the second-first buffer layer includes metal, and

wherein the second-second buffer layer includes a metal oxide.

【Claim 3】

The smart IC substrate of claim 1, wherein the plating layer includes a first plating layer disposed under the metal layer and a second plating layer disposed under the first plating layer, and

wherein the first buffer layer and the first plating layer includes a same metal.

【Claim 4】

The smart IC substrate of claim 3, wherein the first plating layer has a thickness greater than a thickness of the first buffer layer.

【Claim 5】

The smart IC substrate of claim 1, wherein a plurality of holes are formed penetrating the substrate and the bonding layer,

wherein the metal layer includes a first region that does not overlap the plurality of holes and a second region that overlaps the plurality of holes,

wherein the buffer layer is disposed on the first region,

wherein the buffer layer is not disposed on the second region, and

wherein the plating layer is in contact with the metal layer.

【Claim 6】

The smart IC substrate of claim 1, wherein a plurality of holes are formed penetrating the substrate and the bonding layer,

wherein the metal layer includes a first region that does not overlap the plurality of holes and a second region that overlaps the plurality of holes,

wherein the first buffer layer and the second buffer layer are disposed on the first region,

wherein the first buffer layer and the second-first buffer layer are disposed on the

second region, and

wherein the plating layer is in contact with the second-first buffer layer.

【Claim 7】

The smart IC substrate of claim 6, wherein a thickness of the second-first buffer layer in the second region is greater than a thickness of the second-first buffer layer in the first region.

【Claim 8】

The smart IC substrate of claim 1, wherein the plating layer includes a second plating layer disposed under the metal layer,

wherein the second plating layer includes at least one of gold, silver, and palladium, and

wherein a thickness of the first buffer layer is greater than thicknesses of the second buffer layer and the second plating layer.

【Claim 9】

The smart IC substrate of claim 8, wherein a plurality of holes are formed penetrating the substrate and the bonding layer,

wherein the metal layer includes a first region that does not overlap the plurality of holes and a second region that overlaps the plurality of holes,

wherein the first buffer layer and the second buffer layer are disposed on the first region,

wherein the first buffer layer is disposed on the second region, and

wherein the second plating layer is in contact with the first buffer layer.

【Claim 10】

The smart IC substrate of claim 1, wherein a plurality of holes are formed

penetrating the substrate and the bonding layer,

wherein the metal layer includes a first region that does not overlap the plurality of holes and a second region that overlaps the plurality of holes,

wherein the first buffer layer and the second buffer layer are disposed on the first region,

wherein the first buffer layer is disposed on the second region, and

wherein the plating layer includes a first plating layer in contact with the first buffer layer and a second plating layer disposed under the first plating layer.

【Claim 11】

The smart IC substrate of claim 1, wherein a plurality of holes are formed penetrating the substrate and the bonding layer,

wherein the metal layer includes a first region that does not overlap the plurality of holes and a second region that overlaps the plurality of holes,

wherein the first buffer layer and the second buffer layer are disposed on the first region,

wherein the first buffer layer and the second buffer layer are not disposed on the second region,

wherein the metal layer includes a recess portion formed in a region corresponding to the second region, and

wherein the plating layer is disposed in at least one of the recess portion and the hole.

【Claim 12】

The smart IC substrate of claim 11, wherein a portion of a side surface of the plating layer is in contact with the metal layer.

【Claim 13】

The smart IC substrate of claim 11, wherein the plating layer is disposed only inside the recess portion, and

wherein an outer surface of the plating layer is in contact with the metal layer.

【Claim 14】

The smart IC substrate of claim 1, wherein the alloy includes an iron-based alloy or a nickel-based alloy.

【Claim 15】

A smart IC module comprising:

a smart IC substrate according to claim 1;

a chip disposed on the smart IC substrate; and

a wire connecting the smart IC substrate and the chip.

【Claim 16】

An IC card comprising:

a main body including a receiving portion;

a protective layer disposed on the main body; and

a smart IC module according to claim 15 disposed within the receiving portion.