

REGENERATIVE TIE-HIGH TIE-LOW CELL

BACKGROUND OF THE INVENTION

5 1. FIELD OF THE INVENTION

This invention relates to integrated circuits and particularly to the family of logic circuits.

10 2. DESCRIPTION OF THE RELATED ART

Tying off unused logic inputs to the supply rails (V_{CC} and GND) can be risky due to the damaging consequences of electrostatic discharge (ESD), particularly where the inputs are tied to transistor gates. Figures 1a and 1b show the schematic and block diagram, respectively, for a conventional tie-off circuit. This type circuit has been used to provide logic high (HI) and logic low (LO) voltages that reduce the ESD risk when tying off unused inputs. As shown in the block diagram 7 of Figure 1b, the circuit consists logically of a two-input NAND gate 9 and an inverter 8 with the NAND gate's 9 output tied to one of it's inputs (I1) and to the inverter's 8 input. The output of the inverter 8 is tied to the second input (I2) of the NAND gate 9. The HI tie-off voltage is taken from the output of the NAND gate 9 and the LO tie-off voltage is taken from the output of the inverter 8. Since the inverter 8

assures that one of the NAND gate's inputs is complementary to its other input, under normal conditions one input to the NAND gate 9 will always be a logic LO level, forcing the NAND gate's output to a logic HI level and as a result the output of the inverter will always be at a logic LO level.

In the schematic for the conventional tie-off circuit of Figure 1a, the inverter 8 consists of a p-channel transistor 5 and an n-channel transistor 6 pair. The gates of these two transistors 5,6 are tied together to form the inverter's input and the drains of the transistors 5,6 are also tied together to form the inverter's output at node 2 (N2). To complete the inverter circuit, the source of the p-channel transistor 5 is tied to V_{CC} and the source of the n-channel transistor 6 is tied to GND. The NAND gate 9 consists of two p-channel input transistors 1,2 and two n-channel transistors 3,4. The gates of one of the p-channel transistors 1 and one of the n-channel transistors 3 are tied together to form input I2 of the NAND gate 9, which is connected to the output of the inverter 8 at node 2 and to the LO output terminal of the circuit. The drains of these two transistors 1,3 are tied together to form the HI output terminal at node 1 (N1) and also connects to the I1 input of the NAND gate 9 and to the input of

the inverter 8. The sources of the two p-channel transistors 1,2 are tied to V_{CC} . In the NAND gate circuit, the two n-channel transistors 3,4 are connected in series with the source of one of these transistors 3 connected to the drain of the other transistor 4. Finally, the source of transistor 4 is connected to GND. In this circuit configuration, one of the two n-channel transistors 3,4 is always OFF so that no current flows through this portion of the circuit.

10 The above degenerative (negative feedback) circuit consists of n-channel, p-channel transistor pairs that can under certain conditions, converge with HI and/or LO outputs in an alternative state where the HI and LO output levels are at voltages intermediate between V_{DD} and GND. In other words, the HI and LO levels are not uniquely defined and for certain conditions a metastable state can exist with poorly defined HI and/or LO levels. Such things as process spread, supply resistance, and GND resistance can cause these uncertain conditions. Figure 2 illustrates the possible metastable states that can exist where the HI output is less than the logic 1 level and/or the LO output is greater than the logic 0 level; e.g., given as:

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HI = αV_{CC} , where $0 < \alpha < 1$, and

LO = βV_{CC} , where $0 < \beta < 1$.

The metastable level characteristics for the NAND gate and inverter, respectively, are as follows:

5 $\alpha = f(\alpha, \beta)$ and

$\beta = f(\alpha)$.

As a result, it is possible that α can be significantly low and/or that β can be significantly high so that incorrectly defined logical levels result. This means
10 that it is possible to have tie-off levels where the HI and LO levels are significantly below the V_{CC} and/or above the GND level to the extent that it effects the logical output of the overall circuit function.

15 There is a recognized need for a tie-off circuit which provides for ESD protection and at the same time has uniquely defined HI and LO output levels that correspond to the V_{CC} and GND levels, respectively. The invention described herein addressed this need.

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SUMMARY OF THE INVENTION

In accordance with an aspect of the present invention, there is provided a tie-off circuit, which exhibits stable tie-high, tie-low logic outputs, comprising,

a first transistor,

a second transistor, and

a third transistor that provides positive feedback to assure that the second and third transistors are at desired states.

In example embodiments, a regenerative tie-high, tie-low cell (circuit) for tying off logic inputs that provides unconditionally stable logic 1 and 0 output states, is disclosed. The circuit provides uniquely defined HI and LO states to overcome the poorly defined metastable states that can exist in conventional circuits of this type, where the circuit can converge with HI and/or LO outputs in an alternative state with intermediate HI and LO output voltage levels between V_{DD} and GND. The circuit eliminates p-channel/n-channel transistor pair current paths and adds a regenerative transistor to force the circuit to its desired operating state.

Finally, in a first preferred embodiment, the circuit consists of only three CMOS transistors, reducing the required silicon area and in turn improving the reliability and lowering the cost of fabricated ICs.

DESCRIPTION OF THE VIEWS OF THE DRAWINGS

The included drawings are as follows:

Figure 1a is a schematic for a conventional tie-off

5 circuit requiring six CMOS transistors. (prior art)

Figure 1b is a logic block diagram for the conventional tie-off circuit of Figure 1. (prior art)

Figure 2 is a diagram illustrating the metastable levels that can exist in the conventional logic tie-off

10 circuit of Figure 1. (prior art)

Figure 3 is a diagram illustrating the desired logic levels for a logic tie-off circuit.

Figure 4 is a schematic for one embodiment of the tie-off circuit of this invention.

15 Figure 5 is a schematic for a second embodiment of the tie-off circuit of this invention.

DETAILED DESCRIPTION

The desired characteristics of a logic tie-off cell (circuit) is one that is stable with the HI (1) level
5 always at the V_{CC} voltage and the LO (0) level always at GND, as illustrated in the logic block diagram of Figure 3. This invention accomplishes the desired goal.

The schematic for a first embodiment of the tie-off
10 cell (circuit) of this invention is shown in Figure 4. The regenerative nature of this circuit overcomes the possibility of a metastable state that can exist in conventional circuits, as discussed in the prior art, and assures that the circuit quickly achieves the desired
15 output (1 and 0) logic state. This circuit has no p-channel/n-channel transistor pair current paths and as a result, eliminates all non- V_{CC} and/or non-GND nodes that can cause the poorly define metastable states. The circuit consists of three CMOS transistors: two p-channel
20 transistors 40 and 42, and an n-channel transistor 41. The circuit is wired such that the drain of one of the p-channel transistors 40 is tied to the gate of the n-channel transistor 41 and in a reciprocal fashion, the drain of the n-channel transistor 41 is tied to the gate
25 of this p-channel transistor 40. The HI output signal is taken off the drain of the p-channel transistor 40 while

the LO output signal is taken off the drain of the n-channel transistor 41. The second p-channel transistor 42 is added to provide a startup state and assures that the gate of the n-channel transistor 41 is never LO or floating. Transistors 40 and 41 provide regeneration (positive feedback) to maintain the correct HI and LO states. Both the gate and drain of this second p-channel transistor 42 are tied to the drain of the other p-channel transistor 40 (HI output) and to the gate of the n-channel transistor 41. The sources of both p-channel transistors 40 and 42 are tied to the V_{CC} supply and the source of the n-channel transistor 41 is tied to GND.

In operation, the p-channel transistor's 40 drain performs a pull-up on the n-channel transistor's 41 gate, turning the transistor 41 ON and forcing its output LO. Likewise, the n-channel transistor's 41 drain performs a pull-down on the p-channel transistor's 40 gate, turning the transistor 40 ON and forcing its output HI. As long as either of these conditions is performed the desired HI/LO output logic levels will be achieved since both the p-channel transistor 40 and the n-channel transistor 41 are ON. Under normal operating conditions, the P-channel transistor 42 is OFF. However, if for any reason the gate of the n-channel transistor 41 (also the gate of p-channel transistor 42) is ever momentarily LO or

floating, this will turn ON the p-channel transistor 42, which in turn will pull the gate of the n-channel transistor 41 high, turning transistor 41 ON, and this in turn will pull down the gate of the p-channel transistor 40, turning transistor 40 ON, to achieve the desired HI/LO output states.

A second complementary embodiment of the tie-off cell (circuit) of this invention is shown in the schematic of Figure 5. Like the circuit of Figure 4, this circuit has no p-channel/n-channel transistor pairs and as a result, eliminates all non- V_{CC} and/or non-GND nodes that can cause the poorly define metastable states. This circuit also consists of three CMOS transistors: two n-channel transistor 50 and 52, and a p-channel transistor 51. The circuit is wired such that the drain of one of the n-channel transistors 50 is tied to the gate of the p-channel transistor 51 and in a reciprocal fashion, the drain of the p-channel transistor 51 is tied to the gate of this n-channel transistor 50. The HI output signal is taken off the drain of the p-channel transistor 51 while the LO output signal is taken off the drain of the n-channel transistor 50. The second n-channel transistor 52 is added to provide a startup state and assures that the gate of the p-channel transistor 51 is never HI or floating. Transistors 50 and 51 provide

regeneration (positive feedback) to maintain the correct HI and LO states. Both the gate and drain of the n-channel transistor 52 are tied to the drain of the other n-channel transistor 50 (LO output) and the gate of the p-channel transistor 51. The sources of both p-channel transistors 50 and 52 are tied to GND and the source of the p-channel transistor 51 is tied to the V_{CC} supply. In operation, the n-channel transistor's 50 drain performs a pull-down on the p-channel transistor's 51 gate, turning the transistor 51 ON and forcing its output HI. Likewise, the p-channel transistor's 51 drain performs a pull-up on the n-channel transistor's 50 gate, turning the transistor 50 ON and forcing its output LO. As long as either of these conditions is performed the desired HI/LO output levels will be achieved since both the n-channel transistor 50 and the p-channel transistor 51 are ON. Under normal operating conditions, the n-channel transistor 52 is OFF. However, if for any reason the gate of the p-channel transistor 51 (also the gate of n-channel transistor 52) is ever momentarily HI or floating, this will turn ON the p-channel transistor 52 which in turn will pull the gate of the p-channel transistor 51 low, turning transistor 51 ON, and in turn will pull up the gate of the n-channel transistor 50,

turning transistor 50 ON, to achieve the desired HI/LO output states.

The primary advantages of the cell(s) of this invention are (1) the unconditional stable output logic states,
(2) the elimination of any transistor pair current paths which prevents the possibility of metastable states, (3) the minimal transistor count which results in a reduction of required silicon area, and (4) the regenerative functionality of the circuit.

While this invention has been described in the context of two preferred embodiments, it will be apparent to those skilled in the art that the present invention may be modified in numerous ways and may assume embodiments other than that specifically set out and described above. Accordingly, it is intended by the appended claims to cover all modifications of the invention that fall within the true spirit and scope of the invention.

I Claim:

1. A tie-off circuit, which exhibits stable tie-high,
tie-low logic outputs, comprising:
5 a first transistor;
a second transistor; and
a third transistor that provides positive feedback
to assure that said second and third transistors are
at desired states.
- 10 2. The tie-off circuit of Claim 1, wherein
said first, second, and third transistors each have
a first electrode, a second electrode, and a third
electrode.
- 15 3. The tie-off circuit of Claim 2, wherein
said first electrodes of said first, second, and
third transistors are the drain leads of said
transistors;
20 said second electrodes of said first, second, and
third transistors are the gate leads of said
transistors; and
said third electrodes of said first, second, and
third transistors are the source leads of said
25 transistors.

4. The tie-off circuit of Claim 3, wherein non- V_{CC} or GND voltage nodes are eliminated.
5. The tie-off circuit of Claim 4, wherein the flow of
5 current through p-channel/n-channel transistor pairs is eliminated.
6. The tie-off circuit of Claim 5 that is functionally regenerative.
- 10 7. The tie-off circuit of Claim 6, wherein
said first and third transistors are p-channel CMOS transistors; and
said second transistor is an n-channel CMOS
15 transistor.
8. The tie-off circuit of Claim 7, wherein
said first electrode of said first transistor is
tied to said second electrode of said second
20 transistor, to said first and second electrodes of
said third transistor, and to the HI output
terminal;
said first electrode of said second transistor is
tied to said second electrode of said first
25 transistor and to the LO output terminal;
said third electrodes of said first and third
transistors are tied to V_{CC} supply voltage; and

said third electrode of said second transistor is tied to GND.

9. The tie-off circuit of Claim 6, wherein
 5 said first and third transistors are n-channel transistors; and
 said second transistor is a p-channel transistor.

10. The tie-off circuit of Claim 9, wherein
 10 said first electrode of said first transistor is tied to said second electrode of said second transistor, to said first and second electrodes of said third transistor, and to the LO output terminal;

15 said first electrode of said second transistor is tied to said second electrode of said first transistor and to the HI output terminal;
 said third output terminals of said first and third transistors are tied to GND; and
 20 said third electrode of said second transistor is tied to V_{CC} supply voltage.

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