Claims

1. A planar sheet comprising:

a planar dielectric material layer having a first planar surface and a second planar surface, and

first copper foil sheet having a first planar surface and a second planar surface, wherein the first copper foil planar surface is associated with the first dielectric material layer planar surface, wherein the first copper foil sheet first surface and second surface each include a bond enhancement layer having a Rz roughness of from about 0.25 to about 5.0 microns; and

further comprising a circuit pattern formed in the first planar copper sheet such that unnecessary portions of the first planar copper sheet have been removed leaving the circuit pattern copper in place wherein the bond enhancement layer is not applied to the circuit pattern after it is formed.

2. The planar sheet of claim 1 including a second dielectric material layer laminated to the planar sheet such that the second dielectric material layer is adhered to the second planar surface of the circuit pattern.

3. The planar sheet of claim 1 wherein the bond enhancement layers of the first copper foil sheet first surface and second surface are formed by different bond enhancement methods.

4. The planar sheet of claim 1 wherein the bond enhancement layers of the first copper foil sheet first surface and second surface are formed prior to

associating the first copper foil planar surface with the first dielectric material layer planar surface.

5. The planar sheet of claim 1 wherein the surface roughness of the first copper foil sheet first planar surface is less than about 1.5 microns.

6. The planar sheet of claim 1 wherein the surface roughness of the first copper foil sheet second planar surface is less than about 2.5 microns.

7. The planar sheet of claim 1 wherein the circuit pattern includes a bottom wall corresponding to the first copper sheet first planar surface, a top wall corresponding to the first copper foil sheet second planar surface and side walls, wherein the side walls do not include a bond enhancement layer.

8. The planar sheet of claim 7 wherein the circuit pattern includes a plurality of transmission lines.

9. The planar sheet of claim 1 further including a second copper foil sheet having a first planar surface and a second planar surface wherein the second copper foil first planar surface is associated with the dielectric material layer second planar surface and wherein the second planar copper foil sheet first surface and second surface each include a bond enhancement layer.

10. The planar sheet of claim 9 wherein a circuit pattern is formed in the second copper sheet such that unnecessary portions of the second planar copper sheet have been removed leaving the circuit pattern copper in place

wherein the bond enhancement layer is not applied to the circuit pattern after it is formed.

11. The planar sheet of claim 1 wherein the Rz roughness of the first and second planar copper surfaces of the first copper foil sheet are the same.

12. The planar sheet of claim 9 wherein the Rz roughness of the first and second planar copper surfaces of the second copper foil sheet ranges from about 0.1 to about 6.0 microns, or wherein the Rz roughness ranges from about 0.25 to about 5.0 microns.

13. The planar sheet of claim 1 wherein the copper foil is selected from a 1 ounce copper foil, a ½ ounce copper foil and a ¼ ounce copper foil.

14. The planar sheet of claim 1, the first copper foil sheet having thicknesses of from about 5 microns to about 35 microns and Rz surface roughness of 1.3 micrometers or less.

15. The planar sheet of claim 1 wherein at least one first copper sheet bond enhancement layer includes a coating.

16. The planar sheet of claim 1 which is selected from resin coated copper, a copper clad prepreg or a copper clad c-staged laminate.

17. A method for manufacturing a printed circuit board comprising the steps of:

i. providing a planar sheet including a planar dielectric material layer having a first planar surface and a second planar surface, and first copper foil sheet having a first planar surface and a second planar surface, wherein the first copper foil planar surface is associated with the first dielectric material layer planar surface, and wherein the first copper foil sheet first surface and second surface each include a bond enhancement layer having a Rz roughness of from 0.25 to 5.0 μm; and

ii. forming a circuit pattern in the first planar copper sheet by removing unnecessary portions of the first planar copper sheet while leaving the circuit pattern copper in place to form an innerlayer sheet including a circuit pattern having a plurality of transmission lines wherein a bond enhancement layer is not applied to the circuit pattern after it is formed.

18. The method of claim 17 wherein a dielectric material layer is laminated to the innerlayer sheet such that the dielectric material layer adhered to the second planar surface of the circuit pattern.

19. The method of claim 17 wherein bond enhancement methods are used to apply bond enhancement layers to the planar copper foil sheet first and second surfaces.

20. The method of claim 19 wherein a first bond enhancement method is used to apply the bond enhancement layer to the planar copper foil sheet first

surface and a second bond enhancement method is used to apply the bond enhancement layer to the planar copper foil sheet second surface, and wherein the first bond enhancement method and second bond enhancement method are different bond enhancement methods.

21. The method of claim 17 wherein the surface roughness of the first planar copper foil sheet first planar surface is less than 1.5 μm and the surface roughness of the first copper foil sheet second planar surface is less than 2.5 μm.

22. The method of claim 17 wherein the circuit pattern includes a bottom wall corresponding to the first copper sheet first planar surface, a top wall corresponding to the first copper foil sheet second planar surface and side walls, wherein the side walls do not include a bond enhancement layer.

23. The method of claim 17 wherein the planar sheet includes second copper foil sheet having a first planar surface and a second planar surface, wherein the second copper foil first planar surface is associated with the dielectric material layer second planar surface and wherein the second planar copper foil sheet first surface and second surface each include a bond enhancement layer, the method including

forming a circuit pattern in the second copper sheet by removing unnecessary portions of the second planar copper sheet while leaving the

circuit pattern copper in place to form an innerlayer sheet including a circuit pattern having a plurality of transmission lines wherein a bond enhancement layer is not applied to the circuit pattern after it is formed.

24. The method of claim 17 wherein the roughness of the first and second planar copper surfaces of the first copper foil sheet are the same.

25. The method of claim 17 wherein the copper foil is selected from a 1 ounce copper foil, a ½ ounce copper foil and a ¼ ounce copper foil, and/or wherein the planar sheet is selected from resin coated copper, a copper clad prepreg or a c-staged laminate.

26. The method of claim 17 wherein the first copper foil sheet is a copper foil sheet having thicknesses of from 10 to 400 μm, or a copper foil sheet having thicknesses of from 5 μm to 200 μm, or more a copper foil sheet having thicknesses of from 5 to 35 μm.

27. The method of claim 17 wherein at least one first copper sheet bond enhancement layer includes a coating.

28. The method of claim 17 wherein the circuit pattern includes a plurality of transmission lines having widths of from 25 to 250 μm.

29. The method of claim 17 wherein the bond enhancement layers are imparted on the first and second planar copper surfaces of the first copper foil sheet simultaneously.

30. The method of claim 17 further comprising forming a layup by stacking at least one innerlayer sheet on a prepreg.