

ABSTRACT

A 3D stacked FET may include a back-side wiring layer including a first back-side power line and a second back-side power line, a first FET on the back-side wiring layer, a second FET over the first FET, a front-side wiring layer over the second FET, a first through-electrode connecting the first FET to the second FET, and a second through-electrode connecting the front-side and back-side power lines. The front-side wiring layer may extend in a first direction and may include a front-side power line connected to the second back-side power line. The first FET and the second FET may share a gate extending in a second direction. Each of the first FET and the second FET may include a source and a drain respectively on both sides of the gate in the first direction, and a channel between the source and the drain and surrounded by the gate.

FIG. 3B