# MICROELECTRONIC DEVICES HAVING INTERMEDIATE CONTACTS FOR CONNECTION TO INTERPOSER SUBSTRATES, AND ASSOCIATED METHODS OF PACKAGING MICROELECTRONIC DEVICES WITH INTERMEDIATE CONTACTS

## TECHNICAL FIELD

**[0001]** The following disclosure relates generally to packaging microelectronic devices and, more particularly, to methods for electrically coupling microelectronic dies to interposer substrates.

## BACKGROUND

**[0002]** Conventional die-level packaged microelectronic devices typically include a microelectronic die, an interposer substrate or lead frame attached to the die, and a moulded casing around the die. The die generally includes an integrated circuit coupled to a plurality of bond-pads. The bond-pads are typically coupled to contacts on the interposer substrate or lead frame, and serve as external electrical contacts through which supply voltage, signals, etc., are transmitted to and from the integrated circuit. In addition to contacts, interposer substrates can also include ball-pads coupled to the contacts by conductive traces supported in a dielectric material. Solder balls can be attached to the ball-pads in one-to-one correspondence to define a "ball-grid array." Packaged microelectronic devices with ball-grid arrays are generally higher grade packages that have lower profiles and higher pin counts than conventional packages using lead frames.

**[0003]** One process for making a packaged microelectronic device with a ball-grid array includes (a) forming a plurality of dies on a semiconductor wafer, (b) cutting the wafer to separate or singulate the dies, (c) attaching individual dies to an interposer substrate, (d) wire-bonding bond-pads on the dies to contacts on the interposer substrate, and (e) encapsulating the dies with a suitable moulding compound. Packaged microelectronic devices made in the foregoing manner are often used in cellphones,

pagers, personal digital assistants, computers, and other electronic products. As the demand for these products grows, there is a continuing drive to increase the performance of packaged microelectronic devices while at the same time reducing the height and surface area or "footprint" of such devices on printed circuit boards. Reducing the size of microelectronic devices, however, becomes more difficult as the performance increases because higher performance typically requires more integrated circuitry and bond-pads.

**[0004]** Figure 1 is a partially cut-way isometric view of a packaged microelectronic device 100 configured in accordance with the prior art. The packaged microelectronic device 100 includes a microelectronic die 110 attached to an interconnecting substrate 120 in a conventional board-on-chip (BOC) arrangement. The microelectronic die 110 includes an integrated circuit 116 electrically coupled to a plurality of terminals (e.g., bond-pads) 112. Each of the terminals 112 is electrically coupled to a corresponding bond-finger or contact 122 on the interconnecting substrate 120 by an individual wire-bond 114. Each of the contacts 122 is in turn electrically connected to a corresponding ball-pad 126 by a conductive line or trace 124 formed on the surface of the substrate 120. After the electrical connections have been made, the microelectronic die 110 can be encapsulated with a suitable mold compound 140 for protection. Solder balls (not shown) can be attached to the ball-pads 126 in one-to-one correspondence to form a ball-grid array for attaching the packaged microelectronic device 100 to a printed circuit board (PCB), printed wiring assembly (PWA), and/or other electronic interfaces (not shown).

**[0005]** As the performance of the microelectronic die 110 increases, the number of terminals 112 also increases. Combining this with the trend to make the die 110 smaller results in a very fine-pitch array of terminals 112 on the die 110. Providing enough contacts 122 and traces 124 to accommodate the terminals 112 causes the surface of the interconnecting substrate 112 to become very congested near the die 110. At some point, the surface of the substrate 120 will become so congested that it will no longer be possible to add any additional contacts or traces. This constraint limits the ability to shrink the microelectronic device 100 further, especially if the performance of the die 110 increases.

**[0006]** Figure 2 is a partially cut-away isometric view of another packaged microelectronic device 200 configured in accordance with the prior art. The packaged

microelectronic device 200 includes a microelectronic die 210 bonded to an interconnecting substrate 220 in a conventional chip-on-board (COB) arrangement. The microelectronic die 210 includes an integrated circuit 216 electrically coupled to a plurality of first terminals 212a and a plurality of second terminals 212b. As shown, the first terminals 212a are arranged along one side of the die 210 and the second terminals 212b are arranged along the other side of the die 210. Each of the terminals 212 is electrically connected to a corresponding contact 222 on the interconnecting substrate 220 by an individual wire-bond 214. Each of the contacts 222 is in turn electrically coupled to a corresponding ball-pad 226 by a conductive line 224. In the conventional COB arrangement illustrated in Figure 2, the ball-pads 226 are located on a back surface of the interconnecting substrate 220, and a portion of each conductive line 224 extends through the substrate 220 to reach the corresponding ball-pad 226. After all the electrical connections have been made, the microelectronic 210 is encased in a suitable mold compound 240.

**[0007]** Many of the congestion problems discussed above with reference to Figure 1 also apply to the packaged microelectronic device 200 illustrated in Figure 2. For example, as the performance of the microelectronic die 210 increases, the number of terminals 212 and other die components also increases. As a result, the common way to reduce the overall size of the packaged device 200 is to reduce the size of the interconnecting substrate 220. As the interconnecting substrate 220 becomes smaller, however, the contacts 222 need to be smaller and more compressed because the area to accommodate them is reduced. This makes attachment of the wire-bonds 214 to the contacts 222 increasingly difficult which, in turn, tends to limit the ability to shrink the overall package further.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0008]** Figure 1 is a partially cut-away isometric view of a packaged microelectronic device configured in accordance with the prior art.

**[0009]** Figure 2 is a partially cut-away isometric view of another packaged microelectronic device configured in accordance with the prior art.

**[0010]** Figure 3 is an isometric view of a microelectronic device configured in accordance with an embodiment of the present invention.

**[0011]** Figure 4 is an isometric view of an interconnecting substrate configured in accordance with an embodiment of the invention.

**[0012]** Figure 5 is a cross-sectional view of a packaged microelectronic device configured in accordance with an embodiment of the invention.

**[0013]** Figure 6 is an isometric view of a microelectronic device configured in accordance with another embodiment of the invention.

**[0014]** Figure 7 is an isometric view of an interconnecting substrate configured in accordance with another embodiment of the invention.

**[0015]** Figure 8 is a cross-sectional view of a packaged microelectronic device configured in accordance with another embodiment of the invention.

## DETAILED DESCRIPTION

### A. Overview

**[0016]** The following disclosure describes several embodiments of microelectronic devices and/or interconnecting substrates having intermediate contacts. The following disclosure also describes several embodiments of methods for packaging microelectronic devices having intermediate contacts. One aspect of the invention is directed toward a microelectronic device having a first surface, a second surface positioned opposite to the first surface, and an integrated circuit positioned at least partially between the first and second surfaces. The microelectronic device further includes a plurality of terminals, a plurality of first contacts, and a plurality of second contacts. The terminals are positioned on the first surface of the microelectronic device and are electrically coupled to the integrated circuit. The first contacts are positioned on the first surface to one side of the terminals, and the second contacts are positioned on the first surface to the other side of the terminals. Each of the terminals is electrically coupled to a corresponding contact by, for example, a corresponding wire-bond. In one embodiment, the microelectronic device

can further include an insulating layer that is attached to the first surface and carries the first and second contacts.

**[0017]** Another aspect of the invention is directed to a packaged microelectronic device that includes a plurality of first contacts supported by a microelectronic die and a plurality of second contacts supported by an interconnecting substrate. The microelectronic die includes a plurality of terminals electrically coupled to an integrated circuit. A plurality of wire-bonds individually couples each of the terminals to a corresponding one of the first contacts on the die. In one embodiment, each of the first contacts on the die faces a corresponding second contact on the interconnecting substrate. In this embodiment, a conductive coupler can extend between each pair of adjacent contacts to electrically connect the die to the interconnecting substrate.

**[0018]** A further aspect of the invention is directed to a method of manufacturing a packaged microelectronic device. The method includes providing a microelectronic die having a plurality of terminals electrically coupled to an integrated circuit. The method further includes forming a plurality of first contacts adjacent to the terminals, and electrically coupling each of the first contacts to a corresponding one of the terminals. In one embodiment, forming a plurality of first contacts adjacent to the terminals can include forming the first contacts on an insulating layer that is laminated to the die. In another embodiment, electrically coupling each of the first contacts to one of the terminals can include attaching a wire-bond from each of the first contacts to a corresponding one of the terminals. The method additionally includes forming a plurality of second contacts on an interconnecting substrate, and positioning the interconnecting substrate so that the second contacts on the substrate face the first contacts on the microelectronic die. The method then includes electrically coupling each of the first contacts on the die to a corresponding one of the second contacts on the interconnecting substrate. In one embodiment, electrically coupling the first contacts to the second contacts can include forming a solder ball or bump between opposing contacts.

**[0019]** Specific details of several embodiments of the invention are described below with reference to Figures 3-8 to provide a thorough understanding of such embodiments. Other details describing well-known structures often associated with microelectronic

devices and interconnecting substrates are not set forth in the following description, however, to avoid unnecessarily obscuring the description of the various embodiments. Those of ordinary skill in the art will understand that the invention may have other embodiments in addition to those described below. Some of these embodiments may lack one or more of the elements or features shown or described below with reference to Figures 3-8. Alternatively, other of these embodiments may include additional elements or features that are not shown or described below.

**[0020]** The term "microfeature workpiece" is used throughout to include substrates upon which and/or in which microelectronic devices, micromechanical devices, data storage elements, optics, and other features are fabricated. For example, microfeature workpieces can be semiconductor wafers, glass substrates, dielectric substrates, or many other types of substrates. Many features on such microfeature workpieces have critical dimensions less than or equal to 1 µm, and in many applications the critical dimensions of the smaller features are less than 0.25 µm or even less than 0.1 µm.

**[0021]** Where the context permits, singular or plural terms may also include the plural or singular term, respectively. Moreover, unless the word "or" is expressly limited to mean only a single item exclusive from other items in reference to a list of at least two items, then the use of "or" in such a list is to be interpreted as including (a) any single item in the list, (b) all of the items in the list, or (c) any combination of the items in the list. Additionally, the term "comprising" is used throughout to mean including at least the recited feature(s) such that any greater number of the same features and/or types of other features and components are not precluded.

B. Embodiments of Intermediate Contacts for Microelectronic Devices with Centrally Arranged Terminals

**[0022]** Figure 3 is an isometric view of a microelectronic device 302 having a plurality of intermediate contacts 313a-l configured in accordance with an embodiment of the invention. In this embodiment, the microelectronic device 302 includes a microelectronic die 310 having a plurality of centrally-arranged terminals (e.g., bond-pads) 312a-l electrically coupled to an integrated circuit 316. The microelectronic die 310 can be a memory device, processing device, routing device, imager or other type of microelectronic

device known in the art. The intermediate contacts 313 are divided into a plurality of first contacts 313a-f positioned on one side of the terminals 312, and plurality of second contacts 313g-l positioned to the other side of the terminals 312. Each of the contacts 313 is electrically coupled to a corresponding terminal 312 by an individual wire-bond 314.

**[0023]** In the illustrated embodiment, the first contacts 313a-f are carried on a first insulating layer portion 352a which is laminated to the die 310 on one side of the terminals 312, and the second contacts 313g-l are carried on a second insulating layer portion 352b which is laminated to the die 310 on the other side of the terminals 312. In this embodiment, the insulating layer portions 352 can represent an intermediate substrate that is attached to the surface of the die 310. The insulating layer portions 352 can be manufactured from BT resin, FR4, Polyimide Flex, and/or other suitable dialectric materials known in the art. The insulating layer portions 352 can electrically insulate the contacts 313 from the die 310, and can provide a suitable surface for forming the contacts 313 using conventional plating, patterning, and etching methods known in the art. In other embodiments, however, it is expected that the insulating portions 352 can be omitted and the contacts 313 can be formed directly on the surface on the microelectronic die 310 using suitable methods known in the art. Such methods may include, for example, methods that are at least generally similar to those for forming redistribution layers at the wafer manufacturing level.

**[0024]** Figure 4 is an isometric view of an interconnecting substrate 420 having a plurality of intermediate contacts 422a-l configured in accordance with an embodiment of the invention. The interconnecting substrate 420 can be manufactured from a portion of non-conductive material 460 (e.g., FR4, BT resin, Polyimide Flex, or other suitable material known in the art) having a first surface 461 opposite to a second surface 462. The contacts 422 can be formed on the first surface 461 using suitable plating, patterning, and etching techniques (and/or other techniques) known in the art.

**[0025]** In one aspect of this embodiment, the intermediate contacts 422 are divided into a plurality of third contacts 422a-f and a plurality of fourth contacts 422g-l. Each of the contacts 422 is electrically coupled to a corresponding ball-pad 426 by a conductive line 424. The ball-pads 426 are positioned on the second surface 462, and the conductive

lines 424 can accordingly include portions of through-vias, bond-fingers, conductive traces, and/or other elements suitable for making electrical connections on, over, or through non-conductive material. In another aspect of this embodiment, the plurality of third contacts 422a-f is arranged on one side of the first surface 461 in mirror-image of the first contacts 313a-f of Figure 3, and the plurality of fourth contacts 422g-l is arranged on the other side of the first surface 461 in mirror-image of the second contacts 313g-l of Figure 3. As described in greater detail below, this particular arrangement facilitates electrical coupling of the plurality of first contacts 313a-f to the plurality of third contacts 422a-f in one-to-one correspondence, and electrical coupling of the plurality of second contacts 313g-l to the plurality of fourth contacts 422g-l in one-to-one correspondence.

C. Embodiments of Packaged Microelectronic Devices With Centrally Arranged Terminals

**[0026]** Figure 5 is a side cross-sectional view of a packaged microelectronic device 500 configured in accordance with an embodiment of the invention. In this view, the interconnecting substrate 420 is inverted relative to its orientation in Figure 4 so that individual contacts 422 on the interconnecting substrate 420 are at least approximately aligned with corresponding contacts 313 on the microelectronic device 302. Conductive couplers 580 (e.g., solder balls or bumps) can then be reflowed to attach each of the contacts 313 to the adjacent contact 422. The conductive couplers 580 can include gold-to-gold solder and/or other flowable materials known in the art for electrically coupling contacts together in the illustrated manner. Once each of the contacts 313 has been electrically coupled to a corresponding contact 422, the space between the microelectronic device 302 and the interconnecting substrate 420 can be under-filled with a suitable mold compound 570 (e.g., epoxy or other flowable dielectric material known in the art) that bonds the microelectronic device 302 to the interconnecting substrate 420.

**[0027]** As shown in Figure 5, a plurality of solder balls 582 can be suitably attached to the ball-pads 426 on the second surface 462 of the interconnecting substrate 420 to form a ball grid array suitable for attaching the packaged microelectronic device 500 to an associated PCB, PWA, and/or other type of electrical device or assembly.

**[0028]** One feature of the packaged microelectronic device embodiment described above with reference to Figure 5 is that the contacts 313 are distributed over a relatively large area on the die 310. One advantage of this feature is that it reduces congestion on the second surface 462 of the interconnecting substrate 420 by enabling the contacts 422 to be placed on the first surface 461. Reducing congestion on the second surface 462 can make it easier to reduce the overall size of the device package 500. A further advantage of this feature is that it eliminates the need for wire-bonds between the die terminals 312 and contacts on the interconnecting substrate 420.

D. Embodiments of Intermediate Contacts for Microelectronic Devices With Peripherally Arranged Terminals

**[0029]** Figure 6 is an isometric view of a microelectronic device 602 configured in accordance with another embodiment of the invention. Many features of the microelectronic device 602 are at least generally similar in structure and function to corresponding features of the microelectronic device 302 discussed above with reference to Figure 3. For example, the microelectronic device 602 includes a microelectronic die 610 having an integrated circuit 616 electrically coupled to a plurality of terminals (e.g., bond-pads) 612a-x. In the illustrated embodiment, however, the terminals 612a-x are divided into a plurality of first terminals 612a-l positioned on one side of the microelectronic die 610, and a plurality of second terminals 612m-x positioned on the other side of the microelectronic die 610. Such an arrangement of terminals is typical of that found on microelectronic dies attached to interconnecting substrates in COB arrangements.

**[0030]** The microelectronic device 602 further includes a plurality of first contacts 613a-l, and a plurality of second contacts 613m-x, positioned between the plurality of first terminals 612a-l and the plurality of second terminals 612m-x. In the illustrated embodiment, the plurality of first contacts 613a-m is carried by a first insulating layer portion 652a, and the plurality of second contacts 613m-x is carried by a second insulating layer portion 652b. The insulating layer portions 652 can be laminated or otherwise attached to the surface of the die 610, and can include FR4, BT resin, Polyimide Flex, and/or other suitable dialectric materials known in the art. Each of the first terminals 612a-l is electrically coupled to a corresponding one of the first contacts 613a-l by an individual

wire-bond 614a-l. Similarly, each of the second terminals 612m-x is electrically coupled to a corresponding one of the second contacts 613m-x by an individual wire-bond 614m-x.

**[0031]** Figure 7 is an isometric view of an interconnecting substrate 720 configured in accordance with another embodiment of the invention. Many features of the interconnecting substrate 720 are at least generally similar in structure and function to the interconnecting substrate 420 described above with reference to Figure 4. For example, the interconnecting substrate 720 includes a non-conductive material 760 having a first surface 761 opposite to a second surface 762. Further, the interconnecting substrate 720 includes a plurality of third contacts 722a-l, and a plurality of fourth contacts 722m-x, formed on the first surface 761 of the non-conductive material 760. In the illustrated embodiment, the third contacts 722a-l are arranged in a pattern that at least approximately mirrors the pattern of first contacts 613a-l on the die 610 of Figure 6. Similarly, the fourth contacts 722m-x are arranged in a pattern that at least approximately mirrors the pattern of second contacts 613m-x on the die 610. Each of the third and fourth contacts 722 is electrically coupled to a corresponding ball-pad 726 by an individual conductive line 724 that extends at least partially through the non-conductive material 760.

C. Embodiments of Packaged Microelectronic Devices With Peripherally Arranged Terminals

**[0032]** Figure 8 is a side cross-sectional view of a packaged microelectronic device 800 configured in accordance with another embodiment of the invention. In this embodiment, the interconnecting substrate 720 is inverted so that each of the third contacts 722a-l on the substrate 720 faces a corresponding first contact 613a-l on the die 610, and each of the fourth contacts 722m-x on the substrate 720 faces a corresponding second contact 613m-x on the die 610. When the interconnecting substrate 720 and the microelectronic device 602 are in these positions, conductive couplers (e.g., solder bumps) 880 positioned between adjacent contacts can be reflowed to electrically connect the contacts together. After the conductive couplers 880 have been reflowed, the space between the interconnecting substrate 720 and the microelectronic device 602 can be suitably filled with a mold compound, epoxy, adhesive, and/or other material to bond the parts together and/or protect the electrical interconnections.

**[0033]** One feature of the packaged microelectronic device embodiment described above with reference to Figure 8 is that the contacts 613 are distributed over a relatively large area on the die 610 inboard of the corresponding terminals 612. One advantage of this feature is that it reduces congestion on the second surface 762 of the interconnecting substrate 720 because it enables the contacts 722 to be placed on the first surface 761. Another advantage of this feature is that it eliminates the need for peripheral wire-bonds that extend from the terminals 612 to bond pads on the interconnecting substrate 720, as would be found on conventional COB packages. Eliminating these wire-bonds can make it easier to reduce the overall size of the device package 800.

**[0034]** From the foregoing, it will be appreciated that specific embodiments of the invention have been described herein for purposes of illustration, but that various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.

## CLAIMS

I claim:

[c1] 1. A microelectronic device comprising:

a microelectronic die, the microelectronic die including:

a first surface;

a second surface positioned opposite to the first surface;

an integrated circuit positioned at least partially between the first and second surfaces; and

a plurality of terminals positioned on the first surface and electrically coupled to the integrated circuit;

a plurality of contacts supported by the first surface of the die and positioned adjacent to the terminals; and

a plurality of wire-bonds, wherein each of the wire-bonds electrically couples one of the contacts to a corresponding terminal.

[c2] 2. The microelectronic device of claim 1 wherein the plurality of contacts is a plurality of first contacts supported by the first surface of the die and positioned to one side of the terminals, wherein the plurality of wire-bonds is a plurality of first wire-bonds, and wherein the microelectronic device further comprises:

a plurality of second contacts supported by the first surface of the die and positioned to the other side of the terminals; and

a plurality of second wire-bonds, wherein each of the second wire-bonds electrically couples one of the second contacts to a corresponding terminal.

[c3] 3. The microelectronic device of claim 1, further comprising an insulating layer attached to the first surface of the die, wherein the insulating layer carries the plurality of contacts.

[c4] 4. The microelectronic device of claim 1 wherein the plurality of contacts is a plurality of first contacts, wherein the plurality of wire-bonds is a plurality of first wire-bonds, and wherein the microelectronic device further comprises:

a first insulating layer portion laminated to the first surface of the die on one side of the terminals, wherein the first insulating layer portion carries the plurality of first contacts;

a second insulating layer portion laminated to the first surface of the die on the other side of the terminals;

a plurality of second contacts carried by the second insulating layer portion; and

a plurality of second wire-bonds, wherein each of the second wire-bonds electrically couples one of the second contacts to a corresponding

[c5] 5. The microelectronic device of claim 1 wherein the plurality of terminals includes a plurality of first terminals and a plurality of second terminals, wherein the plurality of first terminals is aligned along one side of the first surface and the plurality of second terminals is aligned along the other side of the first surface, and wherein the plurality of contacts is positioned between the plurality of first terminals and the plurality of second terminals.

[c6] 6. The microelectronic device of claim 1 wherein the plurality of terminals includes a plurality of first terminals and a plurality of second terminals, wherein the plurality of first terminals is aligned along one side of the first surface and the plurality of second terminals is aligned along the other side of the first surface, and wherein the microelectronic device further comprises an insulating layer portion attached to the first surface of the die between the plurality of first terminals and the plurality of second terminals, wherein the insulating layer portion carries the plurality of contacts.

[c7] 7. A microelectronic device comprising:

a microelectronic die, the microelectronic die including:

a first surface;

a second surface positioned opposite to the first surface;

an integrated circuit positioned at least partially between the first and second surfaces; and

a plurality of terminals positioned on the first surface and electrically coupled to the integrated circuit; and

an intermediate substrate attached to the first surface of the microelectronic die, wherein the intermediate substrate includes a plurality of contacts positioned adjacent to the terminals, and wherein each of the contacts is electrically coupled to a corresponding terminal.

[c8] 8. The microelectronic device of claim 7, further comprising a plurality of wire-bonds, wherein each of the contacts on the intermediate substrate is electrically coupled to a corresponding terminal with one of the wire-bonds.

[c9] 9. The microelectronic device of claim 7 wherein the plurality of contacts is a plurality of first contacts positioned to one side of the terminals, and wherein the intermediate substrate further includes a plurality of second contacts positioned to the other side of the terminals, wherein each of the second contacts is electrically coupled to a corresponding terminal.

[c10] 10. The microelectronic device of claim 7 wherein the plurality of contacts is a plurality of first contacts positioned to one side of the terminals, wherein the intermediate substrate further includes a plurality of second contacts positioned to the other side of the terminals, and wherein the microelectronic device further comprises:

a plurality of first wire-bonds electrically coupling each of the first contacts to a corresponding terminal; and

a plurality of second wire-bonds electrically coupling each of the second contacts to a corresponding terminal.

[c11] 11. The microelectronic device of claim 7 wherein the plurality of terminals includes a plurality of first terminals and a plurality of second terminals, wherein the plurality of first terminals is positioned to one side of the first surface of the die and the plurality of second terminals is positioned to the other side of the first surface of the die, and wherein the plurality of contacts is positioned between the plurality of first terminals and the plurality of second terminals.

[c12] 12. The microelectronic device of claim 7 wherein the plurality of terminals includes a plurality of first terminals and a plurality of second terminals, wherein the plurality of first terminals is positioned to one side of the first surface of the die and the plurality of second terminals is positioned to the other side of the first surface of the die, wherein the plurality of contacts is positioned between the plurality of first terminals and the plurality of second terminals, and wherein the microelectronic device further comprises:

a plurality of first wire-bonds electrically coupling each of the first terminals to a corresponding one of the contacts; and

a plurality of second wire-bonds electrically coupling each of the second terminals to a corresponding one of the contacts.

[c13] 13. A microelectronic device comprising:

a microelectronic die, the microelectronic die including:

a first surface;

a second surface positioned opposite to the first surface;

an integrated circuit positioned at least partially between the first and second surfaces;

a plurality of first terminals positioned on the first surface and electrically coupled to the integrated circuit;

a plurality of second terminals positioned on the first surface and electrically coupled to the integrated circuit, wherein the plurality of second terminals is spaced apart from the plurality of first terminals;

a plurality of first contacts supported by the first surface and positioned between the plurality of first terminals and the plurality of second terminals;

a plurality of second contacts supported by the first surface and positioned between the plurality of first terminals and the plurality of second terminals;

a plurality of first wire-bonds electrically coupling each of the first terminals to a corresponding first contact; and

a plurality of second wire-bonds electrically coupling each of the second terminals to a corresponding second contact.

[c14] 14. The microelectronic device of claim 13, further comprising an insulating layer attached to the first surface separate from the first and second terminals, wherein at least a portion of the first contacts are carried by the insulating layer.

[c15] 15. The microelectronic device of claim 13 wherein each of the first and second contacts includes metallic plating configured to be attached to solder material, and wherein the microelectronic device further comprises:

a first insulating layer portion laminated to the first surface; and

a second insulating layer portion laminated to the first surface, wherein the first insulating layer portion carries the plurality of first contacts and the second insulating layer portion carries the plurality of second contacts.

[c16] 16. The microelectronic device of claim 13 wherein the plurality of first terminals is aligned proximate to one edge of the microelectronic die, and wherein the plurality of second terminals is aligned proximate to an opposite edge of the microelectronic die.

[c17] 17. A packaged microelectronic device comprising:

a microelectronic die having a plurality of terminals electrically coupled to an integrated circuit;

a plurality of first contacts supported by the microelectronic die;

a plurality of wire-bonds individually coupling each of the first contacts to a corresponding one of the terminals on the die;

an interconnecting substrate attached to the microelectronic die;

a plurality of second contacts supported by the interconnecting substrate; and

a plurality of conductive couplers electrically connecting each of the first contacts on the die to a corresponding one of the second contacts on the interconnecting substrate.

[c18] 18. The packaged microelectronic device of claim 17 wherein the plurality of first contacts on the microelectronic die faces the plurality of second contacts on the interconnecting substrate.

[c19] 19. The packaged microelectronic device of claim 17 wherein the plurality of first contacts on the microelectronic die are positioned in vertical alignment with the plurality of second contacts on the interconnecting substrate.

[c20] 20. The packaged microelectronic device of claim 17 wherein the plurality of first contacts on the microelectronic die are positioned in vertical alignment with the plurality of second contacts on the interconnecting substrate, and wherein the plurality of first contacts on the microelectronic die faces the plurality of second contacts on the interconnecting substrate.

[c21] 21. The packaged microelectronic device of claim 17 wherein the interconnecting substrate is offset from the microelectronic die to define a space therebetween, and wherein the plurality of wire-bonds are positioned entirely within the space between the microelectronic die and the interconnecting substrate.

[c22] 22. The packaged microelectronic device of claim 17 wherein the microelectronic die is bonded to the interconnecting substrate with adhesive, and wherein the adhesive encases at least the plurality of conductive couplers.

[c23] 23. The packaged microelectronic device of claim 17 wherein the microelectronic die is bonded to the interconnecting substrate with adhesive, and wherein the adhesive encases at least the plurality of first contacts, the plurality of second contacts, the plurality of wire-bonds, and the plurality of conductive couplers.

[c24] 24. The packaged microelectronic device of claim 17, further comprising an insulating layer attached to a surface of the microelectronic die, wherein the first contacts are carried by the insulating layer.

[c25] 25. The packaged microelectronic device of claim 17 wherein the plurality of wire-bonds is a plurality of first wire-bonds and the plurality of conductive couplers is a plurality of first conductive couplers, and wherein the packaged microelectronic device further comprises:

a plurality of third contacts supported by the microelectronic die, wherein the third contacts are positioned to one side of the terminals on the die, and the first contacts are positioned to the other side of the terminals on the die;

a plurality of second wire-bonds individually coupling each of the third contacts to a corresponding one of the terminals on the die;

a plurality of fourth contacts supported by the interconnecting substrate; and

a plurality of second conductive couplers electrically connecting each of the third contacts on the die to a corresponding one of the fourth contacts on the interconnecting substrate.

[c26] 26. The packaged microelectronic device of claim 25 wherein the second contacts on the interconnecting substrate are vertically aligned with the first contacts on the die, and wherein the fourth contacts on the interconnecting substrate are vertically aligned with the third contacts on the die.

[c27] 27. The packaged microelectronic device of claim 25 wherein the second contacts and the fourth contacts on the interconnecting substrate face the first contacts and the third contacts on the die.

[c28] 28. The packaged microelectronic device of claim 17 wherein the plurality of wire-bonds is a plurality of first wire-bonds and the plurality of conductive couplers is a plurality of first conductive couplers, and wherein the packaged microelectronic device further comprises:

a first insulating layer portion attached to a surface of the microelectronic die on one side of the terminals, wherein the first contacts are carried by the first insulating layer portion;

a second insulating layer portion attached to the surface of the microelectronic die on the other side of the terminals;

a plurality of third contacts carried by the second insulating layer portion;

a plurality of second wire-bonds individually coupling each of the third contacts to a corresponding one of the terminals on the die;

a plurality of fourth contacts supported by the interconnecting substrate; and

a plurality of second conductive couplers electrically connecting each of the third contacts on the die to a corresponding one of the fourth contacts on the interconnecting substrate.

[c29] 29. The packaged microelectronic device of claim 17 wherein the plurality of terminals on the microelectronic die is a plurality of first terminals, wherein the microelectronic die further includes a plurality of second terminals spaced apart from the first terminals and electrically coupled to the integrated circuit, wherein the plurality of wire-bonds is a plurality of first wire-bonds individually coupling each of the first contacts to a corresponding one of the first terminals, wherein the plurality of conductive couplers is a plurality of first conductive couplers, and wherein the packaged microelectronic device further comprises:

a plurality of third contacts supported by the microelectronic die, wherein the first contacts and the third contacts are positioned between the first terminals and the second terminals on the die;

a plurality of second wire-bonds individually coupling each of the third contacts to a corresponding one of the second terminals;

a plurality of fourth contacts supported by the interconnecting substrate; and

a plurality of second conductive couplers electrically connecting each of the third contacts on the die to a corresponding one of the fourth contacts on the interconnecting substrate.

[c30] 30. The packaged microelectronic device of claim 17 wherein the plurality of terminals on the microelectronic die is a plurality of first terminals, wherein the microelectronic die further includes a plurality of second terminals spaced apart from the first terminals and electrically coupled to the integrated circuit, wherein the plurality of wire-bonds is a plurality of first wire-bonds individually coupling each of the first contacts to a corresponding one of the first terminals, wherein the plurality of conductive couplers is a plurality of first conductive couplers, and wherein the packaged microelectronic device further comprises:

a first insulating layer portion attached to a surface of the microelectronic die between the first terminals and the second terminals, wherein the first contacts are carried by the first insulating layer portion;

a second insulating layer portion attached to the surface of the microelectronic die between the first terminals and the second terminals;

a plurality of third contacts carried by the second insulating layer portion;

a plurality of second wire-bonds individually coupling each of the third contacts to a corresponding one of the second terminals;

a plurality of fourth contacts supported by the interconnecting substrate; and

a plurality of second conductive couplers electrically connecting each of the third contacts on the die to a corresponding one of the fourth contacts on the interconnecting substrate.

[c31] 31. A packaged microelectronic device comprising:

a microelectronic die having a plurality of terminals electrically coupled to an integrated circuit;

a plurality of first contacts supported by the microelectronic die;

a plurality of conductive lines individually coupling each of the first contacts to a corresponding one of the terminals;

an interconnecting substrate attached to the microelectronic die, the interconnecting substrate having a first surface facing toward the die and a second surface facing away from the die;

a plurality of second contacts supported by the first surface of the interconnecting substrate;

a plurality of ball-pads supported by the second surface of the interconnecting substrate, wherein each of the ball-pads is electrically coupled to a corresponding one of the second contacts; and

a plurality of conductive couplers electrically connecting each of the first contacts on the die to a corresponding one of the second contacts on the interconnecting substrate.

[c32] 32. The packaged microelectronic device of claim 31 wherein each of the terminals on the die is electrically coupled to a corresponding first contact with a first

conductive line, and wherein each of the ball-pads on the second surface of the interconnecting substrate is electrically coupled to a corresponding second contact with a second conductive line that includes at least a portion of a conductive via extending through the interconnecting substrate.

[c33] 33. The packaged microelectronic device of claim 31 wherein each of the terminals on the die is electrically coupled to a corresponding first contact with a first conductive line that includes a wire-bond, and wherein each of the ball-pads on the second surface of the interconnecting substrate is electrically coupled to a corresponding second contact with a second conductive line that includes at least a portion of a conductive via extending through the interconnecting substrate.

[c34] 34. The packaged microelectronic device of claim 31 wherein the plurality of first contacts on the die faces the plurality of second contacts on the second surface of the interconnecting substrate.

[c35] 35. The packaged microelectronic device of claim 31 wherein the plurality of first contacts are arranged in a first pattern and the plurality of second contacts are arranged in a second pattern, and wherein the first pattern is a mirror image of the second pattern.

[c36] 36. The packaged microelectronic device of claim 31 wherein the interconnecting substrate is offset from the microelectronic die to define a space therebetween, and wherein the plurality of conductive lines are positioned entirely within the space between the microelectronic die and the interconnecting substrate.

[c37] 37. The packaged microelectronic device of claim 31 wherein the microelectronic die is bonded to the interconnecting substrate with mold compound, and wherein the mold compound encases at least the plurality of conductive couplers.

[c38] 38. The packaged microelectronic device of claim 31 wherein mold compound encases at least the plurality of first contacts, the plurality of second contacts, the plurality of conductive lines, and the plurality of conductive couplers.

[c39] 39. A packaged microelectronic device comprising:

a microelectronic die having a plurality of terminals electrically coupled to an integrated circuit;

a plurality of first contacts supported by the microelectronic die;

an interconnecting substrate attached to the microelectronic die, the interconnecting substrate having a first surface facing toward the die and a second surface facing away from the die;

a plurality of second contacts supported by the first surface of the interconnecting substrate;

means for electrically coupling each of the terminals on the microelectronic die to a corresponding one of the first contacts on the die; and

means for electrically connecting each of the first contacts on the die to a corresponding one of the second contacts on the interconnecting substrate.

[c40] 40. The packaged microelectronic device of claim 39 wherein the means for electrically coupling each of the terminals on the die to a corresponding one of the first contacts on the die include a wire-bond.

[c41] 41. The packaged microelectronic device of claim 39 wherein the means for electrically connecting each of the first contacts on the die to a corresponding one of the second contacts on the interconnecting substrate include reflowed solder material.

[c42] 42. The packaged microelectronic device of claim 39, further comprising insulating means for supporting the plurality of first contacts on a surface of the die.

[c43] 43. A method of manufacturing a microelectronic device, the method comprising:

forming a plurality of terminals on a surface of a microelectronic die having an integrated circuit, wherein each of the terminals is electrically coupled to the integrated circuit;

forming a plurality of contacts adjacent to the terminals on the surface of the microelectronic die; and

electrically connecting each of the contacts to a corresponding terminal with a wire-bond.

[c44] 44. The method of claim 43 wherein forming a plurality of terminals includes arranging the terminals in a line proximate to a central portion of the surface of the microelectronic die, and wherein forming a plurality of contacts adjacent to the terminals includes forming a first plurality of contacts to one side of the terminals and a plurality of second contacts to the other side of the terminals.

[c45] 45. The method of claim 43 wherein forming a plurality of terminals includes arranging a plurality of first terminals proximate to one edge of the microelectronic die and arranging a plurality of second terminals proximate to an opposite edge of the

microelectronic die, and wherein forming a plurality of contacts adjacent to the terminals includes forming a plurality of contacts between the plurality of first terminals and the plurality of second terminals.

[c46] 46. The method of claim 43, further comprising laminating an insulating layer to the surface of the microelectronic die, wherein forming a plurality of contacts adjacent to the terminals includes forming the plurality of contacts on the insulating layer.

[c47] 47. A method of manufacturing a packaged microelectronic device, the method comprising:

forming a plurality of terminals on a microelectronic die having an integrated circuit, wherein each of the terminals is electrically coupled to the integrated circuit;

forming a plurality of first contacts adjacent to the terminals;

electrically coupling each of the first contacts to a corresponding one of the terminals;

forming a plurality of second contacts on an interconnecting substrate;

positioning the interconnecting substrate so that the plurality of second contacts on the substrate face the plurality of first contacts on the microelectronic die; and

electrically coupling each of the first contacts on the die to a corresponding one of the second contacts on the interconnecting substrate.

[c48] 48. The method of claim 47 wherein electrically coupling each of the first contacts to one of the terminals includes attaching a wire-bond from each of the first contacts to a corresponding one of the terminals.

[c49] 49. The method of claim 47, further comprising attaching an insulating layer to a surface of the microelectronic die, wherein forming a plurality of first contacts adjacent to the terminals includes forming a plurality of first contacts on the insulating layer.

[c50] 50. The method of claim 47 wherein electrically coupling each of the first contacts on the die to a corresponding one of the second contacts on the interconnecting substrate includes reflowing solder material between adjacent pairs of first and second contacts.

[c51] 51. The method of claim 47 wherein forming a plurality of second contacts on an interconnecting substrate includes forming a plurality of second contacts on a first surface of the interconnecting substrate that faces toward the microelectronic die, and wherein the method further comprises forming a plurality of third contacts on a second surface of the interconnecting substrate that faces away from the microelectronic die, wherein each of the third contacts is electrically coupled to one of the second contacts by conductive lines that extend at least partially through the interconnecting substrate.

[c52] 52. The method of claim 47 wherein forming a plurality of second contacts on an interconnecting substrate includes forming a plurality of second contacts on a first surface of the interconnecting substrate that faces toward the microelectronic die, and wherein the method further comprises forming a plurality of ball-pads on a second surface of the interconnecting substrate that faces away from the microelectronic die, wherein each of the ball-pads is electrically coupled to one of the second contacts by a conductive lines that includes a portion of a via that extends through the interconnecting substrate.

[c53] 53. The method of claim 47 wherein positioning the interconnecting substrate includes offsetting the interconnecting substrate from the microelectronic die to define a space therebetween, and wherein the method further comprises filling the space with mold compound.

[c54] 54. The method of claim 47 wherein electrically coupling each of the first contacts on the die to a corresponding second contact on the interconnecting substrate includes forming a solder connection between opposing pairs of first and second contacts, and wherein the method further comprises filling a space between the interconnecting

substrate and the microelectronic die with mold compound that encapsulates the plurality of terminals, the plurality of first contacts, the plurality of second contacts, and the solder connections.