DATA PROCESSING APPARATUS FOR DYNAMICALLY SETTING TIMINGS IN A DYNAMIC MEMORY SYSTEM

ABSTRACT

A data processing system includes a memory controller for accessing a dynamic memory having a plurality of SIMMs that differ in size and speed of operation. The memory controller is operable in response to a request to access a given SIMM to read a SIMM definition register and dynamically produce memory access signals in accordance with the timing requirements of the particular SIMM being accessed. Such signals are set each time a SIMM is accessed. The signals provide different clock periods of RAS precharge time, RAS to CAS time, and CAS pulse width.