Description

Title of Invention: Heterostructure Comprising a Rough Exposed Portion of a Support Substrate

[0001] The present invention relates to heterostructures provided for the manufacture of Piezo on Insulator, POI, structures, in particular, POI structures usable for the manufacturing of microelectronic, micromechanical and photonic devices, and manufacturing processes for such heterostructures.

[0002] In the field of microelectronics, micromechanics and photonics POI structures are of increasing importance due to superior sensibility and information propagation properties, for example. For example, devices as surface acoustic wave (SAW) devices, or bulk acoustic wave (BAW) devices utilizing the piezoelectric effect to transduce an electrical signal into a mechanical / acoustic wave offer particularly advantageous options, not only for applications in telecommunication, due to a wide variety of measurable ambient parameters including temperature, pressure, strain and torque, for example.

[0003] A typical POI structure comprises a layer of piezoelectric material, in particular, a single-crystal material, such as, for example, lithium niobate ($LiNbO_3$) or lithium tantalate ($LiTaO_3$), formed on a substrate, for example, made of silicon. Various processes of forming a thin layer of piezoelectric material on the substrate are known in the art. Application of the Smart Cut™ technology has been proven particular advantageous. According to this technology (see, for example, WO 2019/186032,WO 2020/200986 A1, EP4131337 or FR3137792), a heterostructure (donor virtual structure or pseudodonor) comprising a piezoelectric substrate formed on a support substrate is provided. The piezoelectric substrate is implanted by light species (H and/ or He) to form a weakened region in the piezoelectric substrate and afterwards the piezoelectric substrate is bonded to a target substrate. By fracture at the weakened region a thin layer of piezoelectric material can be obtained on the target substrate.

[0004] One problem that arises when producing such a pseudodonor is its fragility. Specifically, the piezoelectric substrates used in microelectronics are provided with a peripheral chamfer which makes it possible to avoid having sharp angles, which are particularly fragile, on the edge of the piezoelectric substrates. The chamfers make it easier to handle the substrates and to avoid edge fragments which could be produced if these edges were projecting edges, such fragments being sources of particulate contamination of wafer surfaces. Given the thinness of the thinned piezoelectric substrate, said piezoelectric substrate has an inclined edge due to the chamfer and thus forms a very thin and brittle strip. However, the debris created by this strip breaking

is liable to contaminate the production line and the substrates produced on this line. Therefore, is has been proposed (WO 2022/195225 A1) to remove an annular portion from the piezoelectric substrate before or after the bonding of that piezoeleectric substrate to the support substrate of the pseudodonor which allows for preventing the formation of a brittle strip of piezoelectric material.

[0005] Due to the removal of the annular portion from the piezoelectric substrate, however, the support substrate is partially exposed to ion implantation for each layer transfer for which the pseudodonor is (re)used since current refresh procedures for re-usage only address the preparation of the surface of the piezoelectric layer. Due to the exposure of a portion of the support substrate implanted species for forming the weakened layer in the piezoelectric substrate accumulate in this portion as well which, disadvantageously, may result in blistering and flaking if a certain threshold of the concentration of the accumulated implantation in the exposed portion of the support substrate is exceeded.

[0006] Therefore, it is an object of the present invention to provide a high-quality hetereostructure for the manufacture of POI structures that is free of blistering and flaking.

[0007] The present invention addresses this object by providing a method of manufacturing a heterostructure (pseudodonor, PSD, or donor virtual structure) for the manufacture of a Piezoelectric on Insulator, POI, structure, comprising the steps of (subsequently performed in the given order):

[0008] providing a support (handling) substrate (for example, a silicon substrate);

[0009] forming a block of a piezoelectric material (for example, consisting of or comprising a lithium tantalite or lithium niobate substrate) on or over the support substrate;

[0010] removing a first peripheral portion of the block of a piezoelectric material and a first peripheral portion of the support substrate (below a part of the first peripheral portion of the block) to obtain an exposed portion of the support substrate (free of removed piezoelectric material) with a roughness with a root-mean-square height, Sq, in the range of 0.4 μm to 0.8 μm, for example, 0.5 μm to 0.7 μm;

[0011] thinning the block of a piezoelectric material after removal of the first peripheral portion of the block of a piezoelectric material to obtain a piezoelectric substrate;.

[0012] Here and in the following parameters related to the roughness are defined by the standard ISO 25178 and measured by a 3D optical profilometer from Wyko, for example, with a 15X or 75 X objective.

[0013] It has been found that a roughness with a root-mean-square height, Sq, in the range of 0.4 μm to 0.8 μm, for example, 0.5 μm to 0.7 μm, advantageously, allows during a thermal treatment at a later processing step (for example, for detachment of a to-be-transferred piezoelectric layer) for efficient out-diffusing of species that are inevitably implanted into the exposed portion of the support substrate during the process of

implanting the species into the piezoelectric substrate for forming the weakened layer needed for facilitating layer transfer to a target substrate. The root-mean-square height, Sq, may be of the same order of magnitude as the implantation depth of the species (which depends on the chosen implantation energy). Blistering and flaking of the support substrate can effectively prevented by the out-diffusion of the implanted species.

[0014] It is noted that after refresh of the piezoelectric substrate following a first layer transfer process another layer transfer process, in fact, a number of (for example, 6) subsequent layer transfer processes, can be performed by means of the heterostructure. Thus, the exposed portion of the support substrate is subject to a number of implantation processes. The root-mean-square height, Sq, according to the invention efficiently counteracts the accumulation of species implanted in the exposed portion of the support substrate that otherwise would give rise to a significant risk of blistering and flaking.

[0015] The piezoelectric substrate obtained by thinning of the block of piezoelectric material may be subject to chemical-mechanical polishing, CMP. Forming the block of piezoelectric material on or over the support substrate may comprise bonding the block of piezoelectric material to the support substrate by means of a dielectric bonding layer, for example, a photo (UV) polymer layer or a layer made of or comprising silicon oxide and/or silicon nitride.

[0016] According to an embodiment, the exposed portion of the support substrate is obtained with a roughness with a maximum height, Sz, in the range of 4 μm to 8 μm, for example, 5 μm to 7 μm. A maximum height in that range may further facilitate the out-diffusion of implanted species from the exposed portion of the support substrate.

[0017] Other roughness parameters that based on experiments have been proven to be advantageous with respect to out-diffusion of specified implanted in to the exposed portion of the support substrate during subsequent thermal treatment comprise a period of roughness in the range of 0.15 μm to 1.5 μm, in particular, 0.3 μm to 0.5 μm.

[0018] Particularly, both the block of piezoelectric material and the support substrate are chamfered. According to an embodiment, the method of manufacturing a heterostructure further comprises forming a chamfer in a second peripheral portion of the block of a piezoelectric material and forming a chamfer in a second peripheral portion of the support substrate before forming the block of a piezoelectric material on or over the support substrate. For example, the first peripheral portion of the block of a piezoelectric material comprises at least a part of the second peripheral portion of the same such that a part or even the entire chamfered portion of the block of a piezoelectric material is no longer present in the piezoelectric substrate due to the removal of the first peripheral portion of the block of a piezoelectric material.

For example, a small part only of the chamfered portion of the support substrate is removed by removing the first peripheral portion of the support substrate.

[0019] According to an embodiment, removing the first peripheral portion of the block of a piezoelectric material and the first peripheral portion of the support substrate is performed by grinding by means of an abrasive wheel. In this case, the method may further comprise placing the support substrate with the block of a piezoelectric material formed thereon or there over on a carrier that is rotatably movable about a first axis and rotating the abrasive wheel about a second axis parallel to the first axis. The abrasive wheel is gradually moved towards the substrate in a direction parallel to the first axis in order to gradually grind away the material of the substrate. It has been found that this particular procedure of grinding may reliably result in the desired roughness characteristics that facilitate the out-diffusion of species implanted in the exposed portion of the support substrate. It is noted that depending on the width of the peripheral portions to be removed, the abrasive wheel may be moved in a direction perpendicular to the first axis in order to gradually grind away the material of the intermediate heterostructure in the radial direction.

[0020] Furthermore, it is provided a method of manufacturing a Piezoelectric on Insulator, POI, structure comprising performing the steps of the method of manufacturing a heterostructure according to one of the above-described examples, implanting a species (for example, hydrogen, maybe supplemented by helium) into the piezoelectric substrate to obtain a weakened layer in the piezoelectric substrate and transferring a piezoelectric layer from the piezoelectric substrate to a target substrate comprising bonding the heterostructure to the target substrate at the side of the piezoelectric substrate and fracturing the piezoelectric substrate at the weakened layer, for example, in an anneal process.

[0021] Thereby, the piezoelectric layer can be reliably transferred to the target substrate without too heavy defects. Further post-processing (annealing and polishing) may, however, still be needed to provide a piezoelectric layer suitable for particular applications. It is noted that naturally occurring silicon oxide may be present between the transferred piezoelectric layer and the target substrate. Further, a dielectric assembly layer may be formed on or over a surface of the target substrate before transfer of the piezoelectric layer to that surface. This dielectric assembly layer may be made of or comprise silicon oxide and/or silicon nitride or a stack of layers composed of these materials. Moreover, depending on the actual application a charge trapping layer may be formed on or over a surface of the target substrate before transfer of the piezoelectric layer to that surface. The charge trapping layer may be made of or comprise polycrystalline silicon.

[0022] After layer transfer from the heterostructure to the target substrate has been completed the piezoelectric substrate can be re-freshed (in particular, polished) for reuse of the hetereostructure for a next layer transfer process.

[0023] Furthermore, it is provided a Piezoelectric on Insulator, POI, structure comprising a piezoelectric layer formed on or over a target substrate and obtainable by the method of manufacturing a POI structure. Additionally, it is provided a microelectronic, micromechanical or photonic device or micro-electro-mechanical system comprising such a POI structure.

[0024] The above-mentioned object of the present invention is also addressed by providing a heterostructure for the manufacture of a Piezoelectric on Insulator, POI, structure, the heterostructure comprising a support substrate (for example, a silicon substrate), a piezoelectric substrate (for example, a lithium tantalite or lithium niobate substrate) formed on or over the support substrate. The support substrate comprises an exposed peripheral portion free of material of the piezoelectric substrate and the peripheral portion of the support substrate has a roughness with a root-mean-square height, Sq, in the range of 0.4 μm to 0.8 μm. Particularly, the peripheral portion of the support substrate of the heterostructure may have a roughness with a maximum height in the range of 4 μm to 8 μm. More particularly, the peripheral portion of the support substrate of the heterostructure may have a roughness with a period in the range of 0.15 μm to 1.5 μm. The support substrate of the provided heterostructure may be chamfered and may contain a weakened layer formed in the piezoelectric substrate by ion implantation.

[0025] The heterostructure may be formed according to one of the above-described examples of a method of manufacturing heterostructure or may be a re-freshed heterostructure obtained by re-feshing the piezoelectric substrate after a previously performed transfer of a piezoelectric layer (part of the piezoelectric substrate) to a target substrate. After respective re-fresh processes performed on the piezoelectric substrate the hetereostructure can be used several (or example, 6) times for subsequent layer transfer processes.

[0026] Additional features and advantages of the present invention will be described with reference to the drawings. In the description, reference is made to the accompanying Figures that are meant to illustrate preferred embodiments of the invention. It is understood that such embodiments do not represent the full scope of the invention.

[0027] [Fig.1] illustrates steps of a method of manufacturing a heterostructure according to an embodiment of the present invention.

[0028] [Fig.2A] illustrates different manufacturing states of a heterostructure according to an embodiment of the present invention.

[0029] [Fig.2B] illustrates different manufacturing states of a heterostructure according to an embodiment of the present invention.

[0030] [Fig.2C] illustrates different manufacturing states of a heterostructure according to an embodiment of the present invention.

[0031] [Fig.3] illustrates a procedure of removing peripheral portions of a massive block of a piezoelectric material and a support substrate of an intermediate heterostructure according to an embodiment of the present invention.

[0032] Herein, it is provided a method of manufacturing a heterostructure comprising a piezoelectric substrate formed on or over a support substrate wherein the heterostructure is intended to be used for the manufacture of a POI structure. The present invention is however not limited to piezoelectric materials, and can be applied to any kind of material suitable for the subsequent transfer on a final substrate. In particular, for materials acting as donor material which have a coefficient of thermal expansion that is substantially different from the coefficient of thermal expansion of the final target substrate, it seems advantageous to form above mentioned heterostructure facilitating said transfer using the SmartCut™ Technology. The present invention allows avoiding any complications regarding the use of said heterostructure for several transfers by avoiding the cumulation of ionic species, in particular hydrogen and/or helium, that are used to determine the weakended zone of the layer to be transferred, in the support substrate and, thus, avoiding blistering or flaking of any kind. The support substrate of the resulting heterostructure comprises an exposed peripheral portion free of the donor material, in particular of the piezoelectric substrate, wherein the exposed peripheral portion exhibits a dedicated roughness that allows for efficient out-diffusion of unintentionally implanted ions (used for the generation of a weakened layer in the piezoelectric substrate) during some thermal treatment. The method may be comprised by a method of manufacturing a POI structure according to the Smart Cut™ technology.

[0033] [Fig.1] illustrates steps of a method of manufacturing a heterostructure according to an embodiment of the present invention. The method comprises forming 11 a chamfered massive block of piezoelectric material on or over a chamfered support substrate. The piezoelectric material may be lithium tantalate ($LiTaO_3$) or lithium niobate ($LiNbO_3$). The function of the support substrate is to temporarily support a piezoelectric substrate to be formed from the massive block of piezoelectric material until a portion of the piezoelectric substrate (piezoelectric layer) is transferred to a target substrate.

[0034] The thickness of the support substrate may be a few hundreds of micrometres. The support substrate may be made of a material (or a plurality of materials) with a

coefficient of thermal expansion close to that exhibited by a target substrate to which a piezoelectric layer is to be transferred. Particularly, the thermal expansion coefficient of the support substrate may differ from the one of the target substrate by less than the difference of the thermal expansion coefficient of the piezoelectric substrate and that of the target substrate. The support substrate and the target substrate may have identical thermal expansion coefficients and both substrates may, for example, consist of or comprise silicon. Other possible materials of the support substrate comprise glass, quartz, sapphire, a ceramic, or polycrystalline aluminium nitride (AlN). As already mentioned, the present invention is not limited to piezoelectric materials, and similar reasoning can be applied to other materials suitable for the transfer of a layer to a target substrate.

[0035] The chamfers of the support substrate and the massive block of piezoelectric material may have angles of 22° to 40° with respect to the respective main surfaces and may extend over a height in the range of 200 to 300 μm in the direction of the respective thicknesses and a width in the range of 200 to 300 μm in the radial direction of the respective substrate/block.

[0036] Forming 11 the chamfered massive block of piezoelectric material on or over the chamfered support substrate may comprise attaching the chamfered massive block of piezoelectric material to the chamfered support substrate using a bonding technique. The bonding may be of molecular adhesion type and/or mediated by a dielectric bonding (adhesion) layer, for example, a photo (UV) polymer layer or a layer made of or comprising silicon oxide and/or silicon nitride. The polymeric layer may be formed by depositing a photopolymerizable layer on the surface of at least one of the block and the support substrate, bonding the block to the support substrate via the photopolymerizable layer and irradiating the thus resulting assembly. The bonding process may include the application of a low temperature heat treatment (for example, at a temperature between 50 and 300°C, typically 100°C) making it possible to sufficiently reinforce the bonding energy to allow a later procedural step of thinning the block of piezoelectric material.

[0037] Due to the thinning of the massive block of piezoelectric material, however, a remaining chamfer of the resulting piezoelectric substrate would have a peripheral chamfered edge comprising a sharp angle at the level of the main face. An edge with such a sharp angle is liable to break when the heterostructure is handled, particularly, bonded to a target substrate. This breaking effect, called “flaking”, is particularly harmful because the debris from the thinned donor substrate might contaminate and damage the entire production line using the heterostructure. Such an effect can be avoided by removing a peripheral portion from the massive block of piezoelectric material or from the piezoelectric substrate. In principle, the peripheral portion may be

removed from the block before or preferentially after bonding to the support substrate. By the removal of the peripheral portion a chamfer remaining in the piezoelectric substrate after thinning of the block can at least be partly, in particular, fully removed from the piezoelectric substrate.

[0038] The method illustrated in [Fig.1] comprises removing 12 a peripheral portion of the chamfered block of piezoelectric material and a peripheral portion of the chamfered support substrate after bonding but before thinning of the block. After removal 12 of the respective peripheral portions a step 13 of thinning the massive block of piezoelectric material is performed to obtain a piezoelectric substrate.

[0039] During the step 12 of removing the peripheral portion of the chamfered block of piezoelectric material and the peripheral portion of the chamfered support substrate the resulting exposed portion of the support substrate is provided with a dedicated roughness characteristics.

[0040] The thinning step 13 is carried out in such a way that the resulting piezoelectric substrate has a sufficiently low thickness such that the stresses generated during heat treatment applied in a later processing stage are reduced. On the other hand, the thickness has to be sufficiently high in order to provide a piezoelectric layer that is to be transferred to a target substrate or to provide for a plurality of such layers that are to be transferred one after the other in multiple transfer steps (after respective regeneration of the piezoelectric substrate) to respective target substrates. The thickness of the piezoelectric substrate resulting from the thinning of the massive block can be, for example, between 5 and 400 μm, for example, 10 μm to 100 μm or 200 μm, in particular between 15 μm and 40 μm.

[0041] Thinning 13 of the block of piezoelectric material may be achieved by grinding, by chemical-mechanical polishing, or by etching that may be carried out in a number of steps. A first part of the block may be removed by coarse grinding, which allows the thickness of the block to be reduced rapidly. Next, finer grinding may be implemented to continue reducing the thickness of the block, while decreasing the roughness of the surface of the resulting piezoelectric substrate. Finally, chemical-mechanical polishing (CMP) may be carried out to smooth the surface of the piezoelectric substrate in order to achieve desired surface smoothness characteristics.

[0042] In step 14 of the method illustrated in [Fig.1] hydrogen and/or helium is implanted in the piezoelectric substrate to form a weakened layer which defines a piezoelectric layer to be transferred from the remainder part of the piezoelectric substrate. The nature and dose of the implanted species and the implantation energy can be chosen according to the thickness of the piezoelectric layer that is to be transferred to a target substrate and the physicochemical properties of the piezoelectric substrate 1a. For example, for a lithium tantalate substrate a dose of hydrogen ions between 10^{16} and $5 \bullet 10^{17}$ at/cm^2 with

an energy between 30 keV and 300 keV may be implanted to delimit a piezoelectric layer with a thickness of about 200 nm, for example.

[0043] The thus obtained heterostructure can be readily used for transfer of the piezoelectric layer to a target substrate. For this, the heterostructure is attached to the target substrate at the side of the piezoelectric substrate by molecular adhesion and/or electrostatic bonding. A dielectric assembly layer may be provided between the piezoelectric substrate of the heterostructure and the target substrate. The dielectric assembly layer may comprise an oxide and may be made of or comprise silicon oxide and/or silicon nitride or a stack of layers composed of these materials, or be made of amorphous silicon when adiabatic bonding is envisaged. Further, a charge trapping layer, for example, made of or comprising polycrystalline silicon, may be formed on or over the target substrate in order to enhance the electrical resistivity of the same if it is desired by an actual application.

[0044] The piezoelectric layer is then detached from the remainder part of the heterostructure to obtain a POI structure comprising the target substrate, the dielectric assembly layer (if provided), the charge trapping layer (if provided) and the piezoelectric layer. Detachment at the weakened layer may be facilitated by heat treatment in a temperature range of around 100°C to 600° to allow the transfer of the piezoelectric layer to the target substrate. Alternatively or additionally detachment at the weakened layer can be facilitated by the application of a blade or a jet of gaseous or liquid fluid or any other mechanical force applied to the weakened layer.

[0045] Post-processing of the transferred piezoelectric layer is necessary to obtain a transferred piezoelectric layer 3 having satisfactory mono-domain crystalline and surface quality (reduced roughness) and thickness uniformity as demanded by actual applications. The post-processing may comprise a heat treatment and polishing process.

[0046] During the ion implantation 14 ions are inevitably implanted in the exposed portion of the support substrate formed in step 12 of the method illustrated in [Fig.1]. After the above-described layer transfer the heterostructure can severally be reused after re-fresh of the piezoelectric substrate for further layer transfer processes and each re-fresh comprises again ion implantation. Accumulation of implanted ions in the exposed portion of the support substrate is avoided by the roughness characteristics intentionally provided for this exposed portion of the support substrate in step 12. The implantation region in the support substrate has an average depth depending on the implantation energy of the ions. The mean path length of the implanted species for out-diffusion during any thermal treatment is, however, much lower than this depth due to the roughness profile provided. The implanted species can be easily mobilized and can

quickly out-diffuse of the support substrate, thereby significantly reducing the risk of blistering caused by an accumulated dose of implanted species.

[0047] Experiments have proven that a roughness with a root-mean-square height, Sq, in the range of 0.4 μm to 0.8 μm, in particular, 0.5 μm to 0.7 μm, is suitable for reliably achieving this out-diffusion effect, particularly, in the case of a silicon substrate and hydrogen ions implanted with an energy between 30 keV and 300 keV. Out-diffusion of the implanted species from the support substrate may be further facilitated by a roughness with a maximum height, Sz, *i.e.*, difference between maximum peak height and maximum valley height, in the range of 4 μm to 8 μm, in particular, 5 μm to 7 μm. Out-diffusion of the implanted species from the support substrate may be further facilitated by a roughness with a period in the range of 0.15 μm to 1.5 μm, in particular, 0.3 μm to 0.5 μm.. All of the given parameters are determined according to the standard ISO 25178 and measured by a 3D optical profilometer from Wyko, for example, with a 15X or 75 X objective.

[0048] [Fig.2A] to 2C illustrate different manufacturing states of a (an intermediate) heterostructure according to an embodiment of the present invention. The shown manufacturing states might be obtained by means of steps of the method illustrated in [Fig.1]. As shown in [Fig.2A] a massive block of a piezoelectric material 1 is formed on or over a support substrate 2 to obtain an intermediate heterostructure. Although no bonding layer is shown in [Fig.2A], a polymeric layer as described above may be used to achieve the bonding between the block 1 and the support substrate 2.

[0049] Each of the block 1 and the support substrate 2 have a peripheral chamfer C on each of their respective main faces. [Fig.2A] schematically illustrates the operation of removing a peripheral portion of the massive block of a piezoelectric material 1 after bonding thereof to the support substrate 2 but before thinning of the block 1 to obtain a piezoelectric substrate (already indicated by reference number 10 in [Fig.2A]) of thickness e. In the shown example, the thickness e is smaller than the thickness of the chamfer C of the piezoelectric substrate to be formed from the block 1. The thick dashed line in [Fig.2A] delimits the peripheral portions of the block 1 and the support substrate 2 that are removed. In the shown example, the width L of the removed peripheral portion is greater than the entire width of the chamfers C, in particular, the width L lies in between 0.1 mm up to 5 mm. The support substrate 2 is removed over a depth ranging from 0.4 μm up to 0.8 μm, in particular at least the depth corresponding to the predetermined level of roughness necessary to outdiffuse implanted species from the support substrate 2.

[0050] [Fig.2B] is a cross-sectional view of the periphery of an intermediate heterostructure comprising the massive block of a piezoelectric material 1 (before thinning thereof) and the support substrate 2 after removal of the respective peripheral portions.

[0051] [Fig.2C] is a cross-sectional view of the periphery of the heterostructure H resulting from thinning of the block 1 to obtain the piezoelectric substrate 10. In the example shown only the support substrate 2 of the heterostructure H still exhibits a chamfer while the edge of the piezoelectric substrate 10 forms a right (alternatively, an obtuse) angle with the surface of the support substrate 1 and is therefore less liable to break.

[0052] [Fig.3] illustrates a procedure of removing peripheral portions of a massive block of a piezoelectric material and a support substrate of an intermediate heterostructure according to an embodiment of the present invention. The procedure may be used to perform step 12 of the method illustrated in [Fig.1] or to achieve the intermediate heterostructure shown in [Fig.2B].

[0053] The intermediate heterostructure is positioned on a support S rotated about an axis X1 (of revolution) of the intermediate heterostructure. A cutting tool T, such as an abrasive wheel, is rotated about an axis X2 parallel to the axis X1 and is brought towards the peripheral portions to be removed. Said tool is gradually moved towards the intermediate heterostructure in a direction parallel to the axis X1 in order to gradually grind away the material of the intermediate heterostructure that it contacts. As grinding wheel one could chose in a non-limitative example for instance a diamond wheel with synthetic diamond as abrasive material with an average grain size ranging from 10 μm to 100 μm, in particular around 50 μm.

[0054] The effect of the grinding is to locally harden the material ground by the tool such that the exposed surface exhibits a predetermined roughness. It may be advantageous to carry out polishing, for example chemical-mechanical polishing (CMP), of the surface of the piezoelectric substrate in order to prevent bonding defects during the subsequent transfer to a receiver substrate. The exposed portion of the support substrate is not polished and exhibits the above-described roughness characteristics that, advantageously, facilitates out-diffusion of implanted species during any subsequent thermal treatment.

Claims

[Claim 1] A method of manufacturing a heterostructure (H) for the manufacture of a Piezoelectric on Insulator, POI, structure, comprising

providing a support substrate (2);

forming (11) a block of a piezoelectric material (1) on or over the support substrate (2);

removing (12) a first peripheral portion of the block of a piezoelectric material (1) and a first peripheral portion of the support substrate (2) to obtain an exposed portion of the support substrate (2) with a roughness with a root-mean-square height, Sq, in the range of 0.4 μm to 0.8 μm;

thinning (13) the block of a piezoelectric material (1) after removal of the first peripheral portion of the block of a piezoelectric material (1) to obtain a piezoelectric substrate (10);.

[Claim 2] The method according to claim 1, wherein the first peripheral portion of the block of a piezoelectric material (1) and the first peripheral portion of the support substrate (2) are removed to obtain an exposed portion of the support substrate (2) with a roughness with a maximum height, Sz, in the range of 4 μm to 8 μm.

[Claim 3] The method according to claim 1 or 2, wherein the first peripheral portion of the block of a piezoelectric material (1) and the first peripheral portion of the support substrate (2) are removed to obtain an exposed portion of the support substrate (2) with a period of roughness in the range of 0.5 μm to 1.5 μm.

[Claim 4] The method according to one of the preceding claims, wherein the block of piezoelectric material (1) and the support substrate (2) are chamfered before forming (11) the block of a piezoelectric material (1) on or over the support substrate (2).

[Claim 5] The method according to one of the preceding claims, wherein removing the first peripheral portion of the block of a piezoelectric material (1) and the first peripheral portion of the

support substrate (2) is performed by grinding by means of an abrasive wheel (T).

[Claim 6] The method according to claim 5, further comprising

placing the support substrate (2) with the block of a piezoelectric material (1) formed thereon or there over on a carrier (S) that is rotatably movable about a first axis (X1); and

wherein the grinding comprises rotating the abrasive wheel (T) about a second axis (X2) parallel to the first axis (X1).

[Claim 7] A method of manufacturing a Piezoelectric on Insulator, POI, structure, comprising

performing the steps of one of the preceding claims;
implanting (14) a species into the piezoelectric substrate (10) to obtain a weakened layer in the piezoelectric substrate (10); and

transferring a piezoelectric layer from the piezoelectric substrate (10) to a target substrate comprising bonding the heterostructure (H) to the target substrate at the side of the piezoelectric substrate (10) and fracturing the piezoelectric substrate (10) at the weakened layer.

[Claim 8] Piezoelectric on Insulator, POI, structure, comprising a piezoelectric layer formed on or over a target substrate and obtainable by the method according to claim 7.

[Claim 9] Microelectronic, micromechanical or photonic device or micro-electro-mechanical system comprising the POI structure (9) according to claim 8.

[Claim 10] Heterostructure (1) for the manufacture of a Piezoelectric on Insulator, POI, structure, the heterostructure comprising

a support substrate (3);

a piezoelectric substrate (10) formed on or over the support substrate (2);

wherein

the support substrate (2) comprises an exposed peripheral portion free of material of the piezoelectric substrate (10) and the peripheral portion of the support substrate (2) has a roughness with a root-mean-square height, Sq, in the range of 0.4 μm to 0.8 μm.

[Claim 11] The heterostructure according to claim 10, the peripheral portion of the support substrate (2) has a roughness with a maximum height in the range of 4 μm to 8 μm.

[Claim 12] The heterostructure according to claim 10 or 11, the peripheral portion of the support substrate has a roughness with a period of roughness in the range of 0.5 μm to 1.5 μm.

[Claim 13] The heterostructure according to any of the claims 10 to 12, wherein the support substrate (2) is chamfered.

[Claim 14] The heterostructure according to any of the claims 10 to 13 further comprising a weakened layer formed in the piezoelectric substrate (10) by ion implantation.