

PIXEL CIRCUIT AND DRIVING METHOD THEREOF

BACKGROUND

Field of Invention

[0001] The present disclosure relates to a pixel circuit. More particularly, the present disclosure relates to a pixel circuit and a driving method thereof.

Description of Related Art

[0002] Micro LEDs have the advantages of low power consumption, high color saturation and high response speed, such that the micro LEDs have become one of the popular technologies used in next-generation display panels. Because the micro LED is a current-driven component, the pixel circuit of the micro LED requires plural transistors and plural signal lines to achieve emission control. Each pixel needs to contain three micro LEDs that emit the red (R) light, the green (G) light and the blue (B) light to achieve a full-color display. However, if the pixel circuit includes too many transistors and/or too many signal lines, it will be not beneficial to improve the aperture ratio and light transmittance.

SUMMARY

[0003] The present disclosure provides a pixel circuit. The pixel circuit includes a driving transistor, an emission control transistor, a first light-emitting element and a second light-emitting element. The driving transistor has a gate terminal for receiving a data signal. The emission control transistor is coupled between a first terminal of the driving transistor and a first system voltage terminal. The first light-

emitting element is coupled between a second terminal of the driving transistor and a second system voltage terminal to emit light with a first color. The second light-emitting element is coupled between the second terminal of the driving transistor and a third system voltage terminal to emit light with a second color different from the first color. A gate terminal of the emission control transistor receives an emission control signal. The first light-emitting element is controlled according to the emission control signal and a voltage level of the second system voltage terminal. The second light-emitting element is controlled according to the emission control signal and a voltage level of the third system voltage terminal. When the first light-emitting element or the second light-emitting element emits light, the voltage level of the second system voltage terminal is different from the voltage level of the third system voltage terminal.

[0004] In accordance with one or more embodiments of the present disclosure, the pixel circuit further includes a first transistor and a second transistor. The first transistor is coupled between the second terminal of the driving transistor and the second system voltage terminal and coupled to the first light-emitting element to drive the first light-emitting element. The second transistor is coupled between the second terminal of the driving transistor and the third system voltage terminal and coupled to the second light-emitting element to drive the second light-emitting element. A gate terminal of each of the first transistor and the second transistor receives the emission control signal. The first transistor is controlled according to the emission control signal and the voltage level of the second system voltage terminal. The second transistor is controlled according to the emission control signal and the voltage level of the third system voltage terminal.

[0005] In accordance with one or more embodiments of the present disclosure, the first system voltage terminal receives a system high voltage. A cathode of the first light-emitting element is coupled to the second system voltage terminal and an anode of the first light-emitting element is coupled to the second terminal of the driving transistor. A cathode of the second light-emitting element is coupled to the third system voltage terminal and an anode of the second light-emitting element is coupled to the second terminal of the driving transistor.

[0006] In accordance with one or more embodiments of the present disclosure, when the first light-emitting element emits light and the second light-emitting element does not emit light, the second system voltage terminal has a low voltage level and the third system voltage terminal has a high voltage level. When the first light-emitting element does not emit light and the second light-emitting element emits light, the second system voltage terminal has the high voltage level and the third system voltage terminal has the low voltage level.

[0007] In accordance with one or more embodiments of the present disclosure, the first system voltage terminal receives a system low voltage. An anode of the first light-emitting element is coupled to the second system voltage terminal and a cathode of the first light-emitting element is coupled to the second terminal of the driving transistor. An anode of the second light-emitting element is coupled to the third system voltage terminal and a cathode of the second light-emitting element is coupled to the second terminal of the driving transistor.

[0008] In accordance with one or more embodiments of the present disclosure, when the first light-emitting element emits light and the second light-emitting element does not emit light, the second system voltage terminal has a high

voltage level and the third system voltage terminal has a low voltage level. When the first light-emitting element does not emit light and the second light-emitting element emits light, the second system voltage terminal has the low voltage level and the third system voltage terminal has the high voltage level.

[0009] In accordance with one or more embodiments of the present disclosure, the pixel circuit further includes a third light-emitting element. The third light-emitting element is coupled between the second terminal of the driving transistor and a fourth system voltage terminal to emit light with a third color different from the first color and the second color. The third light-emitting element is controlled according to the emission control signal and a voltage level of the fourth system voltage terminal. During an emission period of the pixel circuit, a voltage level of one of the second system voltage terminal, the third system voltage terminal and the fourth system voltage terminal is different from voltage levels of the other two of the second system voltage terminal, the third system voltage terminal and the fourth system voltage terminal.

[0010] In accordance with one or more embodiments of the present disclosure, the pixel circuit further includes a third transistor. The third transistor is coupled between the second terminal of the driving transistor and the fourth system voltage terminal and coupled to the third light-emitting element to drive the third light-emitting element. A gate terminal of the third transistor receives the emission control signal. The third transistor is controlled according to the emission control signal and the voltage level of the fourth system voltage terminal.

[0011] In accordance with one or more embodiments of the present disclosure, the first system voltage terminal receives a system high voltage. During the

emission period of the pixel circuit, one of the second system voltage terminal, the third system voltage terminal and the fourth system voltage terminal has a low voltage level, and the other two of the second system voltage terminal, the third system voltage terminal and the fourth system voltage terminal have high voltage levels.

[0012] In accordance with one or more embodiments of the present disclosure, the first system voltage terminal receives a system low voltage. During the emission period of the pixel circuit, one of the second system voltage terminal, the third system voltage terminal and the fourth system voltage terminal has a high voltage level, and the other two of the second system voltage terminal, the third system voltage terminal and the fourth system voltage terminal have low voltage levels.

[0013] In accordance with one or more embodiments of the present disclosure, the pixel circuit further includes a first writing transistor. The first writing transistor has a first terminal to receive the data signal, a second terminal coupled to the gate terminal of the driving transistor, and a gate terminal to receive a first scanning signal. During a writing period of the pixel circuit, the first writing transistor is turned on according to the first scanning signal, thereby transmitting the data signal to the gate terminal of the driving transistor.

[0014] In accordance with one or more embodiments of the present disclosure, the pixel circuit further includes a second writing transistor and a first capacitor. The second writing transistor has a first terminal to receive an initial voltage and a second terminal coupled to the first terminal or the second terminal of the driving transistor. The first capacitor is coupled between the second terminal of the first

writing transistor and the second terminal of the second writing transistor. During the writing period of the pixel circuit, the second writing transistor transmits the initial voltage to the first terminal or the second terminal of the driving transistor.

[0015] In accordance with one or more embodiments of the present disclosure, the pixel circuit further includes a compensation circuit. The compensation circuit is coupled between the gate terminal of the driving transistor and the second terminal of the first writing transistor. The compensation circuit compensates a threshold voltage of the driving transistor through the first capacitor.

[0016] In accordance with one or more embodiments of the present disclosure, the compensation circuit includes a second capacitor, a fourth transistor, a fifth transistor, a sixth transistor and a seventh transistor. The second capacitor is coupled between the gate terminal of the driving transistor and the second terminal of the first writing transistor. The fourth transistor has a first terminal coupled to the gate terminal of the driving transistor, a second terminal for receiving a first reference voltage, and a gate terminal for receiving a second scanning signal. The fifth transistor has a first terminal coupled to the second terminal of the first writing transistor, a second terminal for receiving the first reference voltage, and a gate terminal for receiving the second scanning signal. The sixth transistor has a first terminal coupled to the second terminal of the first writing transistor, a second terminal for receiving the first reference voltage, and a gate terminal for receiving a third scanning signal. The seventh transistor has a first terminal coupled to the gate terminal of the driving transistor and a gate terminal for receiving the third scanning signal.

[0017] The present disclosure further provides a driving method of a pixel circuit. The pixel circuit includes a driving transistor, an emission control transistor, a first light-emitting element and a second light-emitting element. The driving method includes: providing a data signal to a gate terminal of the driving transistor; providing an emission control signal to a gate terminal of the emission control transistor, in which the emission control transistor is coupled between a first terminal of the driving transistor and a first system voltage terminal, in which the first light-emitting element is coupled between a second terminal of the driving transistor and a second system voltage terminal to emit light with a first color, in which the second light-emitting element is coupled between the second terminal of the driving transistor and a third system voltage terminal to emit light with a second color different from the first color; and controlling the emission control signal and voltage levels of the second system voltage terminal and the third system voltage terminal, thereby causing the first light-emitting element or the second light-emitting element to emit light. When the first light-emitting element or the second light-emitting element emits light, the voltage levels of the second system voltage terminal and the third system voltage terminal are different.

[0018] In accordance with one or more embodiments of the present disclosure, the driving method further includes: providing a low voltage level to the second system voltage terminal coupled to a cathode of the first light-emitting element and providing a high voltage level to the third system voltage terminal coupled to a cathode of the second light-emitting element, thereby causing the first light-emitting element to emit light and causing the second light-emitting element not to emit light; and providing the high voltage level to the second system voltage terminal and providing the low voltage level to the third system voltage terminal,

thereby causing the first light-emitting element not to emit light and causing the second light-emitting element to emit light.

[0019] In accordance with one or more embodiments of the present disclosure, the driving method further includes: providing a high voltage level to the second system voltage terminal coupled to an anode of the first light-emitting element and providing a low voltage level to the third system voltage terminal coupled to an anode of the second light-emitting element, thereby causing the first light-emitting element to emit light and causing the second light-emitting element not to emit light; and providing the low voltage level to the second system voltage terminal and providing the high voltage level to the third system voltage terminal, thereby causing the first light-emitting element not to emit light and causing the second light-emitting element to emit light.

[0020] In accordance with one or more embodiments of the present disclosure, the pixel circuit further includes a third light-emitting element. The third light-emitting element is coupled between the second terminal of the driving transistor and a fourth system voltage terminal to emit light with a third color different from the first color and the second color. The driving method further includes: controlling the emission control signal and voltage levels of the second system voltage terminal, the third system voltage terminal and the fourth system voltage terminal, thereby causing the first light-emitting element, the second light-emitting element or the third light-emitting element to emit light. During an emission period of the pixel circuit, a voltage level of one of the second system voltage terminal, the third system voltage terminal and the fourth system voltage terminal is

different from voltage levels of the other two of the second system voltage terminal, the third system voltage terminal and the fourth system voltage terminal.

[0021] In accordance with one or more embodiments of the present disclosure, the driving method further includes: providing a low voltage level to the second system voltage terminal coupled to a cathode of the first light-emitting element and providing a high voltage level to the third system voltage terminal coupled to a cathode of the second light-emitting element and providing the high voltage level to the fourth system voltage terminal coupled to a cathode of the third light-emitting element, thereby causing the first light-emitting element to emit light and causing the second light-emitting element and the third light-emitting element not to emit light; providing the low voltage level to the third system voltage terminal and providing the high voltage level to the second system voltage terminal and the fourth system voltage terminal, thereby causing the second light-emitting element to emit light and causing the first light-emitting element and the third light-emitting element not to emit light; and providing the low voltage level to the fourth system voltage terminal and providing the high voltage level to the second system voltage terminal and the third system voltage terminal, thereby causing the third light-emitting element to emit light and causing the first light-emitting element and the second light-emitting element not to emit light.

[0022] In accordance with one or more embodiments of the present disclosure, the driving method further includes: providing a high voltage level to the second system voltage terminal coupled to an anode of the first light-emitting element and providing a low voltage level to the third system voltage terminal coupled to an anode of the second light-emitting element and providing the low voltage level

to the fourth system voltage terminal coupled to an anode of the third light-emitting element, thereby causing the first light-emitting element to emit light and causing the second light-emitting element and the third light-emitting element not to emit light; providing the high voltage level to the third system voltage terminal and providing the low voltage level to the second system voltage terminal and the fourth system voltage terminal, thereby causing the second light-emitting element to emit light and causing the first light-emitting element and the third light-emitting element not to emit light; and providing the high voltage level to the fourth system voltage terminal and providing the low voltage level to the second system voltage terminal and the third system voltage terminal, thereby causing the third light-emitting element to emit light and causing the first light-emitting element and the second light-emitting element not to emit light.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] The invention can be more fully understood by reading the following detailed description of the embodiment, with reference made to the accompanying drawings as follows.

[0024] FIG. 1 is a circuit diagram of a pixel circuit according to a first embodiment of the present disclosure.

[0025] FIG. 2 is a flowchart of a driving method of a pixel circuit according to some embodiments of the present disclosure.

[0026] FIG. 3 is a control timing diagram of the emission period of the pixel circuit according to the first embodiment of the present disclosure.

[0027] FIG. 4A is a schematic diagram of states of components of the pixel circuit during the emission period of the first light-emitting element according to the first embodiment of the present disclosure.

[0028] FIG. 4B is a schematic diagram of states of components of the pixel circuit during the emission period of the second light-emitting element according to the first embodiment of the present disclosure.

[0029] FIG. 4C is a schematic diagram of states of components of the pixel circuit during the emission period of the third light-emitting element according to the first embodiment of the present disclosure.

[0030] FIG. 5 is a circuit diagram of the pixel circuit according to a second embodiment of the present disclosure.

[0031] FIG. 6 is a control timing diagram of the emission period of the pixel circuit according to the second embodiment of the present disclosure.

[0032] FIG. 7A is a schematic diagram of states of components of the pixel circuit during the emission period of the first light-emitting element according to the second embodiment of the present disclosure.

[0033] FIG. 7B is a schematic diagram of states of components of the pixel circuit during the emission period of the second light-emitting element according to the second embodiment of the present disclosure.

[0034] FIG. 7C is a schematic diagram of states of components of the pixel circuit during the emission period of the third light-emitting element according to the second embodiment of the present disclosure.

[0035] FIG. 8 is a circuit diagram of a pixel circuit according to a third embodiment of the present disclosure.

[0036] FIG. 9 is a circuit diagram of a pixel circuit according to a fourth embodiment of the present disclosure.

DETAILED DESCRIPTION

[0037] FIG. 1 is a circuit diagram of a pixel circuit 10 according to a first embodiment of the present disclosure. The pixel circuit 10 includes an emission circuit 12 and a control circuit 14. The emission circuit 12 includes a driving transistor T_D , an emission control transistor T_{EM} , a first transistor T_R , a first light-emitting element L_R , a second transistor T_G , a second light-emitting element L_G , a third transistor T_B and a third light-emitting element L_B .

[0038] The driving transistor T_D has a gate terminal for receiving a data signal Data. The emission control transistor T_{EM} has a gate terminal for receiving an emission control signal EM. The emission control transistor T_{EM} is coupled between a first terminal of the driving transistor T_D and a system voltage terminal VDD (i.e., the system high voltage terminal).

[0039] The first light-emitting element L_R emits the red light. A cathode of the first light-emitting element L_R is coupled to a system voltage terminal VSS_R. An anode of the first light-emitting element L_R is coupled to a second terminal of the driving transistor T_D . The first light-emitting element L_R and the first transistor T_R are coupled in series and coupled between the second terminal of the driving transistor T_D and the system voltage terminal VSS_R. Specifically, the first transistor T_R has a gate terminal for receiving the emission control signal EM,

such that the first transistor T_R drives the first light-emitting element L_R . It is worth mentioning that the positions of the first light-emitting element L_R and the first transistor T_R as shown in FIG. 1 can be interchanged.

[0040] The second light-emitting element L_G emits the green light. A cathode of the second light-emitting element L_G is coupled to a system voltage terminal VSS_G . An anode of the second light-emitting element L_G is coupled to the second terminal of the driving transistor T_D . The second light-emitting element L_G and the second transistor T_G are coupled in series and coupled between the second terminal of the driving transistor T_D and the system voltage terminal VSS_G . Specifically, the second transistor T_G has a gate terminal for receiving the emission control signal EM , such that the second transistor T_G drives the second light-emitting element L_G . It is worth mentioning that the positions of the second light-emitting element L_G and the second transistor T_G as shown in FIG. 1 can be interchanged.

[0041] The third light-emitting element L_B emits the blue light. A cathode of the third light-emitting element L_B is coupled to a system voltage terminal VSS_B . An anode of the third light-emitting element L_B is coupled to the second terminal of the driving transistor T_D . The third light-emitting element L_B and the third transistor T_B are coupled in series and coupled between the second terminal of the driving transistor T_D and the system voltage terminal VSS_B . Specifically, the third transistor T_B has a gate terminal for receiving the emission control signal EM , such that the third transistor T_B drives the third light-emitting element L_B . It is worth mentioning that the positions of the third light-emitting element L_B and the third transistor T_B as shown in FIG. 1 can be interchanged.

[0042] In the first embodiment of the present disclosure, the first light-emitting element L_R , the second light-emitting element L_G and the third light-emitting element L_B are current-driven light-emitting elements, such as light-emitting diodes (LEDs), micro LEDs, organic light-emitting diodes (OLEDs) or sub-millimeter light-emitting diodes (Mini LEDs).

[0043] The control circuit 14 includes a first writing transistor T_{w1} , a second writing transistor T_{w2} and a capacitor C1. A first terminal of the first writing transistor T_{w1} receives the data signal Data. A second terminal of the first writing transistor T_{w1} is coupled to a gate terminal of the driving transistor T_D . A gate terminal of the first writing transistor T_{w1} receives a scanning signal SN. During a writing period of the pixel circuit 10, the first writing transistor T_{w1} is turned on according to the scanning signal SN to transmit the data signal Data to the gate terminal of the driving transistor T_D . Specifically, the control circuit 14 transmits the data signal Data to the gate terminal of the driving transistor T_D . It is worth mentioning that the circuit configuration of the control circuit 14 as shown in FIG. 1 is merely an example, and the present disclosure is not limited thereto, and other known related circuits that transmit the data signal Data to the gate terminal of the driving transistor T_D are also suitable for the control circuit of the present disclosure.

[0044] A first terminal of the second writing transistor T_{w2} receives the initial voltage V_{ini} . A second terminal of the second writing transistor T_{w2} is coupled to the first terminal of the driving transistor T_D . A gate terminal of the second writing transistor T_{w2} receives the scanning signal SN. During the writing period of the pixel circuit 10, the second writing transistor T_{w2} is turned on according to the scanning signal SN to transmit the initial voltage V_{ini} to the first terminal of the

driving transistor T_D . The capacitor $C1$ is coupled between the second terminal of the first writing transistor T_{w1} (i.e., the gate terminal of the driving transistor T_D) and the second terminal of the second writing transistor T_{w2} (i.e., the first terminal of the driving transistor T_D). In other words, the capacitor $C1$ stores the voltage difference between the data signal $Data$ and the initial voltage V_{ini} .

[0045] FIG. 2 is a flowchart of a driving method of a pixel circuit according to some embodiments of the present disclosure. The driving method of the pixel circuit 10 includes Steps S1~S3. In Step S1, during the writing period of the pixel circuit 10, the data signal $Data$ is provided to the gate terminal of the driving transistor T_D . In Step S2, during the an emission period of the pixel circuit 10, the emission control signal EM is provided to the gate terminals of the emission control transistor T_{EM} , the first transistor T_R , the second transistor T_G and the third transistor T_B . In Step S3, during the emission period of the pixel circuit 10, the emission control signal EM , the voltage level of the system voltage terminal VSS_R , the voltage level of the system voltage terminal VSS_G and the voltage level of the system voltage terminal VSS_B are controlled, thereby causing one of the first light-emitting element L_R , the second light-emitting element L_G and the third light-emitting element L_B to emit light.

[0046] FIG. 3 is a control timing diagram of the emission period of the pixel circuit 10 according to the first embodiment of the present disclosure. The emission period of the pixel circuit 10 is divided into an emission period $Frame_R$ of the first light-emitting element L_R , an emission period $Frame_G$ of the second light-emitting element L_G , and an emission period of the third light-emitting element L_B . As shown in FIG. 3, during the emission period of the pixel circuit 10, one of the

system voltage terminal VSS_R, the system voltage terminal VSS_G and the system voltage terminal VSS_B has a low voltage level and the other two of them have high voltage levels.

[0047] FIG. 4A is a schematic diagram of states of components of the pixel circuit 10 during the emission period Frame_R of the first light-emitting element L_R according to the first embodiment of the present disclosure. FIG. 4B is a schematic diagram of states of components of the pixel circuit 10 during the emission period Frame_G of the second light-emitting element L_G according to the first embodiment of the present disclosure. FIG. 4C is a schematic diagram of states of components of the pixel circuit 10 during the emission period Frame_B of the third light-emitting element L_B according to the first embodiment of the present disclosure. It is worth mentioning that during the emission period of the pixel circuit 10, the scanning signal SN is controlled to turn off the first writing transistor T_{w1} and the second writing transistor T_{w2}.

[0048] As shown in FIG. 3 and FIG. 4A, during the emission period Frame_R of the first light-emitting element L_R, the system voltage terminal VSS_G and the system voltage terminal VSS_B are controlled to have high voltage levels, thereby turning off the second light-emitting element L_G and the third light-emitting element L_B (at the same time, the second transistor T_G and the third transistor T_B are also turned off), and at the same time, the system voltage terminal VSS_R is controlled to have a low voltage level and the emission control signal EM is controlled, so that a current path (as shown by the arrow in FIG. 4A) is formed between the system voltage terminal VDD and the system voltage terminal VSS_R through the emission control transistor T_{EM}, the driving transistor T_D, the

first transistor T_R and the first light-emitting element L_R , thereby causing the first light-emitting element L_R to emit light.

[0049] In other words, when the first light-emitting element L_R emits light, the voltage level of the system voltage terminal VSS_R is different from the voltage levels of the system voltage terminal VSS_G and the system voltage terminal VSS_B . In other words, the first light-emitting element L_R is controlled according to the emission control signal EM and the voltage level of the system voltage terminal VSS_R , and the first transistor T_R is controlled according to the emission control signal EM and the voltage level of the system voltage terminal VSS_R . In other words, when the first light-emitting element L_R emits light and the second light-emitting element L_G and the third light-emitting element L_B do not emit light, the system voltage terminal VSS_R has a low voltage level and the system voltage terminal VSS_G and the system voltage terminal VSS_B have high voltage levels. In other words, the driving method of the pixel circuit 10 further includes: providing a low voltage level to the system voltage terminal VSS_R coupled to the cathode of the first light-emitting element L_R and providing high voltage levels to the system voltage terminal VSS_G coupled to the cathode of the second light-emitting element L_G and the system voltage terminal VSS_B coupled to the cathode of the third light-emitting element L_B , such that the first light-emitting element L_R emits light and the second light-emitting element L_G and the third light-emitting element L_B do not emit light. It is worth mentioning that during the emission period $Frame_R$ of the first light-emitting element L_R , the emission control signal EM is a multi-pulse signal, that is, the emission control signal EM is a signal that switches between a low logic level and a high logic level according to a duty cycle, causing the emission control transistor T_{EM} and the first

transistor T_R to switch between the on-state and the off-state according to the emission control signal EM. Accordingly, the first light-emitting element L_R switches between the on-state and the off-state, thereby achieving the effect of multi-pulse light emission (or multi-pulse time-sharing light emission).

[0050] As shown in FIG. 3 and FIG. 4B, during the emission period Frame_G of the second light-emitting element L_G , the system voltage terminal VSS_R and the system voltage terminal VSS_B are controlled to have high voltage levels, thereby turning off the first light-emitting element L_R and the third light-emitting element L_B (at the same time, the first transistor T_R and the third transistor T_B are also turned off), and at the same time, the system voltage terminal VSS_G is controlled to have a low voltage level and the emission control signal EM is controlled, so that a current path (as shown by the arrow in FIG. 4B) is formed between the system voltage terminal VDD and the system voltage terminal VSS_G through the emission control transistor T_{EM} , the driving transistor T_D , the second transistor T_G and the second light-emitting element L_G , thereby causing the second light-emitting element L_G to emit light.

[0051] In other words, when the second light-emitting element L_G emits light, the voltage level of the system voltage terminal VSS_G is different from the voltage levels of the system voltage terminal VSS_R and the system voltage terminal VSS_B. In other words, the second light-emitting element L_G is controlled according to the emission control signal EM and the voltage level of the system voltage terminal VSS_G, and the second transistor T_G is controlled according to the emission control signal EM and the voltage level of the system voltage terminal VSS_G. In other words, when the second light-emitting element L_G emits

light and the first light-emitting element L_R and the third light-emitting element L_B do not emit light, the system voltage terminal VSS_G has a low voltage level and the system voltage terminal VSS_R and the system voltage terminal VSS_B have high voltage levels. In other words, the driving method of the pixel circuit 10 further includes: providing a low voltage level to the system voltage terminal VSS_G coupled to the cathode of the second light-emitting element L_G and providing high voltage levels to the system voltage terminal VSS_R coupled to the cathode of the first light-emitting element L_R and the system voltage terminal VSS_B coupled to the cathode of the third light-emitting element L_B , such that the second light-emitting element L_G emits light and the first light-emitting element L_R and the third light-emitting element L_B do not emit light. It is worth mentioning that during the emission period $Frame_G$ of the second light-emitting element L_G , the emission control signal EM is a multi-pulse signal, that is, the emission control signal EM is a signal that switches between a low logic level and a high logic level according to a duty cycle, causing the emission control transistor T_{EM} and the second transistor T_G to switch between the on-state and the off-state according to the emission control signal EM . Accordingly, the second light-emitting element L_G switches between the on-state and the off-state, thereby achieving the effect of multi-pulse light emission (or multi-pulse time-sharing light emission).

[0052] As shown in FIG. 3 and FIG. 4C, during the emission period $Frame_B$ of the third light-emitting element L_B , the system voltage terminal VSS_R and the system voltage terminal VSS_G are controlled to have high voltage levels, thereby turning off the first light-emitting element L_R and the second light-emitting element L_G (at the same time, the first transistor T_R and the second transistor T_G are also turned off), and at the same time, the system voltage terminal VSS_B is

controlled to have a low voltage level and the emission control signal EM is controlled, so that a current path (as shown by the arrow in FIG. 4C) is formed between the system voltage terminal VDD and the system voltage terminal VSS_B through the emission control transistor T_{EM}, the driving transistor T_D, the third transistor T_B and the third light-emitting element L_B, thereby causing the third light-emitting element L_B to emit light.

[0053] In other words, when the third light-emitting element L_B emits light, the voltage level of the system voltage terminal VSS_B is different from the voltage levels of the system voltage terminal VSS_R and the system voltage terminal VSS_G. In other words, the third light-emitting element L_B is controlled according to the emission control signal EM and the voltage level of the system voltage terminal VSS_B, and the third transistor T_B is controlled according to the emission control signal EM and the voltage level of the system voltage terminal VSS_B. In other words, when the third light-emitting element L_B emits light and the first light-emitting element L_R and the second light-emitting element L_G do not emit light, the system voltage terminal VSS_B has a low voltage level and the system voltage terminal VSS_R and the system voltage terminal VSS_G have high voltage levels. In other words, the driving method of the pixel circuit 10 further includes: providing a low voltage level to the system voltage terminal VSS_B coupled to the cathode of the third light-emitting element L_B and providing high voltage levels to the system voltage terminal VSS_R coupled to the cathode of the first light-emitting element L_R and the system voltage terminal VSS_G coupled to the cathode of the second light-emitting element L_G, such that the third light-emitting element L_B emits light and the first light-emitting element L_R and the second light-emitting element L_G do not emit light. It is worth mentioning that

during the emission period Frame_B of the third light-emitting element L_B, the emission control signal EM is a multi-pulse signal, that is, the emission control signal EM is a signal that switches between a low logic level and a high logic level according to a duty cycle, causing the emission control transistor T_{EM} and the third transistor T_B to switch between the on-state and the off-state according to the emission control signal EM. Accordingly, the third light-emitting element L_B switches between the on-state and the off-state, thereby achieving the effect of multi-pulse light emission (or multi-pulse time-sharing light emission).

[0054] Specifically, as shown in FIG. 3, the emission period of the pixel circuit 10 is divided into the emission period Frame_R of the first light-emitting element L_R, the emission period Frame_G of the second light-emitting element L_G, and the emission period Frame_B of the third light-emitting element L_B. The first light-emitting element L_R, the second light-emitting element L_G and the third light-emitting element L_B respectively emit light during the emission period Frame_R, the emission period Frame_G and the emission period Frame_B, thereby driving the first light-emitting element L_R, the second light-emitting element L_G and the third light-emitting element L_B in a time-sharing manner during the emission period of the pixel circuit 10, so that the pixel circuit 10 emits light with a specific color.

[0055] Please return to FIG. 1, to sum up, the pixel circuit 10 of the first embodiment of the present disclosure allows the first light-emitting element L_R, the second light-emitting element L_G and the third light-emitting element L_B to share the emission control signal EM and the emission control transistor T_{EM}, thereby reducing the number of transistors and the number of the signal lines,

and thus increasing the aperture ratio and light transmittance and further improving the display effect.

[0056] FIG. 5 is a circuit diagram of the pixel circuit 20 according to a second embodiment of the present disclosure. The pixel circuit 20 includes an emission circuit 22 and the control circuit 14. The emission circuit 22 includes the driving transistor T_D , the emission control transistor T_{EM} , the first light-emitting element L_R , the second light-emitting element L_G , and the third light-emitting element L_B . The control circuit 14 of the pixel circuit 20 in FIG. 5 is substantially the same as the control circuit 14 of the pixel circuit 10 in FIG. 1, and therefore the control circuit 14 of the pixel circuit 20 in FIG. 5 is not described again.

[0057] The driving transistor T_D has the gate terminal for receiving the data signal Data. The emission control transistor T_{EM} has the gate terminal for receiving the emission control signal EM. The emission control transistor T_{EM} is coupled between the first terminal of the driving transistor T_D and the system voltage terminal VSS (i.e., the system low voltage terminal).

[0058] The first light-emitting element L_R emits the red light. The anode of the first light-emitting element L_R is coupled to the system voltage terminal VDD_R. The cathode of the first light-emitting element L_R is coupled to the second terminal of the driving transistor T_D .

[0059] The second light-emitting element L_G emits the green light. The anode of the second light-emitting element L_G is coupled to the system voltage terminal VDD_G. The cathode of the second light-emitting element L_G is coupled to the second terminal of the driving transistor T_D .

[0060] The third light-emitting element L_B emits the blue light. The anode of the third light-emitting element L_B is coupled to the system voltage terminal VDD_B . The cathode of the third light-emitting element L_B is coupled to the second terminal of the driving transistor T_D .

[0061] In the second embodiment of the present disclosure, the first light-emitting element L_R , the second light-emitting element L_G and the third light-emitting element L_B are current-driven light-emitting elements, such as light-emitting diodes (LEDs), micro LEDs, OLEDs, or Mini LEDs.

[0062] Please refer to the flow chart of the driving method of the pixel circuit as shown in FIG. 2. The driving method of the pixel circuit 20 includes the following steps. (1) During the writing period of the pixel circuit 20, the data signal Data is provided to the gate terminal of the driving transistor T_D . (2) During the emission period of the pixel circuit 20, the emission control signal EM is provided to the gate terminal of the emission control transistor T_{EM} . (3) During the emission period of the pixel circuit 20, the emission control signal EM and the voltage level of the system voltage terminal VDD_R , the voltage level of the system voltage terminal VDD_G and the voltage level of the system voltage terminal VDD_B are controlled, thereby causing one of the first light-emitting element L_R , the second light-emitting element L_G and the third light-emitting element L_B to emit light.

[0063] FIG. 6 is a control timing diagram of the emission period of the pixel circuit 20 according to the second embodiment of the present disclosure. The emission period of the pixel circuit 20 is divided into the emission period Frame_R of the first light-emitting element L_R , the emission period Frame_G of the second light-emitting element L_G , and the emission period of the third light-emitting element

L_B. As shown in FIG. 6, during the emission period of the pixel circuit 20, one of the system voltage terminal VSS_R, the system voltage terminal VSS_G and the system voltage terminal VSS_B has the high voltage level and the other two of them have low voltage levels.

[0064] FIG. 7A is a schematic diagram of states of components of the pixel circuit 20 during the emission period Frame_R of the first light-emitting element L_R according to the second embodiment of the present disclosure. FIG. 7B is a schematic diagram of states of components of the pixel circuit 20 during the emission period Frame_G of the second light-emitting element L_G according to the second embodiment of the present disclosure. FIG. 7C is a schematic diagram of states of components of the pixel circuit 20 during the emission period Frame_B of the third light-emitting element L_B according to the second embodiment of the present disclosure.

[0065] As shown in FIG. 6 and FIG. 7A, during the emission period Frame_R of the first light-emitting element L_R, the system voltage terminal VDD_G and the system voltage terminal VDD_B are controlled to have low voltage levels, thereby turning off the second light-emitting element L_G and the third light-emitting element L_B, and at the same time, the system voltage terminal VDD_R is controlled to have a high voltage level and the emission control signal EM is controlled, so that a current path (as shown by the arrow in FIG. 7A) is formed between the system voltage terminal VSS and the system voltage terminal VDD_R through the first transistor T_R, the driving transistor T_D and the emission control transistor T_{EM}, thereby causing the first light-emitting element L_R to emit light.

[0066] In other words, when the first light-emitting element L_R emits light, the voltage level of the system voltage terminal VDD_R is different from the voltage levels of the system voltage terminal VDD_G and the system voltage terminal VDD_B . In other words, the first light-emitting element L_R is controlled according to the emission control signal EM and the voltage level of the system voltage terminal VDD_R . In other words, when the first light-emitting element L_R emits light and the second light-emitting element L_G and the third light-emitting element L_B do not emit light, the system voltage terminal VDD_R has a high voltage level and the system voltage terminal VDD_G and the system voltage terminal VDD_B have low voltage levels. In other words, the driving method of the pixel circuit 20 further includes: providing a high voltage level to the system voltage terminal VDD_R coupled to the anode of the first light-emitting element L_R and providing low voltage levels to the system voltage terminal VDD_G coupled to the anode of the second light-emitting element L_G and the system voltage terminal VDD_B coupled to the anode of the third light-emitting element L_B , such that the first light-emitting element L_R emits light and the second light-emitting element L_G and the third light-emitting element L_B do not emit light. It is worth mentioning that during the emission period $Frame_R$ of the first light-emitting element L_R , the emission control signal EM is a multi-pulse signal, that is, the emission control signal EM is a signal that switches between a low logic level and a high logic level according to a duty cycle, causing the emission control transistor T_{EM} to switch between the on-state and the off-state according to the emission control signal EM . Accordingly, the first light-emitting element L_R switches between the on-state and the off-state, thereby achieving the effect of multi-pulse light emission (or multi-pulse time-sharing light emission).

[0067] As shown in FIG. 6 and FIG. 7B, during the emission period Frame_G of the second light-emitting element L_G , the system voltage terminal VDD_R and the system voltage terminal VDD_B are controlled to have low voltage levels, thereby turning off the first light-emitting element L_R and the third light-emitting element L_B , and at the same time, the system voltage terminal VDD_G is controlled to have a high voltage level and the emission control signal EM is controlled, so that a current path (as shown by the arrow in FIG. 7B) is formed between the system voltage terminal VSS and the system voltage terminal VDD_G through the second light-emitting element L_G , the driving transistor T_D and the emission control transistor T_{EM} , thereby causing the second light-emitting element L_G to emit light.

[0068] In other words, when the second light-emitting element L_G emits light, the voltage level of the system voltage terminal VDD_G is different from the voltage levels of the system voltage terminal VDD_R and the system voltage terminal VDD_B. In other words, the second light-emitting element L_G is controlled according to the emission control signal EM and the voltage level of the system voltage terminal VDD_G. In other words, when the second light-emitting element L_G emits light and the first light-emitting element L_R and the third light-emitting element L_B do not emit light, the system voltage terminal VDD_G has a high voltage level and the system voltage terminal VDD_R and the system voltage terminal VDD_B have low voltage levels. In other words, the driving method of the pixel circuit 20 further includes: providing a high voltage level to the system voltage terminal VDD_G coupled to the anode of the second light-emitting element L_G and providing low voltage levels to the system voltage terminal VDD_R coupled to the anode of the first light-emitting element L_R and the system

voltage terminal VDD_B coupled to the anode of the third light-emitting element L_B, such that the second light-emitting element L_G emits light and the first light-emitting element L_R and the third light-emitting element L_B do not emit light. It is worth mentioning that during the emission period Frame_G of the second light-emitting element L_G, the emission control signal EM is a multi-pulse signal, that is, the emission control signal EM is a signal that switches between a low logic level and a high logic level according to a duty cycle, causing the emission control transistor T_{EM} to switch between the on-state and the off-state according to the emission control signal EM. Accordingly, the second light-emitting element L_G switches between the on-state and the off-state, thereby achieving the effect of multi-pulse light emission (or multi-pulse time-sharing light emission).

[0069] As shown in FIG. 6 and FIG. 7C, during the emission period Frame_B of the third light-emitting element L_B, the system voltage terminal VDD_R and the system voltage terminal VDD_G are controlled to have low voltage levels, thereby turning off the first light-emitting element L_R and the second light-emitting element L_G, and at the same time, the system voltage terminal VDD_B is controlled to have a high voltage level and the emission control signal EM is controlled, so that a current path (as shown by the arrow in FIG. 7C) is formed between the system voltage terminal VSS and the system voltage terminal VDD_B through the third light-emitting element L_B, the driving transistor T_D and the emission control transistor T_{EM}, thereby causing the third light-emitting element L_B to emit light.

[0070] In other words, when the third light-emitting element L_B emits light, the voltage level of the system voltage terminal VDD_B is different from the voltage levels of the system voltage terminal VDD_R and the system voltage terminal

VDD_G. In other words, the third light-emitting element L_B is controlled according to the emission control signal EM and the voltage level of the system voltage terminal VDD_B. In other words, when the third light-emitting element L_B emits light and the first light-emitting element L_R and the second light-emitting element L_G do not emit light, the system voltage terminal VDD_B has a high voltage level and the system voltage terminal VDD_R and the system voltage terminal VDD_G have low voltage levels. In other words, the driving method of the pixel circuit 20 further includes: providing a high voltage level to the system voltage terminal VDD_B coupled to the anode of the third light-emitting element L_B and providing low voltage levels to the system voltage terminal VDD_R coupled to the anode of the first light-emitting element L_R and the system voltage terminal VDD_G coupled to the anode of the second light-emitting element L_G , such that the third light-emitting element L_B emits light and the first light-emitting element L_R and the second light-emitting element L_G do not emit light. It is worth mentioning that during the emission period Frame_B of the third light-emitting element L_B , the emission control signal EM is a multi-pulse signal, that is, the emission control signal EM is a signal that switches between a low logic level and a high logic level according to a duty cycle, causing the emission control transistor T_{EM} to switch between the on-state and the off-state according to the emission control signal EM. Accordingly, the third light-emitting element L_B switches between the on-state and the off-state, thereby achieving the effect of multi-pulse light emission (or multi-pulse time-sharing light emission).

[0071] Specifically, as shown in FIG. 6, the emission period of the pixel circuit 20 is divided into the emission period Frame_R of the first light-emitting element L_R , the emission period Frame_G of the second light-emitting element L_G , and the

emission period Frame_B of the third light-emitting element L_B. The first light-emitting element L_R, the second light-emitting element L_G and the third light-emitting element L_B respectively emit light during the emission period Frame_R, the emission period Frame_G and the emission period Frame_B, thereby driving the first light-emitting element L_R, the second light-emitting element L_G and the third light-emitting element L_B in a time-sharing manner during the emission period of the pixel circuit 20, so that the pixel circuit 20 emits light with a specific color.

[0072] Please return to FIG. 5, to sum up, the pixel circuit 20 of the second embodiment of the present disclosure allows the first light-emitting element L_R, the second light-emitting element L_G and the third light-emitting element L_B to share the emission control signal EM and the emission control transistor T_{EM}, thereby reducing the number of transistors and the number of the signal lines, and thus increasing the aperture ratio and light transmittance and further improving the display effect.

[0073] FIG. 8 is a circuit diagram of a pixel circuit 30 according to a third embodiment of the present disclosure. The pixel circuit 30 of FIG. 8 is similar to the pixel circuit 10 of FIG. 1, and the main difference between them is that the pixel circuit 30 of FIG. 8 further includes a compensation circuit 36. The pixel circuit 30 of FIG. 8 includes the emission circuit 12, a control circuit 34 and a compensation circuit 36. The emission circuit 12 of the pixel circuit 30 of FIG. 8 is substantially the same as the emission circuit 12 of the pixel circuit 10 of FIG. 1, and therefore the emission circuit 12 of the pixel circuit 30 is not described again. The control circuit 34 of the pixel circuit 30 of FIG. 8 is similar to the control

circuit 14 of the pixel circuit 10 of FIG. 1. The only difference between them is that the scanning signal SN of the control circuit 14 of the pixel circuit 10 in FIG. 1 is changed to the scanning signal SN+1 in the control circuit 34 of the pixel circuit 30 in FIG. 8. Therefore, the remaining parts of the control circuit 34 that are the same as the remaining parts of the control circuit 14 are not described again. In addition, the flowchart of the driving method and the control timing during the emission period of the pixel circuit 30 in FIG. 8 are similar to those of the pixel circuit 10 in FIG. 1, respectively, and thus are not described again.

[0074] The compensation circuit 36 of the pixel circuit 30 in FIG. 8 is coupled between the gate terminal of the driving transistor T_D and the second terminal of the first writing transistor T_{w1} . Specifically, the compensation circuit 36 compensates the threshold voltage of the driving transistor T_D through the capacitor C1. It is worth mentioning that the circuit configuration of the compensation circuit 36 as shown in FIG. 8 is merely an example, and the present disclosure is not limited thereto, and other known related circuits for compensating the threshold voltage of the driving transistor T_D are also suitable for the compensation circuit of the present disclosure.

[0075] The compensation circuit 36 of the pixel circuit 30 of FIG. 8 includes a capacitor C2, a fourth transistor T4, a fifth transistor T5, a sixth transistor T6 and a seventh transistor T7. The capacitor C2 is coupled between the gate terminal of the driving transistor T_D and the second terminal of the first writing transistor T_{w1} . The first terminal of the fourth transistor T4 is coupled to the gate terminal of the driving transistor T_D , the second terminal of the fourth transistor T4 receives a first reference voltage Vref1, and the gate terminal of the fourth transistor T4

receives a scanning signal SN-1. The first terminal of the fifth transistor T5 is coupled to the second terminal of the first writing transistor T_{w1} , the second terminal of the fifth transistor T5 receives the first reference voltage Vref1, and the gate terminal of the fifth transistor T5 receives the scanning signal. SN-1. The first terminal of the sixth transistor T6 is coupled to the second terminal of the first writing transistor T_{w1} , the second terminal of the sixth transistor T6 receives the first reference voltage Vref1, and the gate terminal of the sixth transistor T6 receives the scanning signal SN. The first terminal of the seventh transistor T7 is coupled to the gate terminal of the driving transistor T_D , and the gate terminal of the seventh transistor T7 receives the scanning signal SN.

[0076] During the voltage compensation period of the pixel circuit 30, the scanning signal SN-1 and the scanning signal SN can be set to remain in an enabled state (for example, at a low voltage level), so that the fourth to seventh transistors T4-T7 and the driving transistor T_D can continue to be turned on, and the scanning signal SN+1 and the emission control signal EM can be set to be in a disabled state (for example, a high voltage level), so that the first writing transistor T_{w1} , the second writing transistor T_{w2} and the emission control transistor T_{EM} can be turning off, and thus the data signal Data continues to be unable to be transmitted to the gate terminal of the driving transistor T_D .

[0077] In such case, the voltage between the opposite terminals of the capacitor C2 can continue to be the first reference voltage Vref1, and the data stored in the capacitor C2 can continue to be reset. In addition, since the emission control transistor T_{EM} is in an off state, the first terminal of the driving transistor T_D cannot receive the high voltage level of the system voltage terminal VDD, so that the

voltage at the first terminal of the driving transistor T_D can be discharged from the high voltage level of the system voltage terminal VDD to the sum of the first reference voltage V_{ref1} and the threshold voltage of the driving transistor T_D .

[0078] Accordingly, the capacitor C1 will store the threshold voltage of the driving transistor T_D . In other words, during the voltage compensation period of the pixel circuit 30, the compensation circuit 36 compensates for the threshold voltage. In addition, since the driving transistor T_D is in an on-state, the voltage at the second terminal of the driving transistor T_D can continue to be maintained at the first reference voltage V_{ref1} , thereby causing the first light-emitting element L_R , the second light-emitting element L_G and the third light-emitting element L_B to be continuously turned off.

[0079] FIG. 9 is a circuit diagram of a pixel circuit 40 according to a fourth embodiment of the present disclosure. The pixel circuit 40 of FIG. 9 is similar to the pixel circuit 20 of FIG. 5, and the main difference between them is that the pixel circuit 40 of FIG. 9 further includes a compensation circuit 36. The pixel circuit 40 of FIG. 9 includes the emission circuit 22, the control circuit 34 and the compensation circuit 36. The emission circuit 22 of the pixel circuit 40 of FIG. 9 is substantially the same as the emission circuit 22 of the pixel circuit 20 of FIG. 5, and therefore the emission circuit 22 of the pixel circuit 40 is not described again. The control circuit 34 of the pixel circuit 40 of FIG. 9 is similar to the control circuit 14 of the pixel circuit 20 of FIG. 5. The only difference between them is that the scanning signal SN of the control circuit 14 of the pixel circuit 20 in FIG. 5 is changed to the scanning signal SN+1 in the control circuit 34 of the pixel circuit 40 in FIG. 9. Therefore, the remaining parts of the control circuit 34 that

are the same as the remaining parts of the control circuit 14 are not described again. In addition, the flowchart of the driving method and the control timing during the emission period of the pixel circuit 40 in FIG. 9 are similar to those of the pixel circuit 20 in FIG. 5, respectively, and thus are not described again. Finally, the compensation circuit 36 of the pixel circuit 40 in FIG. 9 is substantially the same as the compensation circuit 36 of the pixel circuit 30 in FIG. 8, and therefore the compensation circuit 36 of the pixel circuit 40 is not described again.

[0080] In summary, the present disclosure provides a pixel circuit. The first light-emitting element L_R , the second light-emitting element L_G and the third light-emitting element L_B of the pixel circuit share the emission control signal EM and the emission control transistor T_{EM} , thereby reducing the number of transistors and the number of signal lines, and thus increasing the aperture ratio and light transmittance and further improving the display effect.

WHAT IS CLAIMED IS:

1. A pixel circuit, comprising:

a driving transistor having a gate terminal for receiving a data signal;

an emission control transistor coupled between a first terminal of the driving transistor and a first system voltage terminal;

a first light-emitting element coupled between a second terminal of the driving transistor and a second system voltage terminal to emit light with a first color; and

a second light-emitting element coupled between the second terminal of the driving transistor and a third system voltage terminal to emit light with a second color different from the first color;

wherein a gate terminal of the emission control transistor receives an emission control signal;

wherein the first light-emitting element is controlled according to the emission control signal and a voltage level of the second system voltage terminal, wherein the second light-emitting element is controlled according to the emission control signal and a voltage level of the third system voltage terminal; and

wherein when the first light-emitting element or the second light-emitting element emits light, the voltage level of the second system voltage terminal is different from the voltage level of the third system voltage terminal.

2. The pixel circuit of claim 1, further comprising:

a first transistor coupled between the second terminal of the driving transistor and the second system voltage terminal and coupled to the first light-emitting element to drive the first light-emitting element; and

a second transistor coupled between the second terminal of the driving transistor and the third system voltage terminal and coupled to the second light-emitting element to drive the second light-emitting element;

wherein a gate terminal of each of the first transistor and the second transistor receives the emission control signal; and

wherein the first transistor is controlled according to the emission control signal and the voltage level of the second system voltage terminal, wherein the second transistor is controlled according to the emission control signal and the voltage level of the third system voltage terminal.

3. The pixel circuit of claim 1, wherein the first system voltage terminal receives a system high voltage, wherein a cathode of the first light-emitting element is coupled to the second system voltage terminal and an anode of the first light-emitting element is coupled to the second terminal of the driving transistor, wherein a cathode of the second light-emitting element is coupled to the third system voltage terminal and an anode of the second light-emitting element is coupled to the second terminal of the driving transistor.

4. The pixel circuit of claim 3,

wherein when the first light-emitting element emits light and the second light-emitting element does not emit light, the second system voltage terminal has

a low voltage level and the third system voltage terminal has a high voltage level;
and

wherein when the first light-emitting element does not emit light and the second light-emitting element emits light, the second system voltage terminal has the high voltage level and the third system voltage terminal has the low voltage level.

5. The pixel circuit of claim 1, wherein the first system voltage terminal receives a system low voltage, wherein an anode of the first light-emitting element is coupled to the second system voltage terminal and a cathode of the first light-emitting element is coupled to the second terminal of the driving transistor, wherein an anode of the second light-emitting element is coupled to the third system voltage terminal and a cathode of the second light-emitting element is coupled to the second terminal of the driving transistor.

6. The pixel circuit of claim 5,

wherein when the first light-emitting element emits light and the second light-emitting element does not emit light, the second system voltage terminal has a high voltage level and the third system voltage terminal has a low voltage level;
and

wherein when the first light-emitting element does not emit light and the second light-emitting element emits light, the second system voltage terminal has the low voltage level and the third system voltage terminal has the high voltage level.

7. The pixel circuit of claim 1, further comprising:

a third light-emitting element coupled between the second terminal of the driving transistor and a fourth system voltage terminal to emit light with a third color different from the first color and the second color;

wherein the third light-emitting element is controlled according to the emission control signal and a voltage level of the fourth system voltage terminal; and

wherein during an emission period of the pixel circuit, a voltage level of one of the second system voltage terminal, the third system voltage terminal and the fourth system voltage terminal is different from voltage levels of the other two of the second system voltage terminal, the third system voltage terminal and the fourth system voltage terminal.

8. The pixel circuit of claim 7, further comprising:

a third transistor coupled between the second terminal of the driving transistor and the fourth system voltage terminal and coupled to the third light-emitting element to drive the third light-emitting element;

wherein a gate terminal of the third transistor receives the emission control signal; and

wherein the third transistor is controlled according to the emission control signal and the voltage level of the fourth system voltage terminal.

9. The pixel circuit of claim 7, wherein the first system voltage terminal receives a system high voltage, wherein during the emission period of the pixel circuit, one of the second system voltage terminal, the third system voltage

terminal and the fourth system voltage terminal has a low voltage level, and the other two of the second system voltage terminal, the third system voltage terminal and the fourth system voltage terminal have high voltage levels.

10. The pixel circuit of claim 7, wherein the first system voltage terminal receives a system low voltage, wherein during the emission period of the pixel circuit, one of the second system voltage terminal, the third system voltage terminal and the fourth system voltage terminal has a high voltage level, and the other two of the second system voltage terminal, the third system voltage terminal and the fourth system voltage terminal have low voltage levels.

11. The pixel circuit of claim 1, further comprising:

a first writing transistor having a first terminal to receive the data signal, a second terminal coupled to the gate terminal of the driving transistor, and a gate terminal to receive a first scanning signal; and

wherein during a writing period of the pixel circuit, the first writing transistor is turned on according to the first scanning signal, thereby transmitting the data signal to the gate terminal of the driving transistor.

12. The pixel circuit of claim 11, further comprising:

a second writing transistor having a first terminal to receive an initial voltage and a second terminal coupled to the first terminal or the second terminal of the driving transistor; and

a first capacitor coupled between the second terminal of the first writing transistor and the second terminal of the second writing transistor;

wherein during the writing period of the pixel circuit, the second writing transistor transmits the initial voltage to the first terminal or the second terminal of the driving transistor.

13. The pixel circuit of claim 12, further comprising:

a compensation circuit coupled between the gate terminal of the driving transistor and the second terminal of the first writing transistor, wherein the compensation circuit compensates a threshold voltage of the driving transistor through the first capacitor.

14. The pixel circuit of claim 13, wherein the compensation circuit comprises:

a second capacitor coupled between the gate terminal of the driving transistor and the second terminal of the first writing transistor;

a fourth transistor having a first terminal coupled to the gate terminal of the driving transistor, a second terminal for receiving a first reference voltage, and a gate terminal for receiving a second scanning signal;

a fifth transistor having a first terminal coupled to the second terminal of the first writing transistor, a second terminal for receiving the first reference voltage, and a gate terminal for receiving the second scanning signal;

a sixth transistor having a first terminal coupled to the second terminal of the first writing transistor, a second terminal for receiving the first reference voltage, and a gate terminal for receiving a third scanning signal; and

a seventh transistor having a first terminal coupled to the gate terminal of the driving transistor and a gate terminal for receiving the third scanning signal.

15. A driving method of a pixel circuit, wherein the pixel circuit comprises a driving transistor, an emission control transistor, a first light-emitting element and a second light-emitting element, wherein the driving method comprises:

providing a data signal to a gate terminal of the driving transistor;

providing an emission control signal to a gate terminal of the emission control transistor, wherein the emission control transistor is coupled between a first terminal of the driving transistor and a first system voltage terminal, wherein the first light-emitting element is coupled between a second terminal of the driving transistor and a second system voltage terminal to emit light with a first color, wherein the second light-emitting element is coupled between the second terminal of the driving transistor and a third system voltage terminal to emit light with a second color different from the first color; and

controlling the emission control signal and voltage levels of the second system voltage terminal and the third system voltage terminal, thereby causing the first light-emitting element or the second light-emitting element to emit light;

wherein when the first light-emitting element or the second light-emitting element emits light, the voltage levels of the second system voltage terminal and the third system voltage terminal are different.

16. The driving method of claim 15, further comprising:

providing a low voltage level to the second system voltage terminal coupled to a cathode of the first light-emitting element and providing a high voltage level to the third system voltage terminal coupled to a cathode of the

second light-emitting element, thereby causing the first light-emitting element to emit light and causing the second light-emitting element not to emit light; and

providing the high voltage level to the second system voltage terminal and providing the low voltage level to the third system voltage terminal, thereby causing the first light-emitting element not to emit light and causing the second light-emitting element to emit light.

17. The driving method of claim 15, further comprising:

providing a high voltage level to the second system voltage terminal coupled to an anode of the first light-emitting element and providing a low voltage level to the third system voltage terminal coupled to an anode of the second light-emitting element, thereby causing the first light-emitting element to emit light and causing the second light-emitting element not to emit light; and

providing the low voltage level to the second system voltage terminal and providing the high voltage level to the third system voltage terminal, thereby causing the first light-emitting element not to emit light and causing the second light-emitting element to emit light.

18. The driving method of claim 15, wherein the pixel circuit further comprises a third light-emitting element coupled between the second terminal of the driving transistor and a fourth system voltage terminal to emit light with a third color different from the first color and the second color, wherein the driving method further comprises:

controlling the emission control signal and voltage levels of the second system voltage terminal, the third system voltage terminal and the fourth system

voltage terminal, thereby causing the first light-emitting element, the second light-emitting element or the third light-emitting element to emit light;

wherein during an emission period of the pixel circuit, a voltage level of one of the second system voltage terminal, the third system voltage terminal and the fourth system voltage terminal is different from voltage levels of the other two of the second system voltage terminal, the third system voltage terminal and the fourth system voltage terminal.

19. The driving method of claim 18, further comprising:

providing a low voltage level to the second system voltage terminal coupled to a cathode of the first light-emitting element and providing a high voltage level to the third system voltage terminal coupled to a cathode of the second light-emitting element and providing the high voltage level to the fourth system voltage terminal coupled to a cathode of the third light-emitting element, thereby causing the first light-emitting element to emit light and causing the second light-emitting element and the third light-emitting element not to emit light;

providing the low voltage level to the third system voltage terminal and providing the high voltage level to the second system voltage terminal and the fourth system voltage terminal, thereby causing the second light-emitting element to emit light and causing the first light-emitting element and the third light-emitting element not to emit light; and

providing the low voltage level to the fourth system voltage terminal and providing the high voltage level to the second system voltage terminal and the third system voltage terminal, thereby causing the third light-emitting element to

emit light and causing the first light-emitting element and the second light-emitting element not to emit light.

20. The driving method of claim 18, further comprising:

providing a high voltage level to the second system voltage terminal coupled to an anode of the first light-emitting element and providing a low voltage level to the third system voltage terminal coupled to an anode of the second light-emitting element and providing the low voltage level to the fourth system voltage terminal coupled to an anode of the third light-emitting element, thereby causing the first light-emitting element to emit light and causing the second light-emitting element and the third light-emitting element not to emit light;

providing the high voltage level to the third system voltage terminal and providing the low voltage level to the second system voltage terminal and the fourth system voltage terminal, thereby causing the second light-emitting element to emit light and causing the first light-emitting element and the third light-emitting element not to emit light; and

providing the high voltage level to the fourth system voltage terminal and providing the low voltage level to the second system voltage terminal and the third system voltage terminal, thereby causing the third light-emitting element to emit light and causing the first light-emitting element and the second light-emitting element not to emit light.