FIG. 1

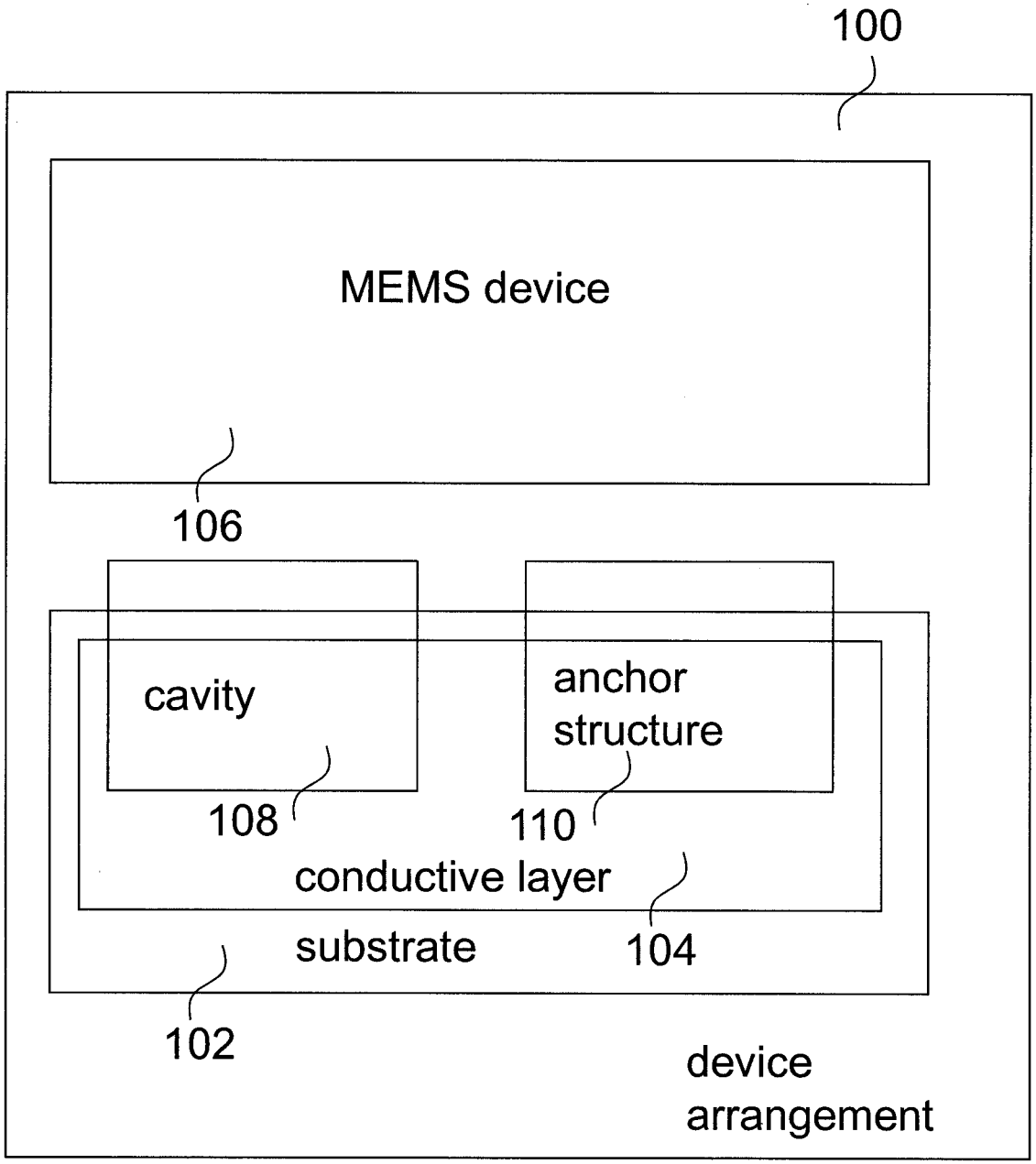

100
MEMS device
106
cavity
anchor
structure
108
110
conductive layer
substrate
104
102
device
arrangement

FIG. 2A

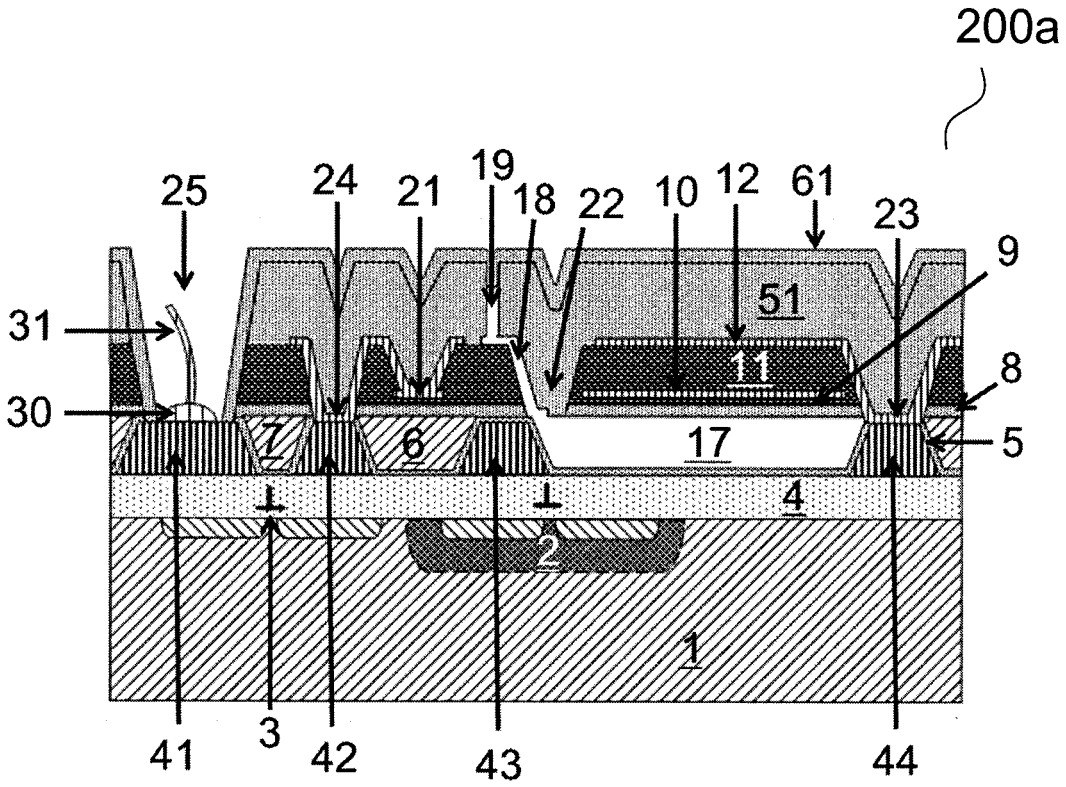

200a
25
24
21
19
18
22
10
12
61
23
9
31
51
11
8
30
7
6
17
5
4
2
1
41
3
42
43
44

FIG. 2B

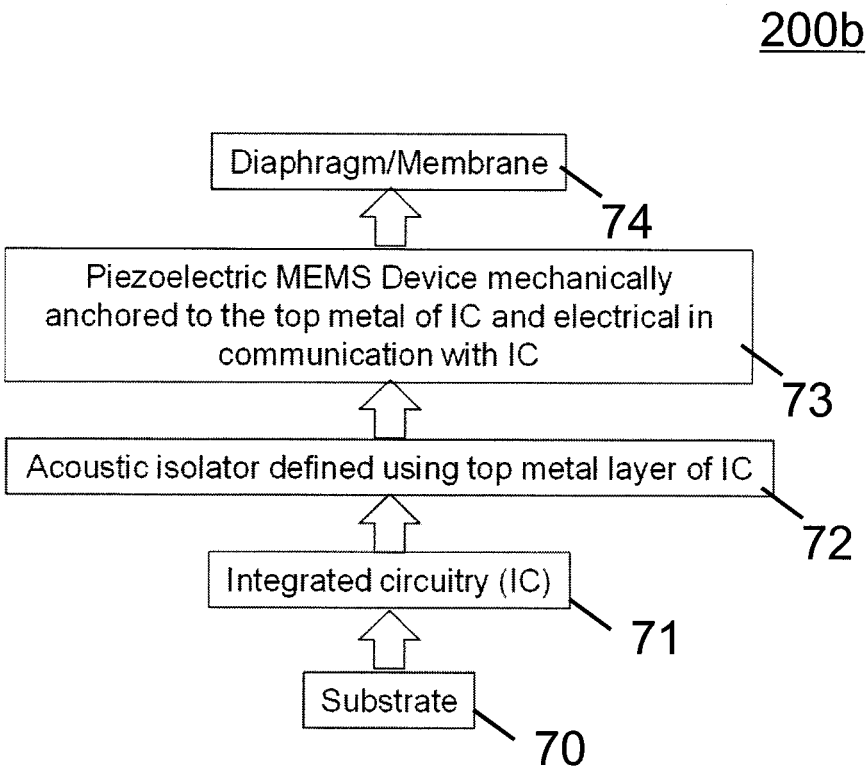

200b
Diaphragm/Membrane
74
Piezoelectric MEMS Device mechanically anchored to the top metal of IC and electrical in communication with IC
73
Acoustic isolator defined using top metal layer of IC
72
Integrated circuitry (IC)
71
Substrate
70

FIG. 2C

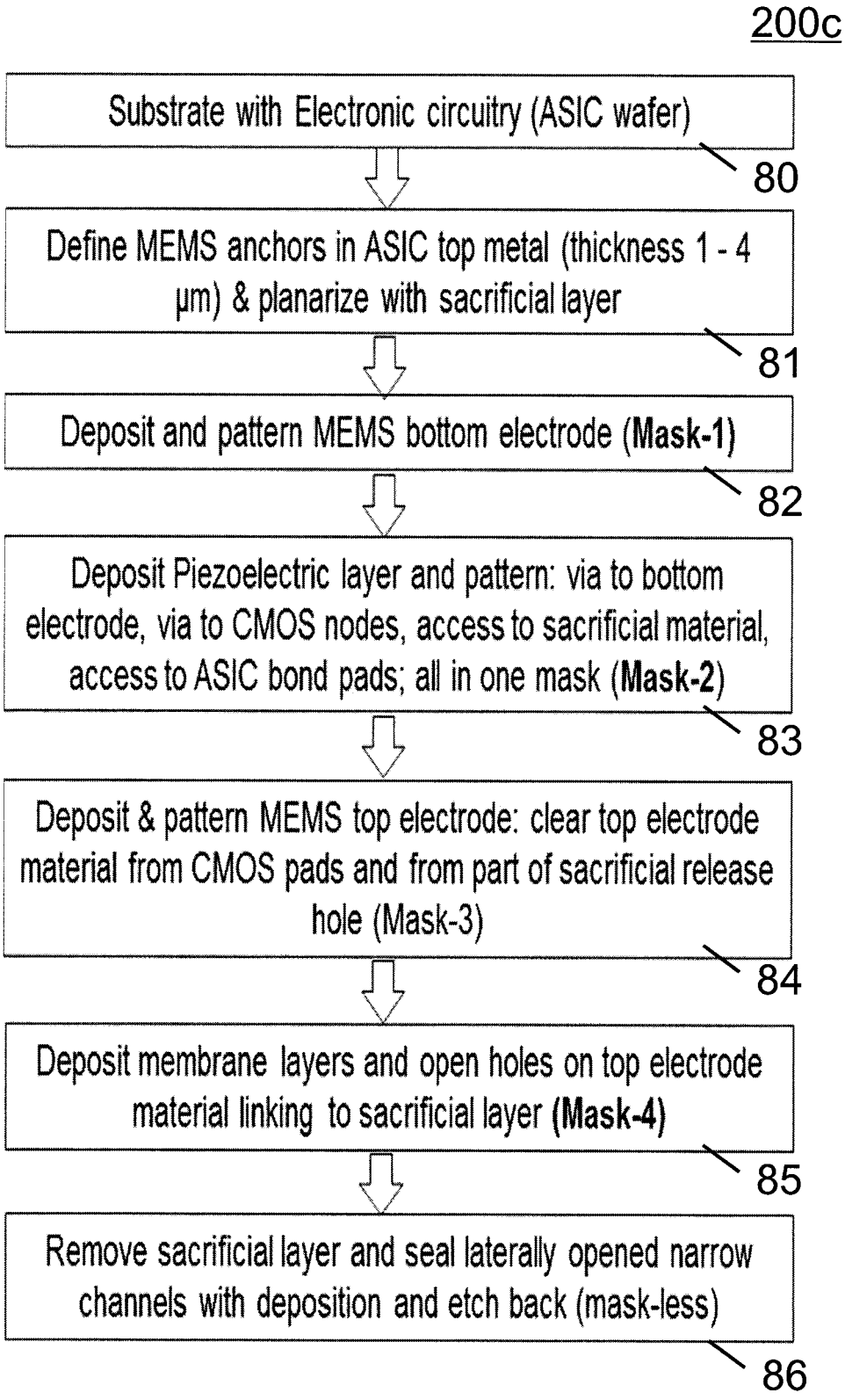

200c
Substrate with Electronic circuitry (ASIC wafer)
80
Define MEMS anchors in ASIC top metal (thickness 1 - 4 µm) & planarize with sacrificial layer
81
Deposit and pattern MEMS bottom electrode (Mask-1)
82
Deposit Piezoelectric layer and pattern: via to bottom electrode, via to CMOS nodes, access to sacrificial material, access to ASIC bond pads; all in one mask (Mask-2)
83
Deposit & pattern MEMS top electrode: clear top electrode material from CMOS pads and from part of sacrificial release hole (Mask-3)
84
Deposit membrane layers and open holes on top electrode material linking to sacrificial layer (Mask-4)
85
Remove sacrificial layer and seal laterally opened narrow channels with deposition and etch back (mask-less)
86

FIG. 3A

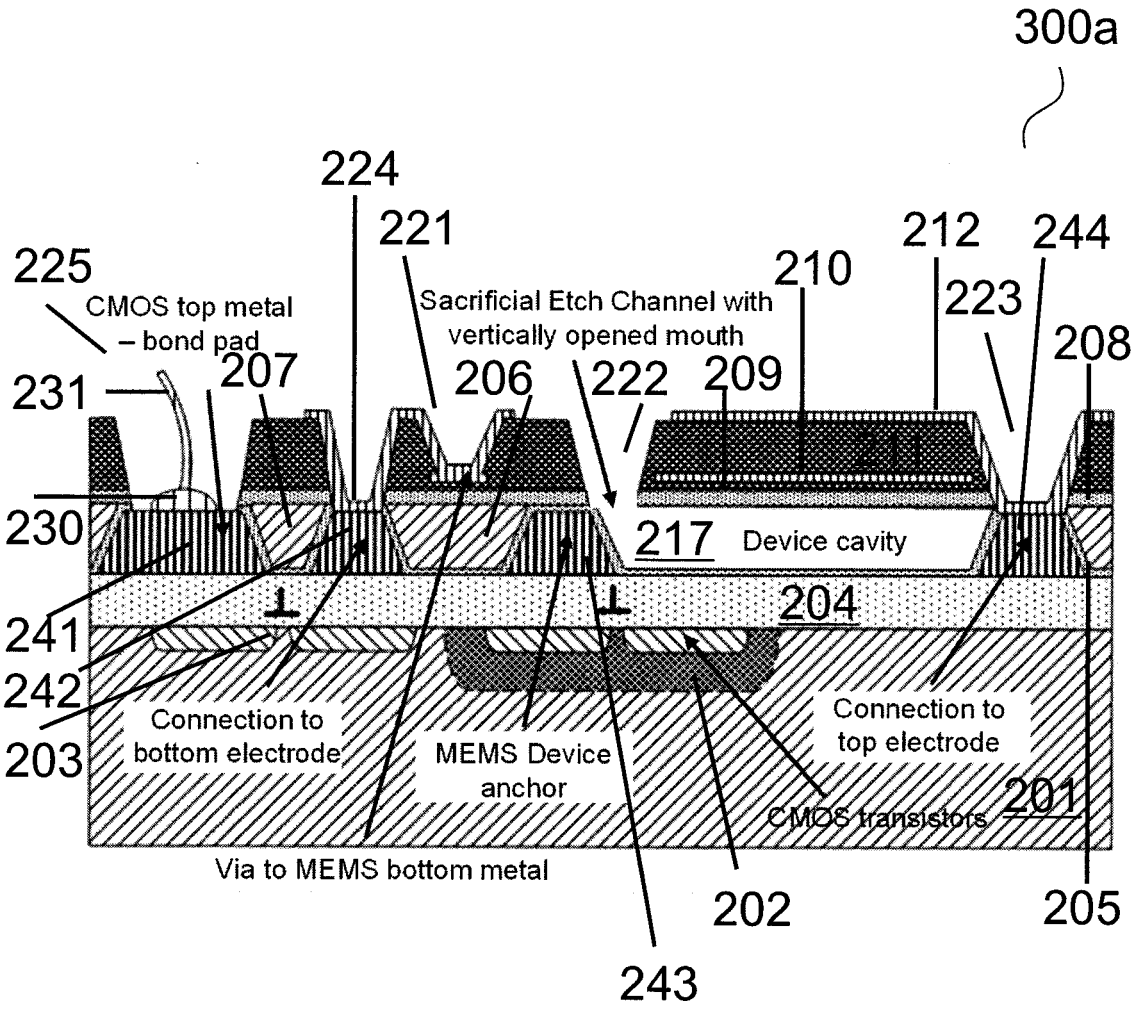

300a
224
221
225
CMOS top metal
– bond pad
Sacrificial Etch Channel with
vertically opened mouth
210
212
244
223
208
231
207
206
222
209
211
230
217
Device cavity
204
241
242
203
Connection to
bottom electrode
MEMS Device
anchor
Connection to
top electrode
CMOS transistors
201
Via to MEMS bottom metal
202
205
243

FIG. 3B

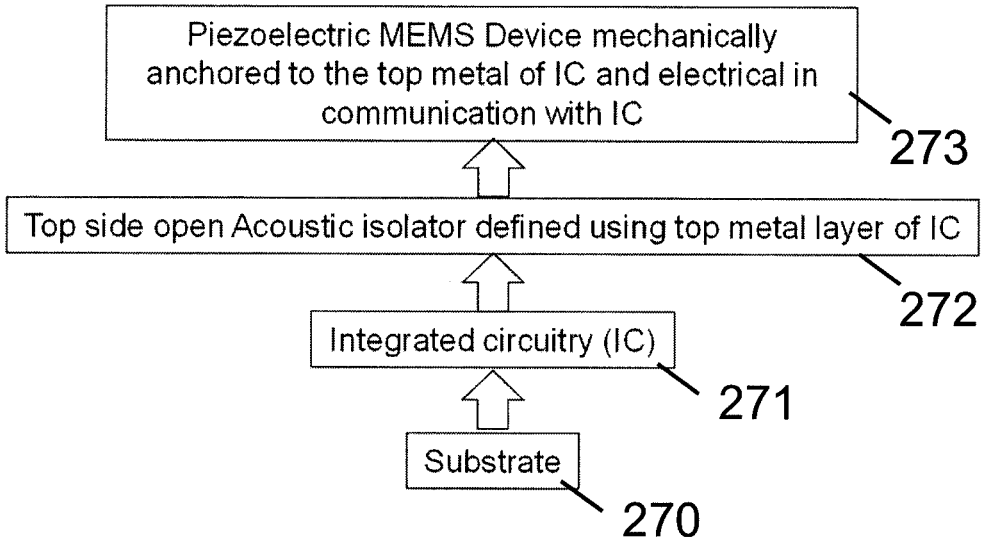

Piezoelectric MEMS Device mechanically anchored to the top metal of IC and electrical in communication with IC
273
Top side open Acoustic isolator defined using top metal layer of IC
272
Integrated circuitry (IC)
271
Substrate
270

FIG. 4

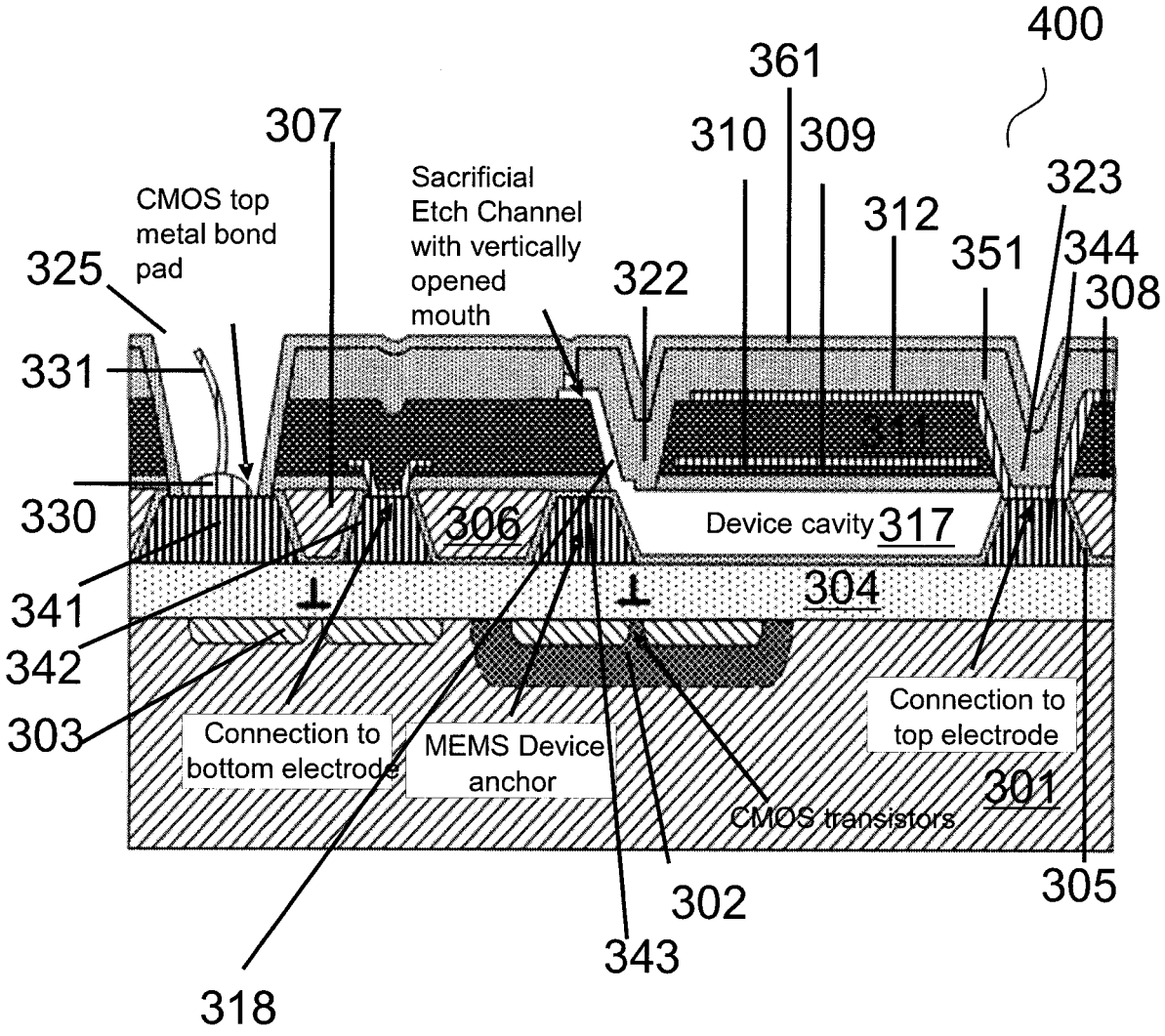

400
361
307
310
309
323
CMOS top metal bond pad
Sacrificial Etch Channel with vertically opened mouth
312
351
344
325
322
308
331
330
306
Device cavity 317
304
341
342
303
Connection to bottom electrode
MEMS Device anchor
Connection to top electrode
CMOS transistors
301
302
305
343
318

FIG. 5

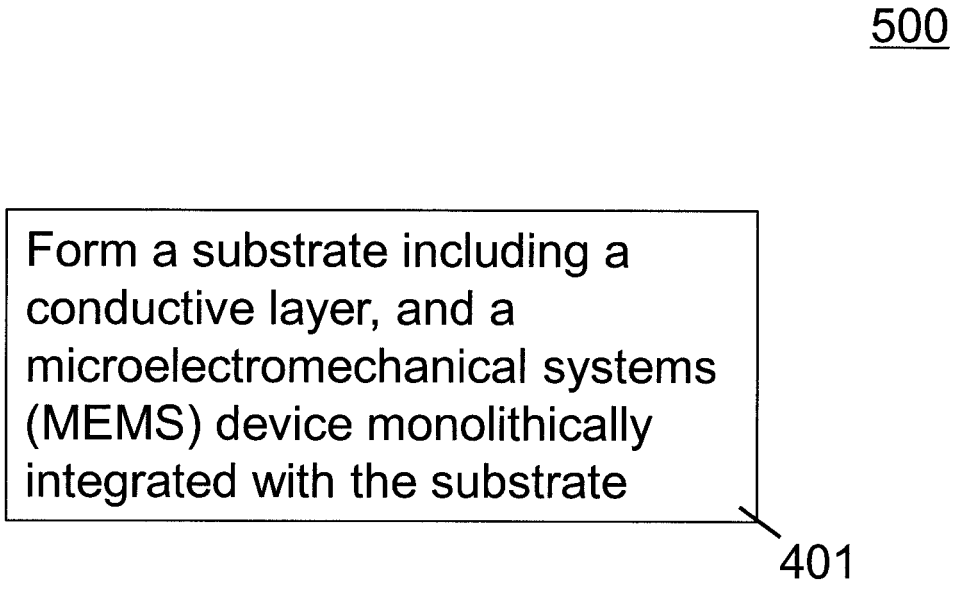

500
Form a substrate including a conductive layer, and a microelectromechanical systems (MEMS) device monolithically integrated with the substrate
401

FIG. 6A

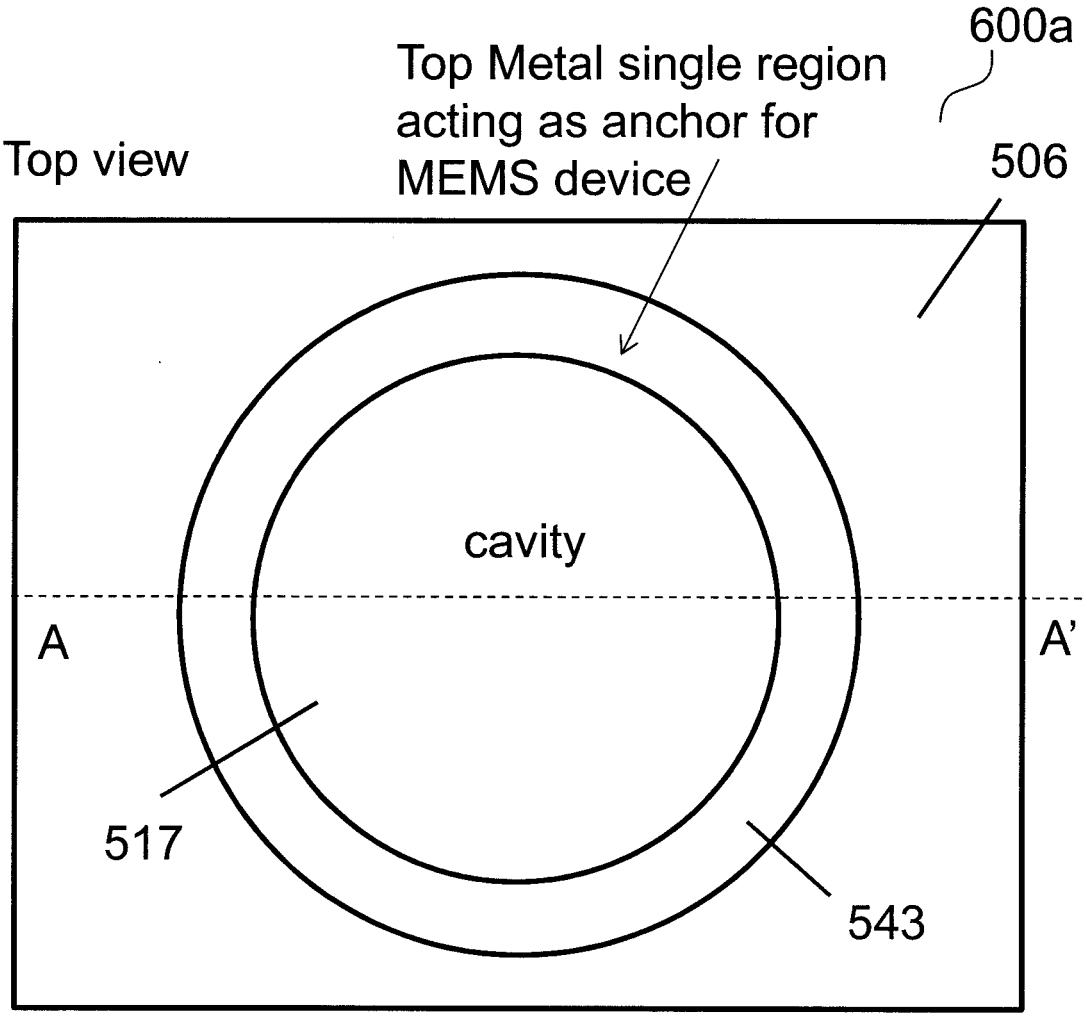
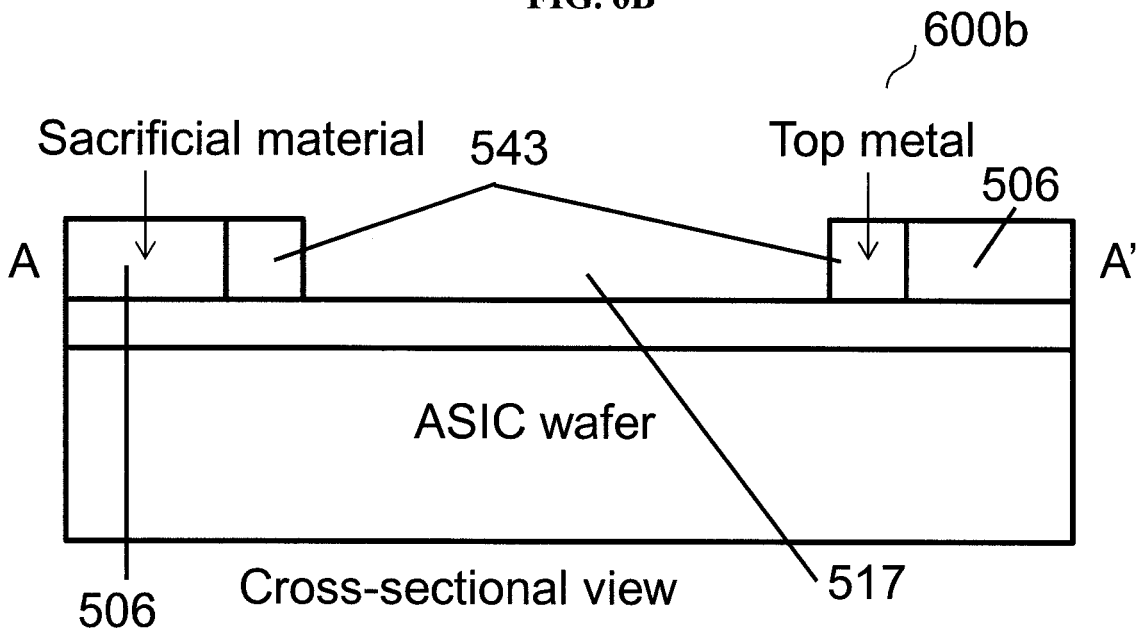

600a
Top Metal single region acting as anchor for MEMS device
Top view
506
cavity
A
A'
517
543

FIG. 6B


600b
Sacrificial material
543
Top metal
506
A
A'
ASIC wafer
506
Cross-sectional view
517