

1 **METHOD AND APPARATUS FOR OPERATING A MICROPROCESSOR
 IN SYNCHRONISM WITH A VIDEO SIGNAL**

 This invention relates to a method and apparatus
for locking the timing of a microprocessor to a video
5 signal and, in particular, to a method and apparatus for
aligning the timing of a microprocessor with the
synchronizing pulses of a video signal to establish a
reference with respect to a video frame.

 It is frequently desirable to align the timing
10 of a microprocessor (or microcomputer) with the timing of
a video frame in a television receiver. When the
microprocessor timing is so aligned, the microprocessor
can establish a reference with respect to a video frame,
and can predict in advance the occurrence of synchronous
15 events in the video signal. The microprocessor is then
able to gate the video signal at appropriate times for
specified signal processing functions. For instance, by
knowing a reference of the video signal, lines can be
counted and gated at the time of occurrence of, for instance
20 the VIR signal on line nineteen, or teletext information
on lines fourteen and fifteenth. By sampling the video
signal at precisely known times it is also possible to
extract synchronous information, such as the burst signal
or a signal used for ghost detection. The extracted
25 information can then be processed by the microprocessor
or other signal processing circuits.

 In accordance with the principles of the present
invention, a microprocessor is herein described which is responsive
to a clock signal which is phase locked to a synchronizing
30 signal component of a composite video signal. The clock
signal is developed by a phase-locked loop and is in phase
synchronism with a horizontal line rate signal. The clock
signal frequency is desirably chosen to be an integer
multiple of the horizontal line frequency and enables the
35 microprocessor to execute an integral number of
instructions in the time interval of one horizontal line.
By counting instructions, the microprocessor can count
whole and fractional line intervals and predict the
occurrence of any synchronously occurring event within a
video line interval.

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Once the microprocessor is clocked to execute instructions in synchronism with the horizontal line rate signal, it is desirable to cause the instructions to be
5 executed in phase alignment with the start of each horizontal line of the video signal. Alignment of the

execution of instructions with the horizontal rate signals is accomplished by executing sampling instructions. These
10 instructions sample the composite sync signals to detect the presence of sync pulses. When a sample fails to detect a sync pulse, a clock pulse is deleted at the microprocessor clock input during a video field. In this way, the phase of the sampling instructions is shifted by
15 one clock cycle each field relative to the sync signals until the sampling instructions are brought into a known phase relationship with the sampled sync signals.

Once the microprocessor is executing instructions in both phase and frequency synchronism with
20 a known location in each horizontal line interval, it is desirable to identify one or more specific lines to provide a reference in each television signal frame. This is done

by sampling each line of the composite sync signal at
25 half-line intervals until a half-line rate (equalizing) pulse is detected. A sequence of half-time rate pulses is then counted to identify the last broad vertical synchronizing pulse of the second (even) field, which establishes a reference which identifies different frames
30 and fields of the video signal. From this reference, the microprocessor can count horizontal rate pulses to identify any specific line or line portion of the video signal.

In the drawings:

FIGURE 1 illustrates in block diagram form,
35 apparatus constructed in accordance with the principles of the present invention for locking the timing of a microprocessor to a video signal;

FIGURES 2, 3 and 4 show waveforms illustrating the method of the present invention for aligning the timing of the microprocessor of FIGURE 1 with each line of a video signal;

FIGURE 5 shows waveforms illustrating a method of providing a video frame reference for the microprocessor of FIGURE 1;

FIGURE 6, (which is on the same sheet as FIGURE 1) shows apparatus constructed in accordance with the principles of the present invention for sampling a VIR signal to control the I.F. passband response of a television receiver; and

FIGURE 7 shows waveforms depicting the operation of the apparatus of FIGURE 6.

Referring to FIGURE 1, apparatus is shown for synchronizing the operation of microprocessor 30 to a video signal in accordance with the present invention. A source of video signals 10, such as a television video detector, produces video signals which are applied to the inputs of a gate 16 and a conventional synchronization signal separator circuit 12. The sync separator 12 produces vertical (V), horizontal (H) and composite (C) (comprising horizontal, vertical and equalizing components) sync signals at respective outputs. The vertical and horizontal sync signals are applied to a conventional television deflection system 14. The deflection system provides horizontal blanking signals at an output, which may, for instance, be derived from the yoke of the kinescope in the usual manner. The horizontal blanking signals and the composite sync signals respectively are applied to data inputs IN_1 and IN_2 of the microprocessor 30. The microprocessor 30 operates in a manner to be described in accordance with instructions stored in a program memory. The horizontal blanking signals are also applied to an input of a phase detector 22, the output of which is coupled by a filter 24 to the control input of a voltage controlled oscillator 26. The output of the voltage controlled

1 oscillator 26 is coupled to a divider 28, and to the
CLOCK input of the microprocessor 30 by way of a switch 32.
5 The output of the divider 28 is coupled to a second input
of the phase detector 22. The phase detector 22, the
filter 24, the voltage controlled oscillator 26 and the
divider 28 are coupled in a phase-locked loop
configuration 20, and operate to produce a clock signal for
10 the microprocessor which is in a substantially constant
phase relationship with the horizontal blanking signal.

The microprocessor 30 has a SKIP CONTROL output
line coupled to the switch 32. Pulses produced by the
microprocessor 30 on this line act to open the normally
15 closed switch 32. The microprocessor also has an output
coupled to the gate 16 to control the conductivity of the
gate. The gate 16 has an output coupled to a signal
utilization circuit 18.

The operation of the arrangement of FIGURE 1
20 may be understood with reference to the following example,
taken in conjunction with the illustrative waveforms of
FIGURES 2-5. For purposes of this example, it is assumed
that the microprocessor used is a model number 8748,
manufactured by Intel and other companies. The voltage
controlled oscillator 26 is assumed to have a nominal
25 operating frequency of 5.66435 MHz, and the divider 28
divides this clock frequency by 360 in the phase-locked
loop 20. The model 8748 microprocessor 30 executes one
instruction cycle every fifteen clock cycles, as shown by
reference to FIGURES 4b and 4c. The model 8748
30 microprocessor is capable of sampling the signals at its
data inputs IN_1 and IN_2 by executing a two-cycle sampling
instruction 110, 112, as shown by FIGURE 4c. The sampling
instruction samples the signal level at a selected input at
a time indicated by the sampling arrow 111 of FIGURE 4c
35 with reference to the microprocessor clock waveform of
FIGURE 4b. At the selected clock frequency of 5.66435 MHz,
the 8748 microprocessor will execute 24 single-cycle
instructions during the time interval of one horizontal line.

When the system of FIGURE 1 is activated, the phase-locked loop derived clock will enable the microprocessor 30 to execute an integral number of single-cycle instructions in one television horizontal line interval. For an NTSC color line interval of 63.555 microseconds, twenty-four instructions of 2.648 microsecond duration will be executed every line interval in this example. If a black-and-white or non-standard signal line interval of different duration is received, the phase-lock loop 20 will adjust the clock frequency to continue the execution of an integer number of instructions each line interval. However, the instructions will be executed in a phase relationship with respect to the beginning of each line which is random at initiation. The microprocessor will then sample the composite sync signal and perform the clock skipping technique of the present invention in order to align the phase of the instruction cycles with the video signal. A reference to each horizontal line is thereby established.

The clock skipping technique overcomes the inherent limitation of the microprocessor of only being able to accurately sample the video signal at sampling instruction intervals which are widely separated in time with respect to the duration of the signals being sampled. In the 8748 microprocessor, for instance, input signals can be sampled only as often as once every 5.3 microseconds, which is twice the instruction cycle time of 2.648 microseconds. Depending upon the phase relationship of the sampling times and the composite sync signal, it is possible for a 2.4 microsecond equalizing pulse to occur between two sampling times. By using the method of the present invention, this limitation can be overcome and the instruction cycles will be quickly aligned in a known phase relationship with the composite sync signal.

When the system of FIGURE 1 is activated, the microprocessor begins to execute a sequence of two-cycle

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sampling instructions to sample the composite sync signal at data input IN_2 . The composite sync signal contains horizontal, equalizing, and vertical sync pulses which, in the NTSC system, have pulse durations of approximately 5, 2.4 and 27 microseconds, respectively. Since the sampling times occur every 5.3 microseconds, only the vertical sync pulses will be sampled by two or more consecutive sampling instructions; the horizontal sync and equalizing pulses are too short to be sampled by two consecutive sampling instructions. When the microprocessor has detected a pulse by detecting a "high" condition by two consecutive sampling instructions for instance, it will execute the next sampling instruction at a time delayed from the first of the two by one-half line interval. Consecutive sampling instructions will again be executed to identify the next vertical sync pulse in the same manner. This sampling technique will continue until the microprocessor has identified the six consecutive vertical sync pulses of the vertical retrace interval. If six vertical sync pulses are not identified, which could occur, for instance, if the sampling sequence begins with the second or subsequent vertical sync pulse, the microprocessor will continue to sample the composite sync signal every 5.3 microseconds until the vertical sync pulse sequence is encountered during the next vertical retrace interval. Once the sequence of six vertical sync pulses has been identified by this technique, the first of the two consecutive instructions which samples the last vertical sync pulse becomes a time reference for the microprocessor which is near the beginning of a half-line interval of the composite sync signal. From this time reference, the microprocessor can sample at half-line intervals to attempt to identify the equalizing pulses of the composite sync signal.

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With the microprocessor sampling instruction timing referenced as described above, the microprocessor will now begin to sample the composite sync signal at

1 half-line intervals, as shown in FIGURES 2b and 2c.
FIGURE 2b shows a horizontal sync pulse 44 followed at
half-line intervals by equalizing pulses 46 and 48, a
pattern which occurs at each transition from an even field
5 to an odd field. FIGURE 2c shows instruction cycles of
the microprocessor drawn in the same time scale as the
composite sync waveform of FIGURE 2b. Sampling times 50,
52 and 54 are represented by arrows, and occur during the
first, thirteenth and first instruction cycles in successive
10 horizontal lines, respectively. The samples are thus
taken one-half line apart in time. In this example, the
horizontal sync pulse 44 will be detected at sampling time
50 but the phase relationship of the microprocessor sampling
instructions and the composite sync waveform of FIGURE 2b
15 results in the inability of the microprocessor to detect
equalizing pulses 46 and 48. The illustrated phase
relationship also causes subsequent equalizing pulses to be
missed by the sampling instructions. The microprocessor
will respond to these undetected pulses by producing a
20 CLOCK SKIP pulse 108 on the SKIP CONTROL line during the
vertical retrace interval, as shown in FIGURE 3c. The
CLOCK SKIP pulse 108 opens switch 32 for one cycle of the
microprocessor clock, as illustrated by the missing clock
cycle after clock cycle 15 in FIGURE 3b. Since each
25 instruction cycle requires fifteen clock pulses, the missed
clock cycle will extend the time of instruction cycle 100
of FIGURE 3a by one clock interval. Instruction cycle 100
will effectively last for sixteen clock cycles, and the
following instruction cycle 102 will begin, as shown, at
30 106 instead of the normal time 104. Thus, instruction cycle
102 and all subsequent instruction cycles are delayed, or
shifted in phase by one clock cycle relative to the
composite sync signal. The microprocessor will now sample
the composite sync waveform with this new phase relationship
35 between the sampling instructions and the composite sync
signal. If the microprocessor again fails to sample the

1 equalizing pulses, a clock cycle will be skipped and the
phase of the sampling instructions will move later in time
relative to the composite sync signal, as shown by
5 sampling times 60, 62 and 64 of FIGURE 2d, all of which are
seen to be shifted in time relative to corresponding
sampling times 50, 52 and 54 of FIGURE 2c.

The microprocessor continues to sample the
composite sync signal and to skip clock cycles in this
10 manner until the sampling time which is concurrent with
the horizontal sync pulse 44 approaches the falling edge
of the pulse, as shown by sampling time 70 of FIGURE 2e.
Subsequent clock cycle skips will cause corresponding
15 sampling instructions to miss the horizontal sync pulse
44. However, these phase shifts will cause the preceding
sampling instruction, shown as sampling time 80, to sample
the horizontal sync pulse 44 in the vicinity of its leading
edge. When this happens, the microprocessor's instruction
reference will increment by two to establish the instruction
20 cycle containing sampling time 80 to be the first
instruction cycle of the line, instead of the twenty-third
of the previous line. After a few more clock cycle skips,
this sampling time will have shifted in phase relative to
the composite sync signal to a time position 90, as shown
25 in FIGURE 2f. In this phase relationship, half-line sample
92 is now in a time position to detect equalizing pulse 46,
and the next sampling time 94 will detect equalizing pulse
48. The microprocessor sampling instructions are now
aligned in phase with the composite sync signal of
30 FIGURE 2b so that all sync pulses will be sampled. In
practice, a fine adjustment of the phase relationship is
performed so that the equalizing pulses are continuously
sampled at their mid-points. It has been found that this
clock skip and phase shift technique will quickly align
35 the sampling times with composite sync signal. Experiments
have shown that analysis of no more than thirty fields is

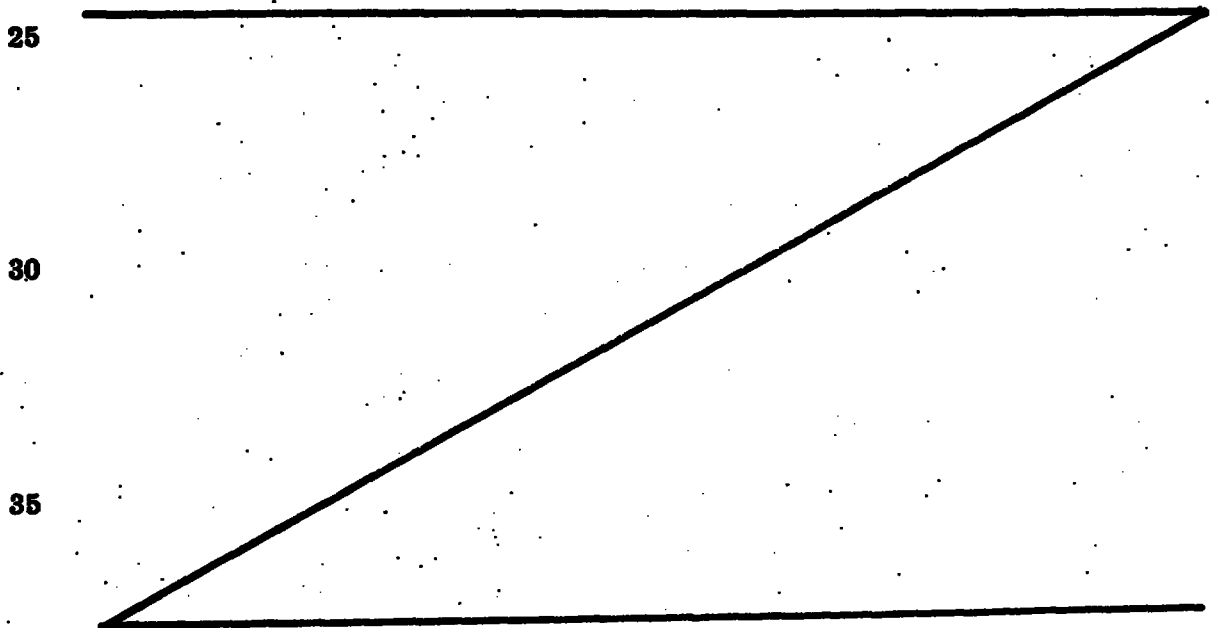
necessary to arrive at the desired alignment from any initial phase condition.

5 The clock skipping technique is advantageously used with microprocessors such as the model 8748 which are designed to easily execute this function. It may be seen from FIGURE 3 that the effect of the clock skip in this example is to lengthen the time required to execute an
10 instruction from 2.648 microseconds to 2.825 microseconds. The phase relationship of subsequent 2.648 microsecond instructions is thereby shifted relative to the incoming sync signals. The same phase shift can be accomplished in software without the clock skip by selectively
15 executing an instruction which has an execution time longer than the nominal 2.648 microsecond instructions. For instance, if the microprocessor is capable of executing another type of instruction in 16, 17, 18, etc. clock cycles, one of these instructions could be executed to
20 provide a phase shift of the timing of the 2.648 microsecond instructions relative to the sync signals. This permits implementation of the principles of the present invention using a microprocessor which does not include the clock skipping feature.

25 When the sampling instructions have been properly aligned in phase with the composite sync signals, any desired portion of a line may be sampled by sampling during the appropriate instruction cycle or cycles. Lines may be counted by counting the horizontal blanking pulses 40 and
30 42 of FIGURE 2a, which are applied to data input IN_1 of the microprocessor 30. However, in order to sample a specific numbered line, such as line nineteen of each field (the VIR line), it is necessary to establish a reference in the video fields. This may be done by sampling the
35 composite sync signal at half-line intervals, as illustrated by the waveforms of FIGURE 5.

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FIGURE 5a shows the composite sync signal waveform at the beginning of an odd (first) field. This waveform is sampled at the sampling times shown in FIGURE 5b. The horizontal sync pulse 120 is the last horizontal sync pulse of the preceding even-numbered field, and is followed by an equalizing pulse 122, one line interval later. The next pulse which is detected is equalizing pulse 124, occurring one-half line interval after pulse 122. Since only a half-line interval has passed between these two signals, the sample time of pulse 124 is counted as "one". Half-line samples are now counted until a count of "twelve" is reached six lines later, at which time equalizing pulse 126 following the vertical sync pulse interval is being sampled. The composite sync waveform is now sampled for a number of consecutive instructions, as indicated by sample times 12' and 12". The narrow width of equalizing pulse 126 allows this pulse to be sampled only by the first sampling time 12, and samples 12' and 12" will find the composite sync waveform to be in a "low" state. The microprocessor now knows that it has identified line seven of an odd video field.



This result may be checked at the start of the following even field, shown in FIGURE 5c. The odd (first) field ends with horizontal sync pulses 130 and 132. Sync pulse 132 is followed one-half line later by an equalizing pulse 134. As in the previous field, the half-line occurrence of two pulses sets the sample counter of the microprocessor to a "one". Half-line samples are now counted until a count of "twelve" is again attained. At the count of twelve, the microprocessor will now be sampling the last broad vertical pulse of the even field. Subsequent consecutive samples 12' and 12" will also detect the broad vertical pulses 136, identifying this pulse 136 as a part of line six of an even field. The microprocessor now has a reference in the video signal, and can identify odd and even fields, as well as specific lines in each field by counting the horizontal blanking pulses at input IN_1 . The microprocessor can gate any specific line to the utilization circuit 18 merely by counting an appropriate number of horizontal blanking pulses and opening gate 16 at the appropriate count. Furthermore, the microprocessor can sample at any specific time of a particular line by executing one or more skips of cycles of the clock signal. These clock skips effectively shift the phase of the sampling instructions into alignment with the time of the line which is to be sampled. The microprocessor can count the clock skips so as to continue to maintain the reference of the sampling times with respect to the video signal.

The arrangement of FIGURE 1 may be configured as shown in FIGURE 6 to sample a VIR signal. The VIR signal samples may then be used, for instance, to control the I.F. passband of the television receiver, as described in United States Patent application serial number 258,928, entitled "I.F. RESPONSE CONTROL SYSTEM FOR A TELEVISION RECEIVER", filed April 30, 1981. In the system there described, the chrominance reference bar and the luminance

1 reference level of the VIR signal are detected and compared
to develop a control signal which is used to peak the I.F.
passband in the vicinity of the picture or chrominance
5 carrier frequency. The basic elements of this system as
shown in FIGURE 6, in which a conventional television
receiver system, including an antenna 152, a tuner 150, a
mixer 154, I.F. signal processing circuitry 158, and
video signal processing circuitry 160 are shown connected
10 in the usual manner. Disposed between the mixer 154 and the
I.F. signal processing circuitry 158 is a tuned I.F. peaking
circuit 156 which may be constructed as shown in the
above-mentioned U.S. application. The detected video signal
at the output of the I.F. signal processing circuitry 158
15 is applied to: a filter 162; a first input of a multiplexer
166; and line lock circuitry 176. The line lock circuitry
176 includes elements 12, 14, 20 and 32 of the arrangement
of FIGURE 1, and is coupled to microprocessor 30 as shown
in that FIGURE. The multiplexer 166 is controlled by
20 signals applied to control lines 172 and 174 by the
microprocessor 30. The output of the filter 162 is coupled
to the input of a detector 164, the output of which is
coupled to a second input of the multiplexer 166.
The output of the multiplexer 166 is coupled to the
25 microprocessor 30 by way of an analog-to-digital converter
168. The microprocessor develops a digital output signal,
which is coupled to the inputs of a digital-to-analog
converter 170, the output of which is coupled to the
30 control input of the tuned I.F. peaking circuit 156.

In operation, the microprocessor timing is aligned
with the composite sync signal of the video signal as
illustrated in FIGURES 2-5. The microprocessor 30 will
count the lines of the video signal to locate line nineteen,
35 which may contain a VIR signal. A typical VIR signal is
shown in FIGURE 7a. Following the conventional horizontal
sync pulse and burst signal, the VIR signal includes a 24
microsecond chrominance reference bar 180, followed by a

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twelve microsecond luminance reference level 182. During
line nineteen, the microprocessor instructions are aligned
with the VIR signal as illustratively shown in FIGURE 7a.
5 During instruction cycle six, the microprocessor 30 will
initiate a chrominance sampling interval pulse on control
line 172, shown as pulse 184 in FIGURE 7b. The
microprocessor terminates pulse 184 during instruction cycle
13. During sampling interval pulse 184, the detected
10 chrominance reference bar level at the output of detector
164 is routed to the A/D converter 168 from the first
input of multiplexer 166. The detected signal level is
converted to a digital signal and stored by the
microprocessor 30.

15 During instruction cycle 15 of line nineteen,
a luminance sampling interval pulse 186 is initiated by
the microprocessor on control line 174. The microprocessor
terminates pulse 186 during instruction cycle 19. Sampling
interval pulse 186 controls the multiplexer to route the
20 luminance reference level from the second input of
multiplexer 166 to the A/D converter 168. The luminance
reference level is digitized and stored by the
microprocessor 30.

25 The microprocessor 30 can now compute a control
signal value for the tuned I.F. peaking circuit 156. The
two stored signals may be analyzed for validity and noise
contamination and a control signal will be calculated in
accordance with the ratio of the two signals. The digital
control signal value is applied to the D/A converter 170,
30 where it is converted to an analog signal and applied to
the tuned I.F. peaking circuit 156. Control of the I.F.
passband of the television receiver will then proceed as
described in the above-mentioned U.S. application serial
number 258,928.
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CLAIMS

1 1. In a television receiver, including a source
of video signals including synchronizing signal components
and means responsive to said synchronizing signal components for producing
a clock signal which is substantially aligned in phase with said
synchronizing signals and has a frequency which is substantially an integer
5 multiple of said synchronizing signal frequency;

apparatus comprising:

a microprocessor having a clock input for receiving
said clock signal and a sampling input terminal, wherein
said clock signal enables said microprocessor to execute
10 instructions at a rate dependent upon the frequency of said
clock signal, and wherein the execution of said instructions
are synchronized with said synchronizing signal components;
and

means for coupling a signal synchronously related to
15 said video signals to said sampling input of said
microprocessor;

wherein said microprocessor samples said synchronously
related signal at times related to the execution of said
instructions.

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2. In a television receiver, including a source of
video signals including synchronizing signal components,
and a synchronizing signal separator circuit responsive to
said video signals for producing separated synchronizing
25 signals of a given frequency; and

means having an input coupled to receive said
synchronizing signals and an output for producing
a clock signal which is substantially aligned in phase with
said synchronizing signals and has a frequency which is
30 substantially an integer multiple of said synchronizing signal
frequency; apparatus comprising:

a microprocessor having a clock input for receiving a clock
signal, said clock signal enabling said microprocessor to execute
instructions at a rate dependent upon the frequency of said clock signal; and

35 means for selectively coupling said output of said
clock signal producing means to said clock input of said
microprocessor in response to a control signal from said
microprocessor whereby, by appropriate skipping of clock



1 pulses, to synchronize execution of said instructions with
said synchronizing signals.

3. The arrangement of Claim 2 wherein;

5 said microprocessor has a data input coupled to
receive said synchronizing signals, and a data output,
said microprocessor being capable of executing an instruction
cycle in a given number of uniform clock signal cycles, being
programmed to execute an integral number of instruction
10 cycles during a horizontal line interval in response to
said clock signal; and

a signal utilization circuit coupled to said data
output of said microprocessor.

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4. The arrangement of Claim 3, wherein ones of
said instruction cycles cause the execution of sampling
25 instructions for sampling the level of said synchronizing
signals at said data input of said microprocessor at
predetermined times; said selective coupling means comprises
a controlled switch; and said microprocessor control signal
is coupled to said controlled switch for opening said
30 switch in response to said control signal generated by said
microprocessor in accordance with said sampled levels of said
synchronizing signals, whereby subsequent sampling
instructions are executed in a known phase relationship
with said synchronizing signals.

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1 5. A method for aligning the timing of a
microprocessor to a video signal, comprising the steps of:

5 a) producing a synchronizing signal containing
horizontal line rate components in response to said video
signal;

 b) producing a clock signal in response to
said synchronizing signal which exhibits a frequency which
is a multiple of the frequency of said synchronizing signal and which is in
substantial phase alignment therewith;

10 c) applying said clock signal to said
microprocessor; and

 d) programming said microprocessor to execute
an integral number of instruction cycles during an integral
number of periods of said synchronizing signal in response
15 to said clock signal.

 e) sampling said synchronizing signal at a
horizontal line rate to detect said horizontal line
rate components and, if a component is not detected,

20 f) preventing the application of a cycle of said
clock signal to said microprocessor; and

 g) repeating steps e) and f) until said
horizontal line rate components are continuously detected
at said horizontal line rate.

25 6. The method of Claim 7, wherein step a)
comprises the step of:

 a) producing a synchronizing signal containing
horizontal sync pulses and equalizing pulses in response
to said video signal; and step e) comprises the step of:

30 e) sampling said synchronizing signal at
half-line intervals to detect the presence of said
equalizing pulses.

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1 7. The method of Claim 6 wherein step a) comprises:

5 a) producing a composite sync signal in response to said video signal; and further comprising steps of:

 h) sampling said composite sync signal at half-line intervals until pulses are detected by two consecutive samples, then

10 i) sampling said composite sync signal, after a period of eleven half-line intervals, for n consecutive sampling instructions, where n is greater than one and less than or equal to the duration of a vertical sync pulse divided by the execution time of a sampling instruction; and

15 j) where a synchronizing signal pulse is detected by the nth sample, identifying that sample as the last broad vertical pulse of an even-numbered video field, and, where a synchronizing signal pulse is not detected by the nth sample;

20 k) identifying the first of said n samples as the first equalizing pulse following the vertical synchronizing pulse interval of an odd-numbered video field.

25 8. Method or apparatus arranged for operating a microprocessor in a television receiver or other video signal processing apparatus, substantially as hereinbefore described with reference to Figure 1 and Figure 2,3,4 or 5 or to Figures 6 and 7, of the
30 accompanying drawings.

