9703064-7
TPOS's copy

REPLACED SHEETS SG

☐ Description : paged ..... to paged .....
☑ Claim(s) : paged 8 to paged 10
☐ Drawing(s) : paged ..... to paged .....
☐ Abstract : paged ..... to paged .....



# SHARED SEGMENTED COMPUTER MEMORY

This invention relates to sharing computer memory.

In personal computers, display of information is typically handled by a dedicated video controller with an associated dedicated video memory. One portion of the dedicated video memory has a frame buffer which stores data corresponding to the pixels to be displayed on a computer monitor. Other portions of video memory can include motion video buffers, buffers for discrete icons (such as cursors, or "pop-ups" displaying system functions like battery life, and the like), and other buffers.

The frame buffer is typically organized in a standard 256K by 16 bit memory architecture, written by a particular width video memory interface. For example, a 32 bit wide video memory interface can access a one megabyte frame buffer, while a 64 bit interface can accommodate a two megabyte frame buffer. The amount of memory required for a given frame buffer, though, is determined by the resolution and dimensions of a given display. For example, a 1024 by 768 pixel display with 16 bit color resolution can require a 1.5 megabyte frame buffer. To accommodate that display, a 2 megabyte dedicated video memory might be required.

Computer manufacturers and users face the choice of paying increased costs to have more dedicated memory to handle higher-resolution displays, or accept lower resolution displays. This choice is becoming more important as manufacturers are integrating the video controller and its dedicated video memory all on the same semiconductor die, because memory size becomes fixed during manufacture.

Unified memory architectures provide an approach for flexible video memory. Such architectures typically share the entire memory subsystem between the video controller and

the system memory controller. Typically, the system memory controller is the master arbiter, while the video controller is a "slave". The system memory controller passes control of the entire memory array to the video controller as needed, which then returns control to the system memory controller for usual memory accesses during program operation. Giving control of the entire memory array to the video controller periodically prevents system memory accesses.

In general, in one aspect, the invention features a method for sharing memory between a video controller and a system memory controller including segmenting system memory to include a video memory segment controlled by the video controller, and allowing the system memory controller to access the video memory segment upon a memory request from the system memory controller.

Embodiments of the invention may include the following features. The segmenting can include providing, in system memory, a system memory segment controlled by the system memory controller, and the system memory segment can be made not accessible by the video memory controller. Memory address and data information provided by the system memory controller can be held for the video memory segment. The held memory address and data information can be released when the system memory controller is allowed to access the video memory segment, and this release can be made by the video controller. The system memory controller, after the accessing, can return control of the video memory segment to the video memory controller. Accessing the video memory segment can include writing and reading data to and from the video memory segment. A second video memory segment can be

provided in system memory not accessible by the system memory controller.

In general, in another aspect, the invention features apparatus for a shared video memory including a video controller, a system memory controller, and a video memory segment in system memory controlled by the video controller, and temporarily accessible by the system memory controller.

Embodiments of the invention may include the following features. An address isolation buffer and a data isolation buffer can be used for address and data information provided by the system memory controller for the video memory segment.

In general, in another aspect, the invention features a computer including a microprocessor, a system memory coupled to the microprocessor, a video controller coupled to the system memory, a system memory controller coupled to the system memory, and a video memory segment in the system memory controlled by the video controller and temporarily accessible by the system memory controller.

Embodiments of the invention may include the following features. The computer system can include a display coupled to the video controller.

The advantages of the invention may include one or more of the following. One linear array of system memory can be segmented into system memory segments and video memory segments. The video controller can master arbitrate accesses to the video memory segment independently of accesses of system memory by the system memory controller. No dedicated video memory is required in addition to the system memory. Video memory can be added and subtracted as required, allowing a number of differing video resolutions

and pixel color depths to be handled without purchasing and installing additional dedicated video memory.

Other features and advantages of the invention will become apparent from the following description and from the claims.

Fig. 1 is a schematic diagram of a computer.

Fig. 2 is a schematic diagram of a unified memory architecture.

Fig. 3 is a schematic diagram of a segmented unified memory architecture.

Fig. 4 is a diagram of the segmentation of a memory array.

Referring to Fig. 1, a computer 10 implementing a segmented unified memory architecture comprises CPU 12, system memory 14, system memory controller 15, and a keyboard (or other data entry device) 16, all coupled via bus 18 (which can be one or more separate bus lines, e.g., microprocessor bus, ISA bus, and PCI bus), and a video controller 20 (also coupled to bus 18) which provides information for display 24.

Referring to Fig. 2, a prior art unified memory architecture scheme allows both video controller 20 and system memory controller 15 to provide memory addresses (ADDR) and data to system memory array 14. System memory controller 15 acts as master arbiter and, upon requests from video controller 20 (carried by control signals 17), may grant video memory accesses. Whichever controller is currently accessing the memory resource has responsibility for handling refreshes for the entire memory array. During video memory accesses, system memory controller cannot access any of the memory array 14. Accordingly, programs

have to wait until the video memory access has been finished, before resuming program and data memory accesses.

Referring to Fig. 3, a segmented unified memory architecture segments the system memory (usually provided as a number of linear DRAM memories linked together) into at least two sections: a first section is DRAM bank X (14x) and below, comprising the bulk of normal system memory for program and data information. The second section is from DRAM Bank X+1 (14x+1) and above, comprising the bulk of video memory. Video controller 20 is the master arbiter of video memory segment 14x+1, while system memory controller 15 controls system memory segment 14x.

Upon a request from system memory controller 15 (on request line REQ 26), video controller 20 grants system memory controller 15 access to video memory segment 14x+1 (upon grant line GNT 28). System memory controller 15 places memory addresses onto address line 32, held by memory address isolation buffer 33. Upon granting the memory request, video controller 20 releases the address(es) held by isolation buffer 33 via buffer control line 36, onto video memory segment address line 34. If system memory controller 15 is writing data, such data is placed onto data line 44, and held by data isolation buffer 45, which is also controlled by video controller 20 (via control line 46). (If reading data, the data from video memory segment 14x+1 is received on data line 44). Isolation buffers 33 and 45 need not store any data; they can function as gates to electrically isolate address and data lines from the shared memory segment 14x+1 until access has been granted.

Once the memory access has been granted, the held data is placed on video memory segment data line 38. System memory controller, via RAS/CAS line 30 (row address strobe/column address strobe), then controls the memory

accesses of video memory segment 14x+1. Once completed, system memory controller 15 returns control of video memory segment 14x+1 to video controller 20, which operates upon its memory segment (providing addresses and data) without isolation buffers 33 and 45. System memory controller 15 directly controls system memory segment 14x via address line 40, memory data line 44 and RAS/CAS control line 42.

The segmented unified memory architecture allows both video and system memory to share at least a portion of the same linear array of system memory, and eliminates the need for dedicated video DRAM memory on a video controller card or the like. Furthermore, the segmented unified memory architecture responds to the fact that video memory accesses tend to be very predictable, with regular cycles for refreshing display 24. Video controller 20 can access its full video memory segment 14x+1 without interfering with accesses by system memory controller 15 of system memory segment 14x. Some video and system memory accesses can proceed simultaneously, engendering no performance problems. Furthermore, portions of the video memory segment can be given over to access by system memory controller 15, providing flexible sharing of the single memory resource. As one example, referring to Fig. 4, 8 megabytes of system memory 50 can be initially segmented as 1.5 Mbytes of a video buffer 54, and 6.5 Mbytes of system RAM 52. A 0.5 MByte border section 56 can be shared and given back to system memory 52 as required. Thus, a variety of display resolutions and pixel color depths can be implemented easily, without adding more expensive video memory, and without substantial system operation degradation.

The invention can be combined with subject matter set forth in a commonly-owned application entitled "INCREMENTAL VIDEO BUFFER", filed on the same day as this application, and incorporated by reference.

Other embodiments are within the scope of the claims. For example, control signals for address and data isolation buffers 33 and 45 may come from system memory controller 15 instead of video controller 20. All or only a portion of video memory segment 14x+1 may be shared between video and system memory. Segments of system memory segment 14x (or the like) can be shared with video controller 20, with system memory controller 15 remaining the master arbiter for the segment(s).

What is claimed is:

This Sheet Has Been Replaced



1. A method for sharing memory between a video controller and a system memory controller comprising:

segmenting system memory to include a video memory segment controlled by the video controller; and

allowing the system memory controller to access the video memory segment upon a memory request from the system memory controller.

2. The method of claim 1 in which the segmenting further includes providing, in system memory, a system memory segment controlled by the system memory controller.

3. The method of claim 2 wherein the system memory segment is not accessible by the video memory controller.

4. The method of claim 1 further comprising holding memory address information provided by the system memory controller for the video memory segment.

5. The method of claim 4 further comprising releasing the held memory address information when the system memory controller is allowed to access the video memory segment.

6. The method of claim 5 wherein the video controller releases the held memory address information.

7. The method of claim 1 further comprising holding memory data information provided by the system memory controller for the video memory segment.

8. The method of claim 7 further comprising releasing the held memory data information when the system memory controller is allowed to access the video memory segment.

9. The method of claim 8 wherein the video controller releases the held memory data information.

10. The method of claim 1 wherein the system memory controller, after the accessing, returns control of the video memory segment to the video memory controller.

* C L M S *

This Sheet Has Been Replaced



11. The method of claim 1 wherein the accessing the video memory segment comprises writing data to the video memory segment.

12. The method of claim 1 wherein the accessing the video memory segment comprises reading data from the video memory segment.

13. The method of claim 1 further comprising providing a second video memory segment in system memory that is not accessible by the system memory controller.

14. Apparatus for shared memory comprising:

a video controller;

a system memory controller; and

a video memory segment in system memory controlled by the video controller, and temporarily accessible by the system memory controller.

15. The apparatus of claim 14 further comprising a system memory segment in system memory controlled by the system memory controller.

16. The apparatus of claim 15 wherein the system memory segment is not accessible by the video memory controller.

17. The apparatus of claim 14 further comprising a an address isolation buffer for address information provided by the system memory controller for the video memory segment.

18. The apparatus of claim 14 further comprising a data isolation buffer for data information provided by the system memory controller for the video memory segment.

19. The apparatus of claim 14 further comprising a second video memory segment in system memory that is not accessible by the system memory controller.

* C L M S *

This Sheet Has Been Replaced



20. A computer system comprising:

a microprocessor;

a system memory coupled to the microprocessor;

a video controller coupled to the system memory;

a system memory controller coupled to the system memory; and

a video memory segment in the system memory controlled by the video controller, and temporarily accessible by the system memory controller.

21. The computer of claim 20 further comprising a display coupled to the video controller.

22. The computer of claim 20 further comprising a system memory segment in the system memory controlled by the system memory controller.

23. The computer of claim 22 wherein the system memory segment is not accessible by the video memory controller.

24. The computer of claim 20 further comprising a an address isolation buffer for address information provided by the system memory controller for the video memory segment.

25. The computer of claim 20 further comprising a data isolation buffer for data information provided by the system memory controller for the video memory segment.

26. The computer of claim 20 further comprising a second video memory segment in the system memory that is not accessible by the system memory controller.

* C L M S *