

"VIDEO SIGNAL SYNCHRONIZING CIRCUIT ARRANGEMENT"

The invention relates to a synchronizing circuit arrangement for deriving and processing a synchronizing signal contained in an incoming composite video signal, the synchronizing signal comprising line and field synchronizing pulses whose amplitude
5 extends between a reference and a peak level, the circuit arrangement comprising a peak level detector coupled to a signal input of the circuit arrangement for detecting the peak level of the synchronizing pulses, a comparator stage having a first input terminal coupled to the signal input, a second input terminal for receiving a
10 clipping level which corresponds to a given level located between the peak and the reference levels, and an output terminal for applying the resulting composite synchronizing signal to a line synchronizing circuit for generating a locally generated signal of line frequency, the circuit arrangement further comprising a
15 synchronization detector for detecting the occurrence of the synchronized state between the incoming line synchronizing pulses and locally generated pulses where the phase difference is less than a predetermined value and for changing the mode of operation of portions of the circuit arrangement.

20 Such a circuit arrangement is disclosed in United States Patent Specification 4 185 299. In this prior art circuit arrangement the composite television synchronizing signal is derived by means of a clipping level which is located between the peak and the
25 reference levels, the reference level being approximately the black level of the video information of the video signal. For a negative-going synchronizing pulse the clipping level is located above the detected peak level at a distance which is approximately equal to the base emitter-threshold voltage of a conducting
30 transistor. If the level of the incoming video signal varies so rapidly that the gain control circuit of the receiver of which the

known circuit forms part cannot respond, then it may happen that the peak level detector cannot follow the shift produced. In that case, however, the synchronizing detector which is in the form of a coincidence stage initiates the non-synchronized state in which the phase difference between the line synchronizing pulses and the locally generated pulses of line frequency is greater than the said predetermined value. The synchronizing detector then renders a recovery circuit operative, which causes a fast variation of the clipping level whereby the loss in synchronizing pulses is reduced.

A circuit arrangement including such a peak detector has the disadvantage that if the incoming signal contains much noise and interferences, the level determined thereby may be incorrect. This can be seen if a disturbing pulse of a large amplitude which is superposed on a synchronizing pulse is considered. With the known circuit this results in a shift in the clipping level, which may result in a shift of the instant at which the output pulse of the comparator stage occurs.

The invention has for its object to provide a change of operation, however, not to compensate for fast level variations of the incoming video signal but to obtain an improved immunity from noise and interferences. To that end, the invention provides a synchronizing circuit arrangement of the type described in the opening paragraph which is characterised in that under the control of the synchronisation detector the peak level detector operates in the synchronized state as a mean-value detector in the presence of line frequency keying pulses occurring during those periods when the incoming video signal assumes a value corresponding with the peak level, and in the non-synchronized state operates as a peak detector.

Preferably, the circuit arrangement is characterised in that a reference level detector for detecting the reference level of the synchronizing pulses in the synchronized state operates as a mean-value detector in the presence of second line frequency keying pulses occurring during those periods when the incoming video signal assumes a value corresponding to the reference level, and operates

as a level detector in the non-synchronized state when synchronizing pulses do not occur, a combining stage being connected to the peak level detector and to the reference level detector to determine the clipping level.

5 Advantageously, the circuit arrangement may be characterised in that the comparator stage is only operational in the synchronized state during the occurrence of third keying pulses, produced simultaneously with line synchronizing pulses and whose pulse duration is slightly longer than that of a line synchronizing pulse, but is
10 operational in the non-synchronized state during the entire line period.

A line synchronizing circuit comprising a phase detector to determine the phase difference between the incoming line synchronizing signal and the locally generated signal derived from an oscillator
15 may be characterised in that in the synchronized state the control voltage generated by the phase detector for application to the oscillator assumes, prior to the occurrence of a line synchronizing pulse, the value which corresponds to the nominal frequency of the oscillator.

20 In one preferred embodiment the synchronizing circuit arrangement in accordance with the invention comprises a control circuit for maintaining the amplitude and the d.c. level of the synchronizing pulses applied to the comparator stage substantially constant, which control circuit comprises a direct current level detector, which is
25 known per se, namely from United States Patent 3 699 256 and whereby the influence of fast variations of the incoming video signal is significantly reduced, and is characterised in that the d.c. level detector operates in the synchronized state as a mean-value detector during the occurrence of the first keying pulse and as a level
30 detector in the non-synchronized state.

Advantageously, the circuit arrangement in accordance with the invention may further be characterised in that it also comprises a second comparator stage having a first input terminal for receiving the synchronizing pulses and a second input terminal which in the
35 non-synchronized state is connected to the second input terminal

of the first mentioned comparator stage and in the synchronized state to a second clipping level which corresponds to the difference between the peak level obtained by means of a sample-and-hold circuit controlled by a sampling pulse of the line frequency occurring
5 during the first half of each line synchronizing pulse and half the substantially constant amplitude of the synchronizing pulses, the second comparator stage having an output terminal coupled to the field synchronizing signal-separating stage.

The circuit arrangement may also be characterised in that in
10 the synchronized state the level detector comprises a limiter for limiting the level detector input signal to substantially the average value thereof.

The invention will now be further described by means of example with reference to the accompanying drawings. Herein:

15 Figure 1 shows a block schematic circuit diagram of a first embodiment of a synchronizing circuit arrangement in accordance with the invention, which forms part of a television receiver,

Figure 2 shows a block schematic circuit diagram of an enlarged second embodiment of a circuit arrangement in accordance with
20 the invention, and

Figure 3 shows a circuit diagram of a level detector suitable for incorporation in the arrangement of Figure 1 or 2.

In Figure 1 reference numeral 1 denotes an amplifier to an input terminal A of which a composite video signal is applied. This
25 signal which is received and processed in known manner in preceding stages, comprises a composite synchronizing signal having descending pulses whose amplitude extends between a reference and a peak level. As with the majority of television standards, the reference level differs only little from the black level of the video information.
30 The amplified video signal is applied to a peak level detector 2 for determining the peak level of the pulses, and to a reference level detector 3 for determining the reference level. Both detectors are constructed in known manner: detector 2 is a peak detector, whereas detector 3 comprises a controlled switch and a peak detector, the
35 switch being operated by the synchronizing pulses derived within the

1 circuit arrangement in such a manner that during the occurrence
of these pulses the switch is non-conducting and is conducting at
least in a portion of the remaining part of the time. Detectors 2
and 3 can be switched over from a mode of operation to another one
5 and the preceding holds for one of the states thereof.

The levels determined by detectors 2 and 3 are applied to a
combining stage 4, which comprises an adder stage and a voltage divider
to determine a level located between the peak and the reference
levels, preferably equidistant therebetween. When the amplitude
10 of the incoming synchronizing signal varies, the relative position
of the clipping level obtained remains fixed with respect to the
peak and the reference levels. This clipping level is applied to
the inverting input terminal of a comparator stage 5, which is in
the form of a differential amplifier to whose non-inverting input
15 terminal the video signal amplified by amplifier 1 is applied. From
this signal stage 5 only transmits and amplifies the portion located
between the peak and the clipping levels. Consequently, the signal
at the output terminal of stage 5 is a regenerated synchronizing
signal which is substantially free from interferences. This signal
20 is applied to the controlled switch in reference level detector 3
and to a line synchronizing circuit.

The line synchronizing circuit is implemented in the form of a
phase control loop comprising a phase detector 6 to which the synchro-
nizing signal from comparator stage 5 as well as a locally generated
25 signal of the line frequency are applied. Phase detector 6 generates
a voltage which depends on the phase difference between the signals
applied thereto and is smoothed by a loop filter 7. The smoothed
control voltage is applied to a voltage-controlled oscillator 8
for controlling the frequency and/or the phase thereof. Oscillator 8
30 has a nominal frequency, that is to say in the absence of control
voltage, of 625 kHz. The signal thereof is applied to a frequency
divider circuit 9, which divides the frequency by 40. So in the nominal
state the frequency of the obtained signal is 15.625 kHz, i.e. the
line frequency in accordance with the European standard. By means
35 of a pulse shaper 10 this signal is given the shape which is suitable

for a line deflection circuit. Pulse shaper 10 also generates other signals of the line frequency which are required in different places in the circuit arrangement. The signal produced by divider circuit 9, this signal being a square-wave signal, is also applied
5 as a local signal to phase detector 6. In this phase detector the phase difference between an edge of the square-wave and the centre of a line synchronizing pulse contained in the signal from stage 5 is determined in known manner for readjusting oscillator 8.

The clipping level obtained by means of stage 4 is also applied
10 to the inverting input terminal of a second comparator stage 11, which is in the form of a differential amplifier. The non-inverting input terminal of this second comparator stage is connected to the output terminal of amplifier 1. In these circumstances the output signal thereof is a composite synchronizing signal which is integrated
15 by an integrator 12. Thereafter the integrated signal is applied to the non-inverting input terminal of a third comparator stage 13, whose inverting input terminal is connected to a voltage which is derived from the supply voltage and has a value of, for example, 6 V. A suitable choice of the integration-time constant and of
20 this voltage ensures that the output signal of stage 13 is the field synchronizing signal which is suitable for application to a field synchronizing circuit 14 of a known type. So integrator 12 and stage 13 form a field synchronizing signal-separating circuit.

The signal from frequency divider circuit 9 and the synchronizing
25 signal supplied by comparator stage 5 are also applied to a coincidence detector 15. Therein, the coincidence between these signals is established, that is to say the at least partly simultaneous occurrence thereof. The line frequency reference signal from divider circuit 9 is applied as a clock signal to a counter 16 which is
30 reset by detector 15 when there is coincidence in this detector. When a predetermined number of coincidence states has occurred counter 16 applies a signal to a synchronizing detector 17. If this number is equal to 2, then counter 16 may be in the form of a bistable element. Synchronizing detector 17 has for its object to switch
35 certain elements of the circuit arrangement of Figure 1 as soon as

the chosen number, 2 in the example described, is obtained, which consequently may be used as a criterion to establish that the locally generated signal has the frequency and the phase of the incoming line synchronizing signals. One coincidence may alternatively suffice, in other words the synchronized state may be detected as soon as the line phase control loop formed by elements 6 to 9, inclusive is pulled in. In that case counter 16 is omitted. Alternatively, coincidence detector 15 may be replaced by a phase detector, which measures whether the phase difference decreases to below a predetermined value.

A switching action effected by means of synchronizing detector 17 is produced in loop filter 7, whose time constant is then increased in the synchronized state. This increases the insensitivity to interference of the control loop. In the circuit of Figure 1 level detectors 2 and 3 are then also switched. So the above-described operation of the circuit relates to the non-synchronized state, i.e. the state prior to pulling in of the line synchronizing circuit or after the synchronization has become lost, for example on switching to a different transmission.

Peak level detector 2 is supplied with a keying pulse generated by pulse-shaper 10 and having duration of approximately $3.2/\mu\text{s}$. In the synchronized state this pulse occurs within a line synchronization pulse, that is to say its leading edge occurs after the leading edge of a line synchronizing pulse and the trailing edge occurs before the trailing edge of this pulse. In the said state, detector 2 operates as a circuit which determines the mean value of the output signal of amplifier 1 during the occurrence of the keying pulse. For that purpose detector 2 comprises a controlled switch which conducts in response to the keying pulse and, more specifically, only during the occurrence thereof. A voltage which is approximately the average value of the voltage supplied during the occurrence of the keying pulse is present across a capacitor. So detector 2 operates as a keyed mean value detector. In the interval between two keying pulses the voltage obtained does not vary substantially and is substantially independent of noise and interferences. During the occurrence of the

keying pulse, the capacitor is charged or discharged, respectively but the variation of the voltage will usually be small, even in the presence of disturbing pulses having a large amplitude. If the noise is symmetrical, that is to say if there is as much signal above the mean value as below it, then the voltage obtained does not vary at all, which is in contrast with the situation prior to the switch-over, the maximum value being obtained by means of peak detection, so that in the presence of noise and interferences this detected maximum value may be incorrect.

In a similar manner reference level detector 3 is supplied with a keying pulse which is also generated by pulse-shaper 10 and which in the synchronized state occurs after the line synchronizing pulse and before the video information. In the switch state detector 3 operates during the occurrence of this pulse as a keyed mean-value detector for the output signal of amplifier 1 and that in the same manner as detector 2. From the foregoing it appears that the levels obtained in this manner and applied to stage 4, and consequently also the clipping level derived therefrom, are affected to a very low extent by noise and interferences.

Comparator stage 5 is also influenced by synchronization detector 17 when the synchronized state has been ascertained. For this purpose stage 5 is supplied with a keying pulse which is also generated by pulse-shaper 10 and has a duration of approximately $7\mu\text{s}$, and whose leading edge occurs before the leading edge of the line synchronizing pulse and the trailing edge occurs after the trailing edge of the line synchronizing pulse which has a duration from 4.5 to $5\mu\text{s}$. Stage 5 operates only during the occurrence of this keying pulse. Interference contained in the incoming video signal in the remaining portion of the line period is not transmitted and consequently cannot produce faulty synchronizing pulses. For this purpose a controlled switch incorporated in the supply lead of the keying pulse is rendered conductive by synchronization detector 17. This switch and also switches of a similar type for supplying keying pulses intended for level detectors 2 and 3 are not shown in Figure 1 for the sake of simplicity.

In the synchronized state phase detector 6 is also influenced by synchronization detector 17, more specifically in such a manner that shortly before the occurrence of a line synchronizing pulse the output capacitor of detector 6, which has a small capacitance value and across which the control voltage generated by phase detector 6 is present, is connected to the voltage corresponding to the nominal frequency of oscillator 8. As after the occurrence of the keying pulse the output voltage of phase detector 6 does not vary, interference present during the occurrence of a line synchronizing pulse will indeed, after having been smoothed by filter 7, cause a phase error for the next line but will consequently not be capable of affecting the lines subsequent thereto.

The circuit arrangement of Figure 1 will operate satisfactorily as long as the d.c. level and the amplitude of the video signal applied thereto vary only to a little extent. This will be so in many cases, as the receiver of which the circuit arrangement of Figure 1 is part, comprises gain control for controlling the gain of the stages preceding the circuit arrangement, in dependence on the amplitude of the received television signal. In spite of this, the synchronizing pulses contained in the input signal of the circuit arrangement may yet be submitted to unwanted variations, for example because in the incoming signal synchronizing pulses are clipped by saturated cable amplifiers. Amplitude variations may also occur on the reception of signals generated by picture pick-up and display devices.

Figure 2 shows a circuit arrangement which also operates satisfactorily in the event of variations in the video signal. In Figure 2 the same elements of Figure 1 are denoted by the same reference numerals. In Figure 2 the incoming video signal is applied to amplifier 1 via a bandwidth limiter 18, which comprises a low-pass filter for limiting the video signal. As a result thereof the noise superposed on the signal is somewhat integrated. The signal obtained reaches the inverting input terminal of amplifier 1 which has a controllable gain, which is for example controllable between 2 and 10 times. With this amplifier variations in the amplitude of the synchronizing pulses

between 0.1 and 1 V can be compensated for. The said input terminal is also connected to the inverting input terminal of an amplifier 19 having a fixed gain of, for example, 5 times. The non-inverting input terminals of amplifiers 1 and 19 are interconnected.

5 Elements 2, 3, 4 and 5 in Figure 2 are of the same construction and connected in the same way as in Figure 1. In addition, the peak level obtained by means of detector 2 is applied to the inverting input terminal of a differential amplifier 20 having a fixed gain of, for example, 4 times. The reference level obtained by means of
10 detector 3 is applied to the non-inverting input terminal of said amplifier. A voltage of, for example, 1.8 V is added to the reference level. Via a controlled switch 21 the output terminal of amplifier 20 is connected to an integrator 22, switch 21 being rendered conductive by synchronizing pulses received from comparator stage 5. So the
15 output signal of amplifier 20 is integrated only during the occurrence of these pulses. In this manner a long integration time constant is obtained without the necessity to give the capacitor of integrator 22 a high value. The output voltage of integrator 22 is applied to amplifier 1 to determine the gain thereof. From this it appears
20 that elements 2, 3, 20, 21 and 22 are part of a control loop by means of which the amplitude of the synchronizing pulses contained in the output signals of amplifier 1 can be kept substantially constant, namely at a value of approximately 1.8 V.

The output signal of amplifier 19 is applied to a peak level
25 detector 23, which determines the peak level of the synchronizing pulses. The level obtained is compared in a comparator stage 24 with a voltage of, for example, 7 V. Via an integrator 25 the output of stage 24 is fed back to the non-inverting input terminals of amplifiers 1 and 19. So by means of elements 19, 23, 24 and 25
30 a control loop is realized by means of which the peak level of the signal at the output of amplifier 1 is clamped at approximately 7 V, which value is substantially independent of the location of the peak level of the input signal, which location might have affected the level on the output terminal of amplifier 1. It will be obvious
35 that elements 19 and 23 for keeping the d.c. level at the output of

amplifier 1 constant may be combined with the corresponding elements 1 and 2, but this would make the assembly less stable. So the operation of the two described control loops results in the video signal applied to comparator stage 5 having a substantially constant amplitude and a substantially constant direct current level.

The operation just described of the control loops holds for the out of synchronization state. Peak detector 23 is supplied with the same keying pulse as peak detector 2. In the synchronized state detector 23 is switched by means of synchronization detector 17 and then operates during the occurrence of the keying pulse as a keyed mean-value detector. As detectors 2, 3 and 23 are switched in the same manner, both control loops are little affected by noise and interferences.

Bandwidth limiter 18 also operates in the synchronized state in a different manner than when the line phase control loop has not yet been pulled in. Under the influence of synchronization detector 17, limiter 18 is controlled by the gain control signal V_1 which controls the gain of the intermediate frequency stages (not shown) of the receiver in such a manner that the bandwidth is controlled in dependence on signal V_1 . The weaker the received television signal, the larger the gain of the intermediate frequency stages and the narrower the bandwidth of the video signal conveyed to amplifier 1. As a result thereof the video signal contains less noise than otherwise, but the edges of the synchronizing pulses become less steep, which may cause uncertainty about the instants at which these edges reach the clipping level in stage 5 after amplification in amplifier 1. A compromise must therefore be found to keep this time error as small as possible in the event of a weak signal. For a strong signal the bandwidth is only affected to a small extent so that the pulse edges are as steep as possible. In practice, bandwidth limiter 18 may be in the form of an RC-integration network, its resistor being shunted by a transistor, for example a field effect transistor. This transistor is non-conducting in the out of synchronization state. In the synchronized state voltage V_1 is applied to the input electrode of the transistor, causing the internal resistance

of the transistor which is arranged in parallel with the resistor to be dependent on voltage V_1 and changes the time constant of the RC-network. A given, but less strong limitation of the bandwidth, also takes place at a high signal value, which has been found
5 to be necessary at it may happen that a strong and yet noisy television signal is received, for example a signal conveyed cable system.

The field synchronizing signal-separating stage in Figure 2 is preceded by a controlled change-over switch 26. A common output
10 terminal thereof is connected to the inverting input terminal of comparator stage 11. In the out of synchronization state of detector 17, the clipping level obtained by means of stage 4 is conveyed to stage 11 via change-over switch 26. In the synchronized state switch 26 is brought under the control of detector 17 into a state
15 in which a different clipping level is conveyed, the reason being that the detectors 2 and 3 which operate as integrators in the synchronized state cannot respond sufficiently rapidly to the situation in which significant echos of a rather long duration, more than approximately $3\mu s$, are superposed on a white picture. At the
20 beginning of the field blanking interval echos of this type may cause a rapid d.c. shift of the level of the video signal applied to amplifier 1, with the effect that the field synchronizing signal can be lost.

The output signal of amplifier 1 is applied to a sample-and-hold
25 circuit 27, which receives a sampling pulse of line frequency from pulse shaper 10. This pulse has a duration of approximately $1\mu s$ and occurs during the first half of the line synchronizing pulses and of the equalizing and field synchronizing pulses occurring in the field blanking interval instead of line synchronizing pulses. So
30 circuit 27 determines the average value of the peak level of the said pulses, which level, if necessary, can vary rapidly. The peak level from detector 2 and the reference level from detector 3 are applied to a stage 28, in which stage half the difference between the levels applied thereto is determined. The level obtained corresponds to
35 half the substantially constant amplitude of the synchronizing pulses

contained in the output signal of amplifier 1. In a stage 29 this level is subtracted from the level in circuit 27 and in the synchronized state the result is used as the clipping level. As no unwanted, rapid shift occurs in the incoming video signal then this clipping level is substantially the same as the "slow" clipping level obtained by means of stage 4.

From frequency divider circuit 9 field synchronizing circuit 14 receives a signal of twice the line frequency. In known manner, this frequency is divided in circuit 14 to obtain the field frequency and the phase of the signal obtained is compared with that of the field synchronizing signal produced by comparator stage 13. Circuit 14 also comprises a synchronizing detector, which for simplicity is not shown in Figure 2, to ascertain that coincidence between the two signals of field frequency has occurred for a given number of times, for example 6 times. In a similar manner as comparator stage 5, comparator stage 13 becomes operative only during that portion of the field frequency in which the field synchronizing signal may be expected, so that interference occurring in the remaining portion of the period does not affect the field synchronization. For this purpose stage 13 receives from circuit 14 a keying pulse having a duration of at least that portion of the field blanking interval which comprises the field synchronizing signal. The same keying pulse is also applied either to line phase detector 6, or to stage 5 to put it out of operation, as a result of which the known instability which may occur at the beginning of a field in the line synchronizing circuit is eliminated.

The circuit arrangement of Figure 2 comprises also a head error detector 30. Owing to errors of the play-back heads of a picture pick-up and display device the received synchronizing pulses may become shifted such that in the time the keying pulses applied to detectors 2 and 3 in the synchronized state suddenly pass into the video information. A large difference then occurs between the previously detected peak level and the video signal now applied. This difference is measured by detector 30 which, on receipt of signals from a pick-up and display device is made operative by a signal VR.

If the difference between the amplitude of the video signal at the output terminal of amplifier 1 and the peak level determined by detector 2 achieves a predetermined value, for example 0.5 V, then head error detector 30 will immediately adjust synchronization
5 detector 17 to the out of synchronization state, causing the stages controlled by the detector 17 to be changed over. Signal VR is also applied to phase detector 6 to increase, for example by a factor of 6, the loop gain of the line phase control loop.

Finally, the circuit arrangement of Figure 2 comprises a counter 31
10 which, as does counter 16, receives the signal of line frequency as a clock signal from frequency divider circuit 9 and is reset by coincidence detector 15. Counter 31 counts the number of times coincidence has not occurred after the synchronized state has prevailed, for example because a change to a different transmission has been
15 effected. If this number exceeds a predetermined value, for example 16, then counter 31 adjusts synchronization detector 17 to the out of synchronization state, in which state the circuit of Figure 2 is indeed sensitive to interference but is rapidly adjusted to the synchronized state.

20 Starting problems may occur with the circuit arrangement of Figure 2 if amplifier 1 has too low a gain and stage 5 does not generate a synchronizing pulse. In that case the switch in detector 3 cannot become conductive. The circuit may be dimensioned in such a manner that the situation outlined above does not occur. This situation
25 will with certainty not occur when the said switch is not controlled by a pulse produced by stage 5 but by the output signal from a detector which determines the difference between the output signals of amplifier 1 and detector 2. This detector which is comparable with the above-described detector 30, applies a signal to the switch
30 in detector 3, causing this switch to become conducting in a period during which the synchronizing pulses have the reference level, if the measured difference exceeds a predetermined value.

The majority of elements in the circuit arrangement of Figures 1
or 2 may be of a known construction, so that they need not be
35 described in further detail. Figure 3 shows a circuit which may be used

for detectors 2 and 23.

In Figure 3, the emitters of two npn transistors T1 and T2 are interconnected and connected to a switch S1. The collector of transistor T1 is connected to the collector of a pnp transistor T3, whose emitter is connected to the positive terminal of a supply voltage source. In a similar manner the collector of transistor T2 is connected to the collector of a pnp transistor T4 whose emitter is connected to the positive terminal. The base of transistor T1 is the input of the circuit; during operation the video signal amplified by amplifier 1 is present on this input. Via a switch S2 the base of transistor T3 may be connected either to the collector of transistor T3 or to the collector of transistor T4. A current source I1 is arranged between switch S1 and the negative terminal of the supply source.

The base of transistor T4 is connected to the collector thereof and to the base of a further pnp transistor T5 whose emitter is connected to the positive terminal of the supply source, while the collector is connected to the collector and to the base of an npn transistor T6 and to the base of a further npn transistor T7. The emitters of transistors T6 and T7 are connected to the negative supply terminal. Via a switch S3 the collector of transistor T7 is connected to the base of transistor T2. A capacitor C is arranged between this base and the negative terminal of the supply source. Parallel therewith is the series arrangement of a switch S4 and a current source I2. Finally, the circuit comprises a pnp transistor T8 whose base is connected to the collector of transistor T1 and the collector to the base of transistor T2, while the emitter is connected to the positive terminal. That terminal of capacitor C which is connected to the base of transistor T2 is the output of the circuit of Figure 3.

Switches S1, S2, S3 and S4 are operated by pulses from detector 17 and that in such a manner that in the situation in which detector 2 operates as a peak level detector switches S1 and S4 conduct, while switch S3 is not-conducting and while switch S2 connects the base of transistor T3 to the collectors of transistors T2 and T4. In this

situation transistors T1 and T2 and source I1 form a differential amplifier. If the input voltage exceeds the output voltage then transistor T1 conducts as its collector is connected to the positive terminal of the supply source via the transistors T3 and T4 which
 5 operate as diodes, while transistor T2 is cut-off. Transistor T8 also conducts and the difference between its collector current and current I2 charges capacitor C. As current I2 has a low value this difference is positive so that the voltage across capacitor C increases. If the maximum value of the input signal, i.e. the peak
 10 level of the synchronizing pulses has been reached, then transistor T1 stops conducting. Current I1 which flowed therethrough now flows through transistor T2, while capacitor C is slowly discharged by current I2. By means of this current a detection resistance of a high value is as it were arranged in parallel with capacitor C.

15 In the other state of the circuit of Figure 3, switch S3 conducts while switch S4 is non-conducting and while switch S2 interconnects the base and the collector of transistor T3. Switch S1 now only conducts during the occurrence of the keying pulse. Transistors T3 and T8 now form a first current mirror and transistor T4 and T5
 20 form a second current mirror. As the emitter current of transistor T1 or T2, respectively cannot exceed the value I1, the currents produced by the two current mirrors cannot increase to above predetermined values. As a result thereof the input signal is sliced.

25 If during the occurrence of the keying pulse the input and output voltages are equal to each other then the collector currents of transistors T1 and T2 are equal. A charging current for capacitor C flows through transistor T8, while the collector current of transistor T7 is a discharging current, these currents being equal, thanks to a suitable dimensioning. So the voltage across the capacitor does not
 30 vary. If the input and output voltages are not equal to each other, then the collector currents of transistors T1 and T2 are not equal, as a result of which capacitor C is charged or discharged. The output voltage then increases or decreases. After the occurrence of the keying pulse, switch S1 is inhibited and the output voltage does
 35 not change until the next keying pulse. If during the occurrence

of the keying pulse the area of a time diagram of the limited input signal above the value obtained for the output voltage is not equal to the area thereunder, then the charging or discharging current, respectively continues to flow until the said areas are equal. So
5 the circuit so adjusts itself that the output voltage thereof corresponds to the average value of the limited input signal. If the input signal comprises few noise pulses of a large amplitude, then the value obtained is substantially equal to the average value of the input signal, in which case the limitation is not necessary.
10 Consequently, the limitation must be considered as a refinement.

The circuit shown in Figure 3 may be used for detector 3, the difference being that in the state in which detector 3 is operative as a reference level detector switch S1 will be inhibited at least during the occurrence of the synchronizing pulses. It will be
15 clear that detectors 2 and 3 may be implemented in a different manner from that shown in Figure 3. Instead of comprising a combined circuit, these detectors may, for example, each comprise a level detector and a keyed mean-value detector, the amplified video signal being applied to both the said portion either the one or
20 the other portion supplying the output signal.

In view of the large number of elements of the described circuit it will be obvious that the circuit arrangements will preferably be produced predominantly in the form of integrated circuits. The what is commonly referred to as LOCMOS technique has been found
25 to be very advantageous.

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CLAIMS:

1. A synchronizing circuit arrangement for deriving and processing a synchronizing signal contained in an incoming composite video signal, the synchronizing signal comprising line and field
5 synchronizing pulses whose amplitude extends between a reference and a peak level, the circuit arrangement comprising a peak level detector coupled to a signal input of the circuit arrangement for detecting the peak level of the synchronizing pulses, a comparator stage having a first input terminal coupled to the signal input,
10 a second input terminal for receiving a clipping level which corresponds to a given level located between the peak and the reference levels, and an output terminal for applying the resulting composite synchronizing signal to a line synchronizing circuit for generating a locally generated signal of line frequency, the
15 circuit arrangement further comprising a synchronization detector for detecting the occurrence of the synchronized state between incoming line synchronizing pulses and locally generated pulses where the phase difference is less than a predetermined value and for changing the mode of operation of portions of the circuit arrangement,
20 characterised in that under the control of said synchronization detector the peak level detector in the synchronized state operates as a mean-value detector in the presence of line frequency keying pulses occurring during those periods when the incoming video signal assumes a value corresponding to the peak level, and in the non-synchronized
25 state operates as a peak detector.
2. A circuit arrangement as claimed in Claim 1, characterised in that the leading and trailing edges of each keying pulse occur between the leading and trailing edges of an associated line synchronizing pulse.
- 30 3. A circuit arrangement as claimed in Claim 1, characterized



in that a reference level detector for detecting the reference level of the synchronizing pulses in the synchronized state operates as a mean-value detector in the presence of second line frequency keying pulses occurring during those periods when the incoming video signal assumes a value corresponding with the reference level, and operates as a level detector in the non-synchronized state when synchronizing pulses do not occur, a combining stage being connected to the peak level detector and to the reference level detector to determine the clipping level.

4. A circuit arrangement as claimed in Claim 3, characterized in that the leading and trailing edges of each second keying pulse occur between the trailing edge of a line synchronizing pulse and the commencement of the video information.

5. A circuit arrangement as claimed in Claim 1, characterized in that the comparator stage is only operational in the synchronized state during the occurrence of third keying pulses produced simultaneously with line synchronizing pulses and whose pulse duration is slightly longer than that of a line synchronizing pulse, but is operational in the non-synchronized state during the entire line period.

6. A circuit arrangement as claimed in Claim 1 in which the line synchronizing circuit comprises a phase detector for determining the phase difference between the incoming line synchronizing signal and the locally generated signal derived from an oscillator, characterized in that in the synchronized state the control voltage generated by the phase detector for application to the oscillator assumes, prior to the occurrence of a line synchronizing pulse, the value which corresponds to the nominal frequency of the oscillator.

7. A circuit arrangement as claimed in Claim 1, further comprising a control circuit for maintaining the amplitude and the d.c. level of the synchronizing pulses applied to the comparator stage substantially constant, which control circuit comprises a direct current level detector, characterised in that the d.c. level detector operates in the synchronized state as a mean-value detector during the occurrence of the first keying pulse and as a



level detector in the non-synchronized state.

8. A circuit arrangement as claimed in Claim 7, characterised in that the circuit arrangement also comprises a second comparator stage having a first input terminal for receiving the synchronizing pulses and a second input terminal which in the non-synchronized state is connected to the second input terminal of the first mentioned comparator stage and in the synchronized state to a second clipping level which corresponds to the difference between the peak level obtained by means of a sample-and-hold circuit, controlled by a sampling pulse of line frequency occurring during the first half of each line synchronizing pulse and half the substantially constant amplitude of the synchronizing pulses, the second comparator stage having an output terminal coupled to a field synchronizing signal-separating stage.

9. A circuit arrangement as claimed in Claim 8 further comprising a coincidence stage for detecting coincidence between field synchronizing pulses obtained by means of the field synchronizing signal-separating stage and locally generated pulses of field frequency, also comprising a counter for counting the number of times said coincidence has been detected, characterised in that either the first comparator stage or a line phase detector is inoperative during the occurrence of a fourth keying pulse when the number of times said coincidence occurs is at least equal to a predetermined number, the fourth keying pulse occurring at least in that portion of the field blanking interval which contains the field synchronizing signal.

10. A circuit arrangement as claimed in Claim 9, characterized in that the field synchronizing signal-separating stage is only operative during the occurrence of the fourth keying pulse.

11. A circuit arrangement as claimed in Claim 7, characterised in that a reference level detector for determining the reference level of the synchronizing pulses is operative in the synchronized state as a mean-value detector in the presence of second line frequency keying pulses occurring during those periods when the incoming video signal assumes a value corresponding to the reference level and in the non-synchronized state as a level detector when



fifth keying pulses are not present, a difference detector for determining the difference between the substantially constant amplitude of the synchronizing pulses and the level determined by the peak level detector generating the fifth keying pulse when the said difference is greater than a predetermined value, a combining stage being connected to the peak level detector and to the reference level detector for determining the clipping level.

12. A circuit arrangement as claimed in Claim 7, characterised by a second difference detector for determining the difference between the substantially constant amplitude of the synchronizing pulses and the peak level determined by the peak level detector and for controlling the synchronization detector so as to initiate the non-synchronized state when the said difference is greater than a predetermined value.

13. A circuit arrangement as claimed in Claim 1, characterised in that a bandwidth limiter for limiting the bandwidth of the incoming video signal is provided between the signal input of the circuit arrangement and the first input terminal of the comparator stage, the bandwidth being controlled in the synchronized state in response to a gain control signal, the weaker a received television signal containing the incoming video signal the narrower the bandwidth.

14. A circuit arrangement as claimed in Claim 1, characterised in that a counter controls the synchronization detector for initiating the synchronized state when the synchronized state has occurred for a predetermined number of times.

15. A circuit arrangement as claimed in Claim 1, characterized in that a counter controls the synchronization detector for initiating the non-synchronized state when the synchronized state has not occurred for a predetermined number of times.

16. A circuit arrangement as claimed in Claims 1, 3, 7 and 11, characterised in that the level detector in the synchronized state comprises a limiter for limiting the input signal of the level detector to substantially the average value thereof.

17. A circuit arrangement as claimed in Claim 16, characterised



in that the level detector comprises a differential amplifier for comparing the input and output signals of the level detector and for charging or discharging, respectively a capacitor, said differential amplifier operating in the synchronized state also as a limiter, the voltage of the capacitor being the level detector output signal.

18. A synchronizing circuit arrangement substantially as herein described with reference to the accompanying drawings.

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