WHAT IS CLAIMED IS:

1. An input/output circuit comprising:

a data pattern detector configured to output an up resistance control code and a down resistance control code according to whether input data has a consecutively varied pattern or an inconsecutively varied pattern; and

an output circuit configured to have resistance controlled in response to the up resistance control code and the down resistance control code, amplify the input data, and output the amplified data to an input/output pad.

2. The input/output circuit of claim 1, wherein the data pattern detector:

when bits of the input data are consecutively varied, designates at least one of the up resistance control code and the down resistance control code as at least one bit of a first value; and

when the bits of the input data are inconsecutively varied, designates each of the up resistance control code and the down resistance control code as at least one bit of a second value.

3. The input/output circuit of claim 1, wherein the output circuit includes:

a trigger controller configured to receive the input data, and output a pull-up pulse and a pull-down pulse according to the received data;

a first pull-up pre-driver configured to vary first internal resistance in response to the up resistance control code, and output a first pull-up code including a pull-up signal in response to the pull-up pulse;

a first pull-down pre-driver configured to vary second internal resistance in response to the down resistance control code, and output a first pull-down code including a pull-down signal in response to the pull-down pulse;

a second pull-up pre-driver configured to output pull-up data and a second pull-up code in response to the first pull-up code;

a second pull-down pre-driver configured to output pull-down data and a second pull-down code in response to the first pull-down code;

a pull-up main driver configured to output data of a logic high level to the input/output pad in response to the pull-up data and the second pull-up code; and

a pull-down main driver configured to output data of a logic low level to the input/output pad in response to the pull-down data and the second pull-down code.

4. The input/output circuit of claim 3, wherein the first pull-up pre-driver decreases the first internal resistance when the up resistance control code is designated as at least one bit of a first value, and increases the first internal resistance when the up resistance control code is designated as at least one bit of a second value.

5. The input/output circuit of claim 3, wherein the first pull-down pre-driver decreases the second internal resistance when the down resistance control code is designated as at least one bit of a first value, and increases the second internal resistance when the down resistance control code is designated as at least one bit of a second value.

6. A memory device comprising:

a memory cell array configured to store data; and

a peripheral circuit configured to store data received from a memory controller in the memory cell array in a program operation, read data stored in the memory cell array in a read operation, and output the read data to the memory controller,

wherein the peripheral circuit includes an input/output circuit configured to:

control internal resistance according to whether the read data has a consecutively varied pattern or an inconsecutively varied pattern; and

output the read data to the memory controller through an input/output pad ~~by controlling internal resistance according to a pattern of the read data~~.

7. The memory device of claim 6, wherein the input/output circuit includes:

an input circuit configured to receive the data from the memory controller through the input/output pad in the program operation, and

output a data signal in the read operation;

a data pattern detector configured to operate in response to the data signal, and output an up resistance control code and a down resistance control code according to ~~the bit~~a pattern of the read data; and

an output circuit configured to have resistance controlled in response to the up resistance control code and the down resistance control code, amplify the read data, and output the amplified data to the input/output pad.

8. The memory device of claim 7, wherein the input circuit:

inactivates the data signal in the program operation; and

activates the data signal in the read operation.

9. The memory device of claim 8, wherein the data signal is used as a power supply voltage of logic gates of the data pattern detector.

10. The memory device of claim 9, wherein the data pattern detector operates when the data signal is activated, and does not operate when the data signal is inactivated.

11. The memory device of claim 7, wherein the data pattern detector:

when the read data is consecutively varied, designates at least one of the up resistance control code and the down resistance control code as

at least one bit of a first value, and

when the read data is inconsecutively varied, designates each of the up resistance control code and the down resistance control code as at least one bit of a second value.

12. The memory device of claim 7, wherein the output circuit includes:

a trigger controller configured to output a pull-up pulse and a pull-down pulse according to the read data;

a first pull-up pre-driver configured to vary first internal resistance in response to the up resistance control code, and output a first pull-up code including a pull-up signal in response to the pull-up pulse;

a first pull-down pre-driver configured to vary second internal resistance in response to the down resistance control code, and output a first pull-down code including a pull-down signal in response to the pull-down pulse;

a second pull-up pre-driver configured to output ~~the~~ pull-up data and a second pull-up code in response to the first pull-up code;

a second pull-down pre-driver configured to output ~~the~~ pull-down data and a second pull-down code in response to the first pull-down code;

a pull-up main driver configured to output data of a logic high level to the input/output pad in response to the pull-up data and the second pull-up code; and

a pull-down main driver configured to output data of a logic low

level to the input/output pad in response to the pull-down data and the second pull-down code.

13. The memory device of claim 12, wherein the first pull-up pre-driver decreases the first internal resistance when the up resistance control code is designated as at least one bit of a first value, and increases the first internal resistance when the up resistance control code is designated as at least one bit of a second value.

14. The memory device of claim 12, wherein the first pull-down pre-driver decreases the second internal resistance when the down resistance control code is designated as at least one bit of a first value, and increases the second internal resistance when the down resistance control code is designated as at least one bit of a second value.

15. A method for operating a memory device, the method comprising:

reading memory cells;

outputting an up resistance control code and a down resistance control code according to a pattern of data read from the memory cells;

outputting a pull-up pulse or a pull-down pulse according to the read data; and

setting resistance according to the up resistance control code and the down resistance control code, and outputting a first pull-up code or a

first pull-down code in response to the pull-up pulse or the pull-down pulse.

16. The method of claim 15, wherein the outputting of the up resistance control code and the down resistance control code comprises:

when bits of the read data are consecutively varied, designating at least one of the up resistance control code and the down resistance control code by at least one bit of a first value, and

when the bits of the read data ~~is~~ are inconsecutively varied, designating each of the up resistance control code and the down resistance control code by at least one bit of a second value.

17. The method of claim 16, wherein the bits of the read data consecutively varied include '101' or '010,' and

wherein the bits of the read data inconsecutively varied include '000,' '001,' '011,' '100,' '110' or '111.'

18. The method of claim 15, wherein the first pull-up code includes a pull-up signal corresponding to the read data and a pull-up trimming code for trimming the read data, and

the first pull-down code includes a pull-down signal corresponding to the read data and a pull-down trimming code for trimming the read data.

19. The method of claim 18, further comprising: after the outputting of the first pull-up code or the first pull-down code,

outputting pull-up data for determining a logic high level of output data and a second pull-up code including a code obtained by re-trimming the pull-up trimming code in response to the first pull-up code, or outputting pull-down data for determining a logic low level of output data and a second pull-down code including a code obtained by re-trimming the pull-down trimming code in response to the first pull-down code; and

outputting data of a logic high level or data of a logic low level to an input/output pad in response to the second pull-up code or the second pull-down code.

20. An input/output circuit comprising:

a data pad;

a data pattern detector activated in response to a data output operation through the data pad to detect a pattern of bits in a sequence of output data and generating a resistance control code based on the detected pattern of bits in the sequence; and

an output circuit including a driver having ~~a~~ resistance that is controlled based on the resistance control code, the output circuit configured for receiving the output data and driving the data pad to output data in accordance with the controlled resistance of the driver,

wherein the resistance of the driver is controlled to have ~~a~~ first resistance when all of the bits of the sequence have the same value, ~~a~~

second resistance when a sub-sequence of bits, but not all bits, of the sequence have the same value, and ~~a~~ third resistance when no consecutive bits in the sequence have the same value.