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PATENT SPECIFICATION

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COMPLETE SPECIFICATION

DRAWINGS ATTACHED

Methods relating to Miniature Semiconductor Devices

We, TEXAS INSTRUMENTS INCORPORATED, of 13500 North Central Expressway, Dallas, Texas, United States of America, a corporation organized and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:

This invention relates to miniature semiconductor devices and more particularly to such devices having a configuration of regions and at least one elongated portion especially suitable for a semiconductor wafer to contain two or more diverse circuit elements therein.

One proposal which has been put forward in the field of circuit miniaturization has been to include, within a semiconductor body, some circuit elements of a phase shift oscillator including an alloyed transistor having p-n junctions near opposite surfaces of the semiconductor body and a distributed R-C circuit element integrally connected to the base region of the transistor. The limitations of the proposed structure and steps required for its manufacture do not facilitate production techniques and do not allow the manufacture of unitary structures with a wide variety of circuit elements therein or versatility in the number and kind of circuit elements that may be embodied in the unitary structure.

Some objects of the present invention are to provide a miniature semiconductor device which facilitates production of the device, which allows versatility in the number and kind of circuit elements formed in or on a wafer of semiconductor material and which allows the manufacture of unitary structures with a wide variety of circuit elements therein.

[Price 4s. 6d.]

This invention is a miniature semiconductor device comprising a wafer of single crystal semiconductor material, said wafer having closely adjacent one major face thereof a plurality of first regions each composed of semiconductor material of conductivity type opposite to that immediately underlying such first region and each occupying a limited portion of the area of said one major face, the first regions being laterally spaced and separated from one another along said one major face, said wafer having also closely adjacent said one major face thereof a plurality of second regions each overlying at least a portion of a respective different one of said first regions and each composed of semiconductor material of a conductivity type opposite to that of the semiconductor material immediately underlying such second region, each second region occupying a limited portion of the area of said one major face, an elongated portion defined in the wafer and providing an elongated current path generally parallel to said one major face, the elongated portion having a surface lying on a major face of the wafer and there occupying only a limited portion of the surface area of the major face, the elongated portion being spaced from said first regions for its entire length and being electrically isolated through the wafer from the first regions along at least the major portion of its length, and a pair of ohmic contacts secured to the wafer on a major face thereof and positioned at opposite ends of the elongated portion.

This invention also is a miniature semiconductor device comprising a wafer of single crystal semiconductor material, said wafer having closely adjacent one major face thereof two or more first regions each composed of semiconductor material of conductivity type opposite to that immediately un-

derlying such first region, and each occupying a limited portion of the area of said one major face, the first regions being laterally spaced and separated from one another along said one major face, said wafer having also closely adjacent said one major face thereof two or more second regions each overlying at least a portion of a respective different one of said first regions and each composed of semiconductor material of a conductivity type opposite to that of the semiconductor material immediately underlying such second region, each second region occupying a limited portion of the area of said major face, first and second elongated portions defined in the wafer and each providing an elongated current path parallel to said one major face, said first and second elongated portions each having a surface lying on a major face of the wafer and there occupying a limited portion of the surface area of the major face, the first and second elongated portions being spaced from said first regions for their entire lengths and being electrically isolated through the wafer from the first regions along at least the major portion of their lengths, third and fourth elongated portions defined in the wafer and each providing an elongated current path generally parallel to said one major wafer, the third and fourth elongated portions each having a surface lying on a major face of the wafer and there occupying a limited portion of the surface area of the major face, third and fourth regions of the wafer closely adjacent one major face thereof, each of said third and fourth regions being composed of semiconductor material of conductivity type opposite to that immediately underlying such region, each third and fourth region occupying a limited portion of the area of said one major face, said third and fourth regions being laterally spaced and separated from one another and from said first regions along said one major face, a first pair of ohmic contacts secured to the wafer on a major face thereof and being positioned at opposite ends of the first elongated portion, a second pair of ohmic contacts secured to the wafer on a major face thereof and being positioned at opposite ends of the second elongated portion, a first plurality of electrical contacts secured to said one major face and ohmically connected one to each of said first regions, a second plurality of electrical contacts secured to said one major face and ohmically connected one to each of said second regions, a third plurality of electrical contacts secured to said one major face and ohmically connected one to each of said third and fourth regions, and means interconnecting selected one of said contacts.

The semiconductor device according to the invention generally has the regions and elongated portions which are to comprise circuit elements formed closely adjacent one major wafer face and to fabricate the device there may be utilized a combination of steps such as diffusion of conductivity type producing ingredients into a semiconductor wafer, masking in order to define predetermined areas of the wafer in which circuit elements are to be formed and mechanical and/or electrical shaping to confine paths for current flow.

Circuit elements within or on the semiconductor wafer may be effectively electrically isolated through the advantageous employment of electrical and/or mechanical shaping.

Shaping includes various ways of obtaining the confined current paths which ways include, as mechanical shaping, the removal of portions of the semiconductor material as by etching, and specialized configuration of the semiconductor material such as long and narrow "L" shaped, "V" shaped, etc., and which ways further include, as electrical shaping, selective conversion of intrinsic semiconductor material by diffusion of impurities thereinto to provide low resistivity paths for current flow and selective conversion of semiconductor material of one conductivity-type to the opposite conductivity-type wherein the p-n junction thereby formed acts as a barrier to current flow.

The invention will be apparent from the following more complete discussion of the cooperative relationships which exist in the forming, shaping and positioning of the various areas within a wafer of single crystal semiconductor material to produce a miniature semiconductor device susceptible of exploitation in a variety of practical circuit embodiments.

In the accompanying drawings:—

Figures 1 to 5a illustrate schematically various circuit components, a number of which may be fabricated in accordance with the present invention in and/or on a wafer of single crystal semiconductor material to be adapted to form at least part of a miniature electrical circuit.

Figure 6a illustrates schematically a multivibrator circuit embodying the present invention.

Figure 6b shows the wiring diagram for the multi-vibrator circuit of Figure 6a laid out in the same relationship and

Figure 7 illustrates the wiring diagram of the multivibrator circuit of Figure 6a in a more conventional presentation.

Referring now to the drawings in detail, preferred embodiments of the present invention will now be described in detail in order that a better understanding of the invention and the various forms and embodiments of the invention may be obtained.

Figures 1-5a inclusive illustrate in detail

circuit elements which can be formed in and/or on a single wafer of semiconductor material. It is noted at this point that the wafer of semiconductor material is of single crystal structure, and can be composed of any suitable semiconductor material. There may be mentioned as example of suitable materials germanium, silicon, intermetallic alloys such as gallium arsenide, aluminium antimonide, indium antimonide, as well as others.

Referring particularly to Figure 1, there is shown a typical design for a resistor which may be formed in a wafer or single crystal semiconductor with at least one other circuit element. As noted in Figure 1, the design contemplates utilizing the bulk resistance of an elongated portion of body 10 of semiconductor material of either n or p-type conductivity. Contacts 11 and 12 are made ohmically to one surface of the body 10 at opposite ends of said elongated portion and spaced apart a sufficient distance to achieve a desired resistance. As will be apparent to one skilled in the art, ohmic connections are those which exhibit symmetry and linearity in terms of resistance to flow of current in any available direction. If two resistors are to be connected together, it is not necessary to provide separate terminations for the common point. The resistance may be calculated from

$$R = \rho L/A$$

Where L is the active length in centimetres, A is the cross sectional area, and ρ is the resistivity in ohm-cm of the semiconductor material.

In addition and alternatively to the resistor shown in Figure 1, a resistor may be provided as shown in Figure 1a formed as an elongated portion of a wafer of single crystal semiconductor material. In Figure 1a, there is shown a body comprising a region 10a of p-type semiconductor material and an elongated n-type region or portion 10b. Of course, between the region 10a and portion 10b there is a p-n junction which is designated by the numeral 13. Contacts 11a and 12a are made to the outside surface of the portion 10b at opposite ends thereof and spaced apart from each other in order to achieve a desired resistance. As in Figure 1, the contacts 11a and 12a are ohmic contacts to the portion 10b. A resistor formed in the manner of Figure 1a has several important advantages. First, the p-n junction 13 provides a barrier to current flow from the n-type portion 10b into the p-type region 10a and, thus, the current flow is confined to a path in the n-type portion 10b between the contacts thereto. The second advantage in that the total resistance value thereof can be controlled to a large degree. The total resistance value may be controlled by etching very lightly over the entire surface to remove the uppermost portion of the n-type portion 10b, being very careful not to etch through the p-n junction. The third, and perhaps major advantage in forming a resistor according to Figure 1a is in that, by controlling the doping level or impurity concentration in the n-type portion 10b, lower and more nearly constant temperature coefficients may be provided for the resistor.

The above description has been in terms of a p-type region 10a and an n-type portion 10b but it is obvious that the region 10a could be equally as well of n-type conductivity and the portion 10b of p-type conductivity.

Capacitor designs may be obtained by utilizing the capacitance of a p-n junction, as shown in Figure 2, wherein is shown a semiconductor body comprising region 15 of p-type conductivity and an n-type diffused region 16. Ohmic contacts 17 are made to opposite faces of the body 15, 16. The capacitance of a diffused junction is given by

$$C = A\epsilon \left(\frac{q\,a}{12\,\epsilon\,V} \right)^{\frac{1}{3}}$$

where A is the area of the junction in square cm, ϵ is the dielectric constant, q is electronic charge, where a is the impurity density gradient and V is the applied voltage.

Instead of the capacitor of Figure 2, capacitance in a body of single crystal semiconductor material may be provided as shown and described in connection with Figure 2a, and which capacitor is the subject of our co-pending patent application No. 5691/62 (Serial No. 945,737). Figure 2a shows a body 15a of single crystal semiconductor material of either n-or p-type conductivity, which constitutes one plate of the capacitor. Evaporated on to the body 15a is a layer 18 providing a dielectric layer for the capacitor. It is necessary that the layer 18 have a suitable dielectric constant and be inert when in contact with the semiconductor body 15a. Silicon dioxide has been found to be a suitable material for dielectric layer 18 and may be applied by evaporation or thermal oxidation techniques onto body 15a. Plate 19 forms the other plate of the capacitor and is provided by eveporating a conductive material onto layer 18. Gold and Aluminium have been found to be satisfactory materials for the plate 19. Ohmic contact 17a is made to the body of semiconductor material 15a and contact to plate 19 may be made by any suitable electric contact (not shown). Capacitors formed in the manner described in connection with Figure 2a have been found to exhibit much more stable characteristics than pure junction capacitors, that is p-n junction capacitors.

Capacitors produced in the manner of Figure 2 are also diodes, and must, therefore, be properly polarized in the circuit. Non-

polar capacitors may be made by connecting two such areas back to back. Although junction capacitors have a marked voltage dependance, such dependance is present to a lesser degree for low voltage in the non-polar configuration.

Resistor and capacitor designs may be combined to form a distributed R-C network. Such is shown in Figure 3, wherein a body comprising a region 20 of p-type conductivity has an n-type conductivity diffused region 21 formed therein. A broad area contact 22 is placed on the diffused region on one face of the body and spaced contacts 23 on the opposite face of the body. These networks are useful for low pass-filters, phase shift networks, coupling elements, etc. Their parameters may be calculated from the equations above. Other configurations of this general type are also possible.

As shown in Figures 4 and 5, transistors and diodes may be formed on or in a single wafer. In Fig. 4, the transistor has a collector region 25, a diffused p-n junction 26, a base layer 27, an emitter contact 28 forming a rectifying connection with base layer 27 and base and collector contacts 29 and 30, respectively. The base layer 27 is formed as a mesa of small cross section. A diode of similar design is shown in Figure 5 and consists of region 35 of one type conductivity, and a mesa region 36 of opposite conductivity-type with a p-n diffused junction formed therebetween and contacts 37 and 48 connected to each region.

Small inductances, suitable for high frequency use, may also be made by shaping the semiconductor as evidenced by Figure 5a, which shows a spiral of semiconductor material. It is also possible to prepare photosensistive devices, including photovoltaic cells photoresistors and solar cells and other like components utilizing the basic design considerations hereinbefore outlined.

Although all the circuit elements have been described in terms of a single diffused layer, it is quite possible to use, where practical, double diffused structure. Thus, double diffusion may be employed to form both n-p-n and p-n-p transistor structure, for example. Moreover, any suitable materials can be used for the semiconductor materials, conductivity producing impurities and contact materials; and suitable and known processing can be exploited to produce circuit element designs.

Because all of the circuit element designs described above can be formed from a single material, a semiconductor, it is possible by shaping to integrate all of them into a single crystal semiconductor wafer and to process the wafer to provide the proper network and the correct circuit element values.

As will be apparent to one skilled in the art, circuit elements can be classified according to their circuit functions. Thus, circuit elements may be thought of as being either active or passive in nature. Active elements are those which in an impedance network act as current generators; whereas passive elements do not so act, and the term "active element(s)" and "passive elements(s)" where used hereinafter and in the claims are to be construed in this sense. Examples of active elements are photovoltaic cells and transistors, and examples of passive elements are resistors, capacitors and inductors. Elements which fall into the general category of diodes and are normally employed as passive elements, may if suitable biased and energized, function in an active nature.

A specific illustration of an electronic circuit embodying the invention is shown in Figure 6a. As shown, a thin wafer of single crystal semiconductor material contains a p-n junction formed between two monocrystalline layers, which wafer has been processed and shaped to include discrete areas adapted to provide the electrical properties of circuit elements forming a complete and integrated multivibrator electronic circuit closely adjacent one major wafer face. The regions and portions of the wafer have been marked with symbols representative of the circuit element functions that are performed in the various areas. Figure 6b shows a wiring diagram of the various circuit functions in the relationship which they occupy in the wafer of Figure 6a. A more conventionally drawn circuit diagram is shown in Figure 7 with the circuit values actually used. The multivibrator circuit shown in Figure 6a, 6b and 7 will be described as illustrative of the processing techniques required. First, a wafer of single crystal semiconductor material, preferably silicon or germanium, of the proper resistivity is lapped and polished on one side. For this design, 3 ohm-cm p-type germanium was used. The wafer was then subjected to an antimony diffusion process which produced a monocrystalline n-type layer on the surface about 0.7 mils deep. The wafer was then cut to the proper size, 0.200×080 inches and the unpolished surface lapped to give a wafer thickness of 0.0025 inches.

Gold plated Kovar (Registered Trade Mark) leads 50 were attached by alloying to the wafer in the proper positions. Kovar is a trade name for an iron-nickel- cobalt alloy. Gold was then evaporated through a mask to provide the areas 51-54 which provide ohmic contact with the n region, such as the transistor base connections and the capacitor contacts. Aluminium was evaporated through a properly shaped mask to provide the transistor emitter areas 56, which form rectifying contacts with the n layer. Alternatively a p-type conductivity producing ingredient may be diffused through a properly shaped mask to provide the transistor emitter areas 56. Suitable ohmic con-

tacts may be secured to the emitter areas in the same manner as the securing of contacts 53 and 54 to base areas of transistors T_2 and T_1. When the emitter area is formed either by diffusion or alloying a monocrystalline layer of conductivity type opposite to that of the base region is provided. The monocrystalline layers of the base and emitter regions are contiguous and form therebetween a p-n junction extending to the major wafer face and there defining an enclosed area of semiconductor material.

In the completed device the p-n junction formed between the collector and base regions also extends to the major wafer face and there defines an enclosed area of semiconductor material surrounding the first mentioned enclosed area.

The wafer was then coated with a photosensitive resist or lacquer, such as Eastman (Registered Trade Mark) Photo Resist, supplied by Eastman Kodak Company, and exposed through a negative to a light. The lacquer image remaining after development was used as a resist for etching the wafer to the proper shape. In particular, this etching forms a slot through the wafer to provide an isolation volume between elongated portions R_1 and R_2 thereby electrically isolating R_1 and R_2 from each other along at least a major part of their lengths and from the rest of the circuit elements. This etching also shapes all of the resistor areas to the previously calculated configuration. Either chemical etching or electrolytic etching may be used, although electrolytic etching appears to be preferable.

After this step, the photoresist was removed with a solvent, and the areas 60, and such other areas as necessary, were masked by the same photographic process. The wafer was again immersed in etchant, and the a layer completely removed in the exposed areas thereby forming the mesa shapes. A chemical etch is considered perferable. The photoresist was then removed.

Gold wires 70 were then thermally bonded to the appropriate areas to complete the connections and a final clean-up etch given. Instead of using the gold wires 70 in making electrical connections, connections may be provided in other ways. For example, in accordance with the invention described in our co-pending patent application No. 3836/63, (Serial No. 945.938), an insulating and inert material such as silicon oxide may be evaporated onto the semiconductor circuit wafer through a mask either to cover the wafer completely except at the points where electrical contact is to be made thereto, or to cover only selected portions joining the points to be electrically connected. Electrically conducting material such as gold may then be laid down on the insulating material to make the necessary electrical circuit connections.

After testing, the circuit may be hermetically sealed, if required, for protection against contamination. The finished device was smaller by several orders of magnitude than any others which have previously been proposed. Because the fabrication steps required are quite similar to those now used in manufacturing transistors and because of the relatively small number of steps required, these devices are inherently inexpensive and reliable as well as compact.

It must be emphasized that the embodiment described above is merely an example of innumerable networks which can be fabricated embodying the present invention. There is no limit upon the complexity of configuration of circuits which can be made in this manner, for example any desired cooperative combination of selected circuit elements and having configuration of regions and portions in accordance with the invention, as hereinbefore described may be embodied in a single wafer to form a network and the network may be such that upon the application of electrical power, there is performed within the structure an electrical function equivalent to the function performed by a plural element electrical network. While there is a limit upon the types and values of circuit elements which can be made in a limited space, the invention hereof nevertheless represents a remarkable improvement over the prior art. As evidence of the advance in the art accomplished by the present invention, it is possible using the principles described above to achieve component densities of greater than thirty million per cubic foot as compared with five hundred thousand per cubic foot which is the highest component densities attained prior to this invention.

Reference is additionally made to our co-pending parent patent Application No. 3633/60 and to our co-pending patent applications Nos. 27542/63; 27196/63; 27326/63; 27197/63; 28004/63; 27198/63; 28005/63; 27540/63; 32744/63 and 27541/63 (Serial Nos. 945,734, 945,746, 945,740, 945,743, 945,741, 945,747, 945,742, 945,748, 945,744, 945,749, and 945,745), also divided from said parent application.

Terms indicative of position such as "on" "overlying" and "underlying" are used in the following claims to define relationship of parts in a form convenient for the purpose, but such terms are not to be construed in any restrictive sense and it will be manifest that the semiconductor devices could be utilised in any desired positional orientation.

WHAT WE CLAIM IS:—

1. A miniature semiconductor device comprising a wafer of single crystal semiconductor material, said wafer having closely adjacent one major face thereof a plurality of first regions each composed of semicon-

tacts may be secured to the emitter areas in the same manner as the securing of contacts 53 and 54 to base areas of transistors T_2 and T_1. When the emitter area is formed either by diffusion or alloying a monocrystalline layer of conductivity type opposite to that of the base region is provided. The monocrystalline layers of the base and emitter regions are contiguous and form therebetween a p-n junction extending to the major wafer face and there defining an enclosed area of semiconductor material.

In the completed device the p-n junction formed between the collector and base regions also extends to the major wafer face and there defines an enclosed area of semiconductor material surrounding the first mentioned enclosed area.

The wafer was then coated with a photosensitive resist or lacquer, such as Eastman (Registered Trade Mark) Photo Resist, supplied by Eastman Kodak Company, and exposed through a negative to a light. The lacquer image remaining after development was used as a resist for etching the wafer to the proper shape. In particular, this etching forms a slot through the wafer to provide an isolation volume between elongated portions R_1 and R_2 thereby electrically isolating R_1 and R_2 from each other along at least a major part of their lengths and from the rest of the circuit elements. This etching also shapes all of the resistor areas to the previously calculated configuration. Either chemical etching or electrolytic etching may be used, although electrolytic etching appears to be preferable.

After this step, the photoresist was removed with a solvent, and the areas 60, and such other areas as necessary, were masked by the same photographic process. The wafer was again immersed in etchant, and the a layer completely removed in the exposed areas thereby forming the mesa shapes. A chemical etch is considered perferable. The photoresist was then removed.

Gold wires 70 were then thermally bonded to the appropriate areas to complete the connections and a final clean-up etch given. Instead of using the gold wires 70 in making electrical connections, connections may be provided in other ways. For example, in accordance with the invention described in our co-pending patent application No. 3836/63, (Serial No. 945,938), an insulating and inert material such as silicon oxide may be evaporated onto the semiconductor circuit wafer through a mask either to cover the wafer completely except at the points where electrical contact is to be made thereto, or to cover only selected portions joining the points to be electrically connected. Electrically conducting material such as gold may then be laid down on the insulating material to make the necessary electrical circuit connections.

After testing, the circuit may be hermetically sealed, if required, for protection against contamination. The finished device was smaller by several orders of magnitude than any others which have previously been proposed. Because the fabrication steps required are quite similar to those now used in manufacturing transistors and because of the relatively small number of steps required, these devices are inherently inexpensive and reliable as well as compact.

It must be emphasized that the embodiment described above is merely an example of innumerable networks which can be fabricated embodying the present invention. There is no limit upon the complexity of configuration of circuits which can be made in this manner, for example any desired cooperative combination of selected circuit elements and having configuration of regions and portions in accordance with the invention, as hereinbefore described may be embodied in a single wafer to form a network and the network may be such that upon the application of electrical power, there is performed within the structure an electrical function equivalent to the function performed by a plural element electrical network. While there is a limit upon the types and values of circuit elements which can be made in a limited space, the invention hereof nevertheless represents a remarkable improvement over the prior art. As evidence of the advance in the art accomplished by the present invention, it is possible using the principles described above to achieve component densities of greater than thirty million per cubic foot as compared with five hundred thousand per cubic foot which is the highest component densities attained prior to this invention.

Reference is additionally made to our co-pending parent patent Application No. 3633/60 and to our co-pending patent applications Nos. 27542/63; 27196/63; 27326/63; 27197/63; 28004/63; 27198/63; 28005/63; 27540/63; 32744/63 and 27541/63 (Serial Nos. 945,734, 945,746, 945,740, 945,743, 945,741, 945,747, 945,742, 945,748, 945,744, 945,749, and 945,745), also divided from said parent application.

Terms indicative of position such as "on" "overlying" and "underlying" are used in the following claims to define relationship of parts in a form convenient for the purpose, but such terms are not to be construed in any restrictive sense and it will be manifest that the semiconductor devices could be utilised in any desired positional orientation.

WHAT WE CLAIM IS:—

1. A miniature semiconductor device comprising a wafer of single crystal semiconductor material, said wafer having closely adjacent one major face thereof a plurality of first regions each composed of semicon-

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ductor material of conductivity type opposite to that immediately underlying such first region, and each occupying a limited portion of the area of said one major face, the first regions being laterally spaced and separated from one another along said one major face, said wafer having also closely adjacent said one major face thereof a plurality of second regions each overlying at least a portion of a respective different one of said first regions and each composed of semiconductor material of a conductivity type opposite to that of the semiconductor material immediately underlying such second region, each second region occupying a limited portion of the area of said one major face, an elongated portion defined in the wafer and providing an elongated current path generally parallel to said one major face, the elongated portion having a surface lying on a major face of the wafer and there occupying only a limited portion of the surface area of the major face, the elongated portion being spaced from said first regions for its entire length and being electrically isolated through the wafer from the first regions along at least the major portion of its length, and a pair of ohmic contacts secured to the wafer on a major face thereof and positioned at opposite ends of the elongated portion.

2. A miniature semiconductor device according to claim 1, including another elongated portion defined in the wafer and providing an elongated current path generally parallel to said one major face, said other elongated portion having a surface lying on a major face of the wafer and there occupying only a limited portion of the surface area of the major face, the elongated portions being electrically isolated along their lengths from each other and the other elongated portion being electrically isolated through the wafer from the first regions along at least the major portion of its length and having a pair of ohmic contacts positioned at opposite ends thereof.

3. A miniature semiconductor device according to either preceding claim, including a first plurality of electrical contacts secured to said one major wafer face and ohmically connected one to each of said first regions.

4. A miniature semiconductor device according to claim 3, including a second plurality of electrical contacts secured to said one major wafer face and ohmically connected one to each of said second regions.

5. A miniature semiconductor device according to claim 4, including a third plurality of electrical contacts ohmically connected one to each region immediately underlying said first regions.

6. A miniature semiconductor device according to any of claims 3 to 5, including conductive means connected to predetermined ones of said electrical contacts.

7. A miniature semiconductor device according to any preceding claim, wherein each first region, the overlying second region and the region immediately underlying said first region define a transistor.

8. A miniature semiconductor device according to claim 7, wherein the transistor includes the first region as the base, the second region as the emitter, and the region immediately underlying the first region as the collector.

9. A miniature semiconductor device according to claims 1, 3 and 6 or 1, 3, 6 and 7 or 8, wherein said conductive means includes means interconnecting a selected one of said ohmic contacts and a selected one of said first plurality of electrical contacts.

10. A miniature semiconductor device according to claims 2, 3 and 6 or 2, 3, 6 and 7 or 8, wherein said conductive means includes means interconnecting a selected one of each pair of said ohmic contacts and a respective different selected one of said first plurality of electrical contacts.

11. A miniature semiconductor device according to any of claims 2 to 10, including a third elongated portion defined in the wafer and providing an elongated current path generally parallel to said one major face, said third elongated portion having a surface lying on a major face of the wafer and there occupying only a limited portion of the surface area of the major face, and a pair of ohmic contacts secured to the wafer on a major face thereof and positioned at opposite ends of the third elongated portion.

12. A miniature semiconductor device according to claim 11, wherein one end of said third elongated portion is ohmically connected to the region immediately underlying one of said first regions.

13. A miniature semiconductor device according to claim 11 or 12, including a fourth elongated portion defined in the wafer and providing an elongated current path generally parallel to said one major face, said fourth elongated portion having a surface lying on a major face of the wafer and there occupying only a limited portion of the surface area of the major face, and a pair of ohmic contacts secured to the wafer on a major face thereof and positioned at opposite ends of the fourth elongated portion.

14. A miniature semiconductor device according to claims 12 and 13, wherein one end of said fourth elongated portion is ohmically connected to the region immediately underlying the other or another one of said first regions.

15. A miniature semiconductor device according to any preceding claim, wherein the P-N junction defined between said first and second regions extends to said one major wafer face.

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16. A miniature semiconductor device according to any preceding claim, wherein the P-N junction defined between the first region and the region immediately underlying the first region extends to said one major wafer face.

17. A miniature semiconductor device according to claims 15 and 16, wherein each of said P-N junctions terminates at said one major face of the wafer in an enclosed surface area.

18. A miniature semiconductor device comprising a wafer of single crystal semiconductor material, said wafer having closely adjacent one major face thereof two or more first regions each composed of semiconductor material of conductivity type opposite to that immediately underlying such first region, and each occupying a limited portion of the area of said one major face, the first regions being laterally spaced and separated from one another along said one major face, said wafer having also closely adjacent said one major face thereof two or more second regions each overlying at least a portion of a respective different one of said first regions and each composed of semiconductor material of a conductivity type opposite to that of the semiconductor material immediately underlying such second region, each second region occupying a limited portion of the area of said major face, first and second elongated portions defined in the wafer and each providing an elongated current path generally parallel to said one major face, said first and second elongated portions each having a surface lying on a major face of the wafer and there occupying a limited portion of the surface area of the major face, the first and second elongated portions being spaced from said first regions for their entire lengths and being electrically isolated through the wafer from the first regions along at least the major portion of their lengths, third and fourth elongated portions defined in the wafer and each providing an elongated current path generally parallel to said one major wafer face, the third and fourth elongated portions each having a surface lying on a major face of the wafer and there occupying a limited portion of the surface area of the major face, third and fourth regions of the wafer closely adjacent one major face thereof, each of said third and fourth regions being composed of semiconductor material of conductivity type opposite to that immediately underlying such region, each third and fourth region occupying a limited portion of the area of said one major face, said third and fourth regions being laterally spaced and separated from one another and from said first regions along said one major face, a first pair of ohmic contacts secured to the wafer on a major face thereof and being positioned at opposite ends of the first elongated portion, a second pair of ohmic contacts secured to the wafer on a major face thereof and being positioned at opposite ends of the second elongated portion, a first plurality of electrical contacts secured to said one major face and ohmically connected one to each of said first regions, a second plurality of electrical contacts secured to said one major face and ohmically connected one to each of said second regions, a third plurality of electrical contacts secured to said one major face and ohmically connected one to each of said third and fourth regions, and means interconnecting selected ones of said contacts.

19. A miniature semiconductor device according to claim 18, wherein one end of said third elongated portion is ohmically connected to the region immediately underlying one of said first regions, and one end of said fourth elongated portion is ohmically connected to the region immediately underlying another one of said first regions.

20. A miniature semiconductor device according to claim 19, including a first conductive lead means connecting one of said first plurality of contacts to one of said third plurality of contacts and one of said first pair of ohmic contacts, second conconductive lead means connecting another of said first plurality of electrical contacts to another of said third plurality of electrical contacts and one of said second pair of ohmic contacts, and bias potential means connecting said third and fourth elongated portions and said second regions.

21. A miniature semiconductor device according to any of claims 18 to 20, wherein each first region, the overlying second region, and the region immediately underlying said first region define a transistor.

22. A miniature semiconductor device according to claim 21, wherein said third and fourth elongated portions constitute collector load resistors for respective transistors.

23. A miniature semiconductor device according to claim 20 or 21, wherein said first and second elongated portions constitute base resistors for respective transistors.

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