CLAIMS

What is claimed is:

1. A method of testing a semiconductor device, the method comprising:

contacting a pad of the semiconductor device with a plurality of probe needles, the plurality of probe needles comprising a plurality of first needles and at least one second needle;

supplying current through the plurality of first needles, wherein supplying current comprises regulating the current through each of the plurality of first needles with a plurality of current control circuits, such that currents through the plurality of first needles have a predetermined relationship;

measuring a voltage at the at least one second needle, wherein

for each first needle of the plurality of first needles, regulating the current comprises: receiving, at a control input to a control loop in a current control circuit of the plurality of current control circuits, the measured voltage:

coupling the first needle to the control loop: and

regulating the current through the first needle with the control loop based on the measured voltage.

2. The method of claim 1, wherein:

regulating the current comprises, in a current splitter, generating a current supplied through each of the plurality of first needles.

3. The method of claim 2, wherein:

generating the current supplied through each of the plurality of first needles comprises:

supplying the current through each of the plurality of needles in the range of 0 Amps to 7 Amps; and

supplying an aggregate current through the plurality of needles in the range of 40 Amps to 60 Amps.

4. The method of claim 1, further comprising:

computing an ON resistance of the semiconductor device based on the measured voltage.

5. A method of manufacturing a semiconductor device incorporating the method of testing of claim 4,

further comprising; selecting at least one subsequent step in the manufacturing based on the computed ON resistance.

6. The method of claim 1, further comprising:

sensing contact resistance between needles of the plurality of first needles and the semiconductor device; and generating an alarm when a sensed contact resistance exceeds a threshold.

7. The method of claim 1, wherein:

an ON resistance of the semiconductor device is less than 5 milliOhm.

8. The method of claim 1, wherein:

the semiconductor device is a power FET.

9. The method of claim 1, wherein:

the at least one second needle comprises a plurality of second needles; and a tip of each of the plurality of second needles is positioned adjacent a tip of a needle of the plurality of first needles.

10. The method of claim 9, wherein:

measuring voltage comprises measuring a composite voltage at a node to which the plurality of second needles are connected.

11. The method of claim 1, wherein:

the semiconductor device is a semiconductor device on a wafer;

the wafer is attached to a chuck; and

supplying current comprises inducing a current between the first needles and the chuck.

12. The method of claim 1, wherein:

regulating the current further comprises, equalizing the current supplied through each of the plurality of first needles.

13. The method of claim 12, wherein:

equalizing the current further comprises, dividing the current to generate the current supplied through each of the plurality of first needles.

14. The method of 1, further comprising: sensing a total current flow, wherein the sensed total current flow is used to adjust control signals to a plurality of current regulators based on a sensed total

current.

15. The method of claim 1, wherein the control loop comprises a comparator having a control output, the comparator configured to generate an output voltage based on a difference between the measured voltage and a voltage representation of the current through the first needle.

16. The method of claim 15, wherein the control loop further comprises a transistor having a control terminal coupled to the control output of the comparator, wherein the transistor is configured to regulate the current through the first needle based on the output voltage at the control output.

17. A device interface board configured to connect to a test system for testing a high current device, the device interface board comprising:

a plurality of connection points positioned to connect to a probe card, the plurality of connection points comprising a plurality of first connection points and at least one second connection point;

a current regulator, the current regulator comprising a plurality of outputs coupled to the plurality of first connection points; and

a conducting path positioned to couple the at least one second connection point to a measurement point on a test system, wherein

the current regulator is configured to regulate current flow through each of the plurality of first connection points based on a voltage at the measurement point, wherein

the current regulator comprises a plurality of circuits, each circuit comprises a control loop coupled to an output of the plurality of outputs, the control loop comprising a control input coupled to the voltage at the measurement point, and configured to regulate a current in the output based on the voltage.

18. The device interface board of claim 17, further comprising:

alarm circuitry that outputs an alarm when a contact resistance of a probe needle coupled to a connection point of the plurality of first connection points exceeds a threshold.

19. The device interface board of claim 17, wherein:

the at least one second connection point comprises a plurality of second connection points; and

the device interface board comprises conductive elements connecting the plurality of second connection points.

20. The device interface board of claim 17, wherein:

the current regulator is configured to regulate current through each of the plurality of first connection points with a tolerance of +/-1%.

21. The device interface board of claim 20, wherein:

the current regulator is configured to regulate current through each of the plurality of first connection points within a range of 0 Amps to 7 Amps.

22. The device interface board of claim 17, wherein the control loop comprises a comparator having a control output, the comparator configured to generate an output voltage based on a difference between the voltage and a voltage representation of the current in the output.

23. The device interface board of claim 22, wherein the control loop further comprises a transistor having a control terminal coupled to the control output of the comparator, wherein the transistor is configured to regulate the current in the output based on the output voltage at the control output.

24. A test system for testing a semiconductor device, the semiconductor device comprising a pad, the test system comprising:

a probe card comprising:

a plurality of needles comprising tips positioned to contact the pad, the plurality of needles comprising a plurality of first needles and at least one second needle:

a plurality of current control circuits, each current control circuit coupled to a first needle of the plurality of first needles: and

at least one voltage sense circuit coupled to the at least one second needle and configured to provide a sensed voltage, wherein:

the plurality of current control circuits are configured to regulate current in the plurality of first needles based on the sensed voltage, and wherein

each current control circuit comprises a control loop coupled to a first needle of the plurality of first needles, the control loop comprising a control input coupled to the sensed voltage, and configured to regulate a current in the first needle based on the sensed voltage.

25. The test system of claim 24, further comprising: a chuck; and

a processor coupled to receive a value indicative of voltage sensed by the at least one voltage sense circuit and to compute, based on the voltage sensed, an ON resistance of the semiconductor device, wherein the voltage is sensed between the pad and the chuck.

26. The test system of claim 25, wherein the chuck is configured to position a wafer comprising the semiconductor device in contact with the plurality of needles, wherein the chuck comprises a surface for receiving the wafer and the surface comprises gold plating.

27. The test system of claim 24, wherein the plurality of current control circuits are configured to generate an aggregate current through the plurality of first needles in excess of 10 Amps.

28. The test system of claim 27, wherein plurality of current control circuits are configured to generate a current through each of the plurality of first needles that differs by less than +/-2%.

29. The test system of claim 24, wherein:

the first plurality of needles comprise force needles and the at least one second needle comprises a sense needle.

30. The test system of claim 24, wherein:

the at least one second needle comprises a plurality of second needles; and

the plurality of second needles are connected to a single voltage sense circuit of the at least one voltage sense circuit.

31. The test system of claim 24, wherein the plurality of first needles are positioned with tips that are equi-resistant from a nearest tip of a needle of the at least one second needle.

32. The test system of claim 24, wherein the control loop comprises a comparator having a control output, the comparator configured to generate an output voltage based on a difference between the sensed voltage and a voltage representation of the current in the first needle.

33. The test system of claim 32, wherein the control loop further comprises a transistor having a control terminal coupled to the control output of the comparator, wherein the transistor is configured to regulate the current in the first needle based on the output voltage at the control output.

34. The test system of claim 24, wherein the plurality of control circuits are configured to equalize current through the plurality of first needles.