CLAIMS

1. A data processing apparatus, comprising:

at least two processing cores;

a synchronization scheduler, configured to generate and send a configuration signal in response to a program update signal from each of the processing cores connected to the synchronization scheduler; and

a direct memory access controller, configured to read a program corresponding to each of the processing cores from an external storage unit and send the program to the corresponding processing core, based on the configuration signal;

wherein the synchronization scheduler is further configured to, in response to the program update signal, send a synchronous operation signal to each of the processing cores connected to the synchronization scheduler, wherein the synchronous operation signal is sent to each of the processing cores after the synchronization scheduler receives a predetermined number of the program update signals, and the synchronous operation signal is configured to instruct each of the processing cores to start executing the corresponding program simultaneously.

2. The data processing apparatus according to claim 1, wherein

the program comprises a plurality of program segments.

3. The data processing apparatus according to claim 2, wherein

the processing cores are configured to send the program update signal to the synchronization scheduler after executing each of the program segments.

4. The data processing apparatus according to claim 2 or 3, wherein

the direct memory access controller is configured to read the program segment corresponding to each of the processing cores from the external storage unit, and send the program segments to the corresponding processing cores; and

the direct memory access controller is further configured to send a configuration completion signal to the synchronization scheduler after sending the program segments to the corresponding processing cores.

5. The data processing apparatus according to claim 4, wherein

the synchronization scheduler is further configured to, in response to the program update signal and the configuration completion signal, send the synchronous operation signal to each of the processing cores connected to the synchronization scheduler.

6. The data processing apparatus according to any of claims 1-5, wherein the synchronization scheduler comprises a counter configured to record the number of the program update signals received; and

the synchronization scheduler is further configured to prepare to send the synchronous operation signal in response to the number of the program update signals being equal to the predetermined number.

7. The data processing apparatus according to any of claims 1-6, wherein

the number of program segments executed by each of the processing cores is the same; and

the predetermined number is the number of the program segments, or the predetermined number is the product of the number of the processing cores connected to the synchronization scheduler and the number of the program segments.

8. The data processing apparatus according to any of claim 1-7, wherein the at least two processing cores comprise a first processing core and a second processing core; and

the first processing core and the second processing core execute different programs, and a computation result of the program executed by the first processing core is an input of the program executed by the second processing core.

9. A data processing method, comprising:

executing programs by processing cores;

generating and sending a configuration signal by a synchronization scheduler in response to a program update signal from each of the processing cores connected to the synchronization scheduler;

reading a program corresponding to each of the processing cores from an external storage unit and sending the program to the corresponding processing core by a direct memory access controller, based on the configuration signal; and

in response to the program update signal, sending a synchronous operation signal to each of the processing cores connected to the synchronization scheduler, wherein the synchronous operation signal is sent to each of the processing cores after the synchronization scheduler receives a predetermined number of the program update signals, and the synchronous operation signal is configured to instruct each of the processing cores to start executing the corresponding program simultaneously.