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NON-ANNULAR LANDS

BACKGROUND OF THE INVENTION

Early circuit board fabrication techniques involved connecting wires on the surface of the circuit board directly to through holes. Through holes, when plated with a conductive material, serve to connect the front and back surfaces of the circuit board. Unfortunately connecting wires directly to the through holes produced connections that had a high failure rate. The difference between the thermal expansion of the metal wire and the substrate lead to cracking, particularly at the juncture of the wire and the through hole. As a result, the electrical connection between the wire and the through hole was broken.

To overcome the failure rate of the connections, a land was created to connect the wire to a through hole. The land which is made of electrically conductive material, typically copper, is a circular or more specifically annular structure, that completely encircled the through hole. By providing lands the surface area of the connection between the

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through hole and the wire was significantly increased; this resulted in fewer failed connections.

Lands have been historically annular, to maximize the contact area between the edge of the plated through holes and the land. In addition, lands were circular in configuration to compensate for errors in drilling or photolithography that caused the lands to be offset from the through hole during the printed circuit board fabrication process.

In the quest for miniaturization of circuit boards and integrated circuit devices, designers have sought to place more and more electronic structures on the surface of circuit boards and devices. To accomplish this goal, designers require an ever increasing amount of space, that is "real estate," on the surface of a circuit board. In an attempt to increase the available "real estate", the diameter of conventional lands relative to the diameter of through holes was decreased. However, when the through holes were drilled, the drill bit often stripped the lands from the substrate, leaving an irregularity in the through hole which creates an unreliable plated through hole.

Indeed, as circuit board technology has developed, the land size has increased rather than decreased. Projections known as "flares" have been added to lands along the axis of the wire to further improve the reliability of the

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connection between the wire and the land. The addition of the flares to circular lands consumes even more real estate than the conventional lands.

It would be desirable to increase the available real estate on a substrate while preserving reliable connections between wires and through holes afforded by lands.

SUMMARY OF THE INVENTION

The present invention increases real estate by providing non-annular lands which do not completely encircle the through holes;, that is they do not extend 360° around the through hole. Preferably the non-annular lands contact no more than one side of the through holes thereby providing real estate not otherwise available using conventional lands. The present invention also relates to a method for producing such non-annular lands.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic diagram of a portion of a circuit board showing land configurations and wiring between holes of typical prior art configuration;

Figure 2 is a schematic diagram similar to Figure 1, showing the non-annular land of the present invention and wiring between holes;

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Figure 3 is a diagram showing the relationship of an non-annular land to a plated through hole;

Figure 4 is a plated through hole showing positioning of artwork in producing the non-annular land;

Figures 5, 6 and 7 show various wiring configurations with Non-annular lands of this invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention increases real estate by providing a new land shape while preserving reliable connections between through holes and wires. Instead of a 360° annular land which contacts the entire circumference of the plated through hole, the non-annular lands of the present invention contact only a portion, that is, less than 360° of the through holes. An non-annular land is positioned on the same side of the through hole as the wire that contacts the through hole and is preferably oval in shape.

By employing the non-annular land increased real estate is obtained. For example, referring to Figure 1, the conventional 360° annular lands 10 and the conventional 360° annular lands 12 with flares 14 can be seen connected to through holes 20 and 22. Where the through hole centers are spaced 0.05 inches apart, only two 0.004 inch wires 16 and 18

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can be accommodated in the space between through holes 20 and 22.

With reference to Figure 2, non-annular land 40 can be seen partially surrounding through hole 42. In the 0.05 inch space between the centers of through holes 42 and three 0.004 inch wires, wires 46, 48 and 50 may be accommodated. When epoxy-glass is the dielectric material used for the card, the minimum space between the wires, necessary to prevent shorts between the wires, is 2 mil. Thus the Non-annular lands provide a significant increase in real estate when compared to real estate available when using conventional lands.

Referring now to Figure 3, the preferred length of the non-annular land is preferably determined by calculating the offset distance d_o. The offset distance d_o represents the distance that the reticules, that is the preferred artwork, are offset from the center of the through hole during the photolithographic process.

The preferred offset distance d_o is determined by the following formula:

$$d_o = z + (r_h - r_I) + t_o - s$$

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wherein:

t_o is the tolerance of conductor generation process, that is the etching process (and t_o equals 0 where the tolerance is unknown);

s is the minimum spacing of conductor lines, also referred to herein as wires, which varies depending on the circuit board design;

z, is the minimum desired space between the nearest adjacent wire and the edge of the through hole 60;

r_h is the radius of through hole 60 as drilled;

r_I is the radius of the reticule used to form the non-annular land 62, preferably r_I is the same as r_H.

For example, in a system where: z is 6.5 r_h is 6 mil, s is desired to be a minimum of 2 mil, the t_o is 1.0 mil, r_I is 6 mil, then

$$d_o = 6.5 + (6 - 6) + 1.0 - 2.0$$

$$d_o = 5.5$$

Thus the center of the reticule should be offset 5.5 mil from the center of the through hole at the last exposure. Preferably between the first exposure in which the reticule is positioned over the intended through hole position, and the

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exposure at which the reticule is positioned 5.5 mil from the center of the through hole, the reticule is positioned at halfway or 2.75 mil from the center of the through hole and exposed.

As used herein, "length" refers to the dimension of the non-annular land along the axis of the wire connected to the non-annular land, as measured from the edge of the through hole to the edge of the wire. The non-annular land length is preferably 0.1 to 2 times, more preferably 0.5 to 0.75 times the value of z minus $(s + t_o)$. While the non-annular land length could exceed 2 times the value of z minus $(s + t_o)$, this defeats the objective of providing increased real estate. Smaller lengths, that is smaller than 0.1 times the value of z minus $(s + t_o)$ result in an increased rate of failure for connections, and are less preferred. Typically, when such lengths smaller than 0.1 times the value of z minus $(s + t_o)$ are employed, there is not enough dielectric material between the non-annular land and the adjacent wire so that a short occurs between the non-annular land and the adjacent wire.

The width of the non-annular land is the dimension of the land along the direction perpendicular to the length of the land. The width of the non-annular land is greater than the width of the wire. While the width of the Non-annular land may exceed the width of the drilled through hole.

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Preferably, the width of the Non-annular land is less than or equal to the drilled through hole width.

The lands are made of the same material as the wires, which are typically copper.

Producing the non-annular land

First the artwork is formed employing conventional photolithographic techniques. The image of the desired non-annular land is exposed on a photo-sensitive emulsion carrier on glass or other transparent substrate. The preferred method for forming the non-annular land is shown in Figure 4. A conventional circular reticule is centered, at the position corresponding to (x, y), which is the center of where the through hole is to be drilled. The emulsion is exposed to light, preferably UV light. Then the reticule is offset from the through hole center by the offset distance d_o calculated using the above Formulae. Thus, the reticule is centered at position corresponding to $(x + d_o/2, y)$ and exposed. Preferably, to obtain an even longer Non-annular land, the reticule is positioned at position corresponding to $(x + d_o, y)$ and exposed a second time. Thereafter the emulsion carrier is developed. Typically, the non-annular land need only be large enough to allow the actual through hole to be positioned at the minimum adjacent conductor spacing.

Alternatively, the custom artwork, that is, the exposure mask formed in the desired shape of the non-annular

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land may be used, rather than forming the artwork using a conventional circular reticule.

The artwork is then used in a traditional printed circuit photoimaging process, in which a photoimageable resist is applied to a substrate, and exposed to actinic radiation through the artwork. The photoresist is conventionally developed using conventional processes to form the desired pattern. Preferably subtractive processes are used in which the photoresist when developed, forms the final non-annular land shape. The unexposed photoresist is removed by conventional solvents, leaving the exposed photoresist in the desired pattern. An etchant is then used to remove metal not protected by exposed photoresist. The exposed photoresist is stripped leaving the final conductive pattern including the desired non-annular lands.

Alternatively, or additionally, conventional additive processes may be used. In such additive processes, the spaces between the photoresist, when developed, define the circuitization pattern. The circuitization is then formed in such spaces by conventional methods such as by additive plating. After the plating, the photoresist is stripped leaving the final conductive pattern including the desired non-annular lands.

Upon assembly of the "core" substrate into a composite structure, the cores are registered, that is

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aligned, to make the proper connection to the required layers. The assembly is then drilled to form the desired through holes and through holes are conventionally plated typically using electrolytic or electroless copper plating. Alternatively, the through holes may be filled with conductive paste. As a result, the plated through hole contacts the non-annular land as shown in Figure 3.

Example 1

A thin light card having an minimum spacing between lines of 2 mils and containing the non-annular land of the present invention was prepared as follows. A circular opaque reticule having a diameter of 0.011 inches was placed on a photosensitive emulsion which was deposited on a transparent substrate to create the artwork. The reticule was placed at centers of desired through holes and exposed to ultraviolet light. The reticules were offset by 3 mils from hole center, exposed, offset a second time by 3 mils and exposed. The reticules were removed and the emulsion developed to produce artwork. A conventional negative photoresist available under the name "Resiston" from DuPont Chemical Company was applied to 0.0014 inches layer of copper disposed on a card having grid dimensions of 0.050 x 0.025 inches. The photoresist was exposed to actinic radiation through the artwork and conventionally developed. The card was etched to define the

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Lands, then the photoresist was stripped. After completing several conventional fabrication steps including lamination, pinning and registration, the through holes were drilled using a 0.010 inch drill bit. The through holes were conventionally plated using electrolytic copper plating, to provide through holes having a diameter of 0.008 inches and a Land having a width of 0.010 inches and a length of 0.006 inches. The wiring pattern for a portion of the card is shown in Figure 5.

Example 2

A card having an s value of 2 mils and containing the non-annular land of the present invention was prepared as follows. A circular opaque reticule having a diameter of 0.009 inches was placed on a photosensitive emulsion which was deposited on a transparent substrate to create artwork. The reticule was placed at centers of desired through holes and exposed to ultraviolet light. The reticules were offset by 3 mils from the through hole center, exposed, offset a second time by 3 mils and exposed. The reticules were removed and the emulsion developed to produce artwork. A conventional negative photoresist available under the name Resiston from Dupont was applied to 0.0014 inch layer of copper disposed on a card having grid dimensions of 0.050 x 0.025 inches. The photoresist was exposed to actinic radiation through the artwork, and conventionally developed. The card was etched to

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define the Lands, then the photoresist was stripped. Next, the through holes were drilled using a 0.008 inch drill bit. The through holes were conventionally plated using electrolytic copper plating, to provide through holes having a diameter of 0.006 inches and a Land having an width of 0.008 inches and an length of 0.006 inches. The wiring pattern is shown in Figure 6.

Example 3

A card containing an non-annular land of the present invention was prepared as follows. A circular opaque reticule having a diameter of 0.011 inches was placed on a photosensitive emulsion which was deposited on a transparent substrate to create artwork. The reticule was placed at centers of desired through holes and exposed to ultraviolet light. The reticules were offset by 3 mils from the through hole center, exposed and offset a second time by 3 mils and exposed. The reticules were removed and the emulsion developed to produce artwork. A conventional negative photoresist available under the name "Resiston" from Dupont Chemical Company, was applied to 0.0014 inch layer of copper disposed on card having grid dimensions of 0.050 x 0.025 inches. The photoresist was exposed to actinic radiation through the artwork, and conventionally developed. The card was etched to define the Lands, then the photoresist was

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holes were drilled using a 0.010 inch drill bit. The through holes were conventionally plated using electrolytic copper plating, to provide through holes having a diameter of 0.008 inches and a Land having a width of 0.010 inches and a length of 0.006 inches. The wiring diagram is shown in Figure 7.

Evaluation of the non-annular lands

As shown in Figure 1, by using the non-annular lands the real estate is increased between through holes that are spaced 50 mils apart. As a result, this permits room for a third wire having a width of 0.004 inches to be added in addition to the other two wires thereby increasing the wireability density by 50%. In turn, this increased wiring capability on one surface, permits the number of wiring planes required, to be reduced in certain applications.

The reliability of the wire connections was determined by subjecting the cards to a simulated card assembly process. The cards were subjected to accelerated thermal cycling and insulation resistance tests to simulate the power on hours and thermal cycles associated with the on off cycling. There were no failures of the Non-annular lands.

Although certain embodiment of this invention have been shown and described, various adaptations and modifications can be made without departing from the scope of the invention as defined in the appended claims.

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CLAIMS:

1. In a circuit board having disposed thereon a wire, and at least one through hole which has an electrically conductive material disposed therein, the improvement comprising a land, partially surrounding the through hole and in connection with the conductive material and the wire.

2. A land as claimed in Claim 1, wherein the width of the land ranges from greater than the wire width to less than or equal to the through hole width.

3. A land as claimed in Claim 1, further comprising a second wire adjacent to the through hole having a length of from 0.1 to 2 times $z - (t_o + s)$, wherein z is the minimum desired space between the edge of the through hole and the adjacent wire and s is the minimum desired spacing of the conductor lines, and t_o is the tolerance of the etch process or 0.

4. A land as claimed in Claim 2, having a length of from 0.1 to 2 times $z - t_o + s$, wherein z is the minimum desired space between the edge of the through hole and the adjacent wire and s is the minimum desired spacing of the conductor lines, and t_o is the tolerance of the etch process or 0.

5. A land as claimed in any one of Claims 1-4, wherein the electrically conductive material comprises plated metal.

6. A land as claimed in any one of Claims 1-4, wherein the electrically conductive material comprises paste.

7. A land for a printed circuit board, said land being substantially as herein described with reference to Figs 2-7 of the accompanying drawings.

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8. A circuit board including a land as claimed in any one of Claims 1-7.

9. A circuit board having a portion thereof which is substantially as herein described with reference to any one of Figs 5-7 of the accompanying drawings.

10. A method for forming a land in a circuit board, said method comprising the steps of,

a. providing a substrate having wires disposed thereon;

b. providing positions for through holes in the substrate;

c. forming metal on the substrate over the positions for the through holes;

d. drilling through the metal at the desired through hole locations to provide through holes; and

e. disposing conductive material in said through holes;

to thereby provide lands which partially surround said through holes and which serve to connect the wire to the conductive material in the through hole.

11. The method as claimed in Claim 10, wherein the conductive material comprises plated metal.

12. The method as claimed in Claim 10, wherein the conductive material comprises electrically conductive paste.

13. The method as claimed in any one of Claims 10-12, wherein the length of the land is determined by the following formula $d_o = z + (r_h - r_I) + t_o - s$, wherein in z is the minimum desired space between the edge of the through hole and the nearest adjacent wire, t_o is the tolerance of the etch process or o, r_h is the radius of the through hole, r_I is the radius of the reticule used to form the Non-annular land, and d_o is the offset distance of the reticule.

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14. The method as claimed in any one of Claims 10-12, wherein the land has a length from 0.1 to 2 times $z + t_o - s$, wherein z is the minimum desired space between the edge of the through hole and the nearest adjacent wire and s is the minimum desired spacing of the conductor lines, and t_o is the tolerance of the etch process or 0.

15. The method as claimed in any one of Claims 10-12, wherein the width of the land ranges from greater than the wire width to less than or equal to the through hole width.

16. A method for forming a land in a circuit board, said method being substantially as herein described with reference to Figs 2-7 of the accompanying drawings.

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NON-ANNULAR LANDS

ABSTRACT:

The present invention discloses non-annular lands 40 which increase the available real estate on printed circuit boards. The non-annular lands 40 do not completely encircle the through holes 42. The non-annular lands 40 are non-annular, that is they do not extend 360° around the through hole 42. Preferably the non-annular lands contact no more than one side of the through holes 42 thereby providing real estate not otherwise available using conventional lands 10. The present invention also relates to a method for producing such non-annular lands 42.

Fig. 2

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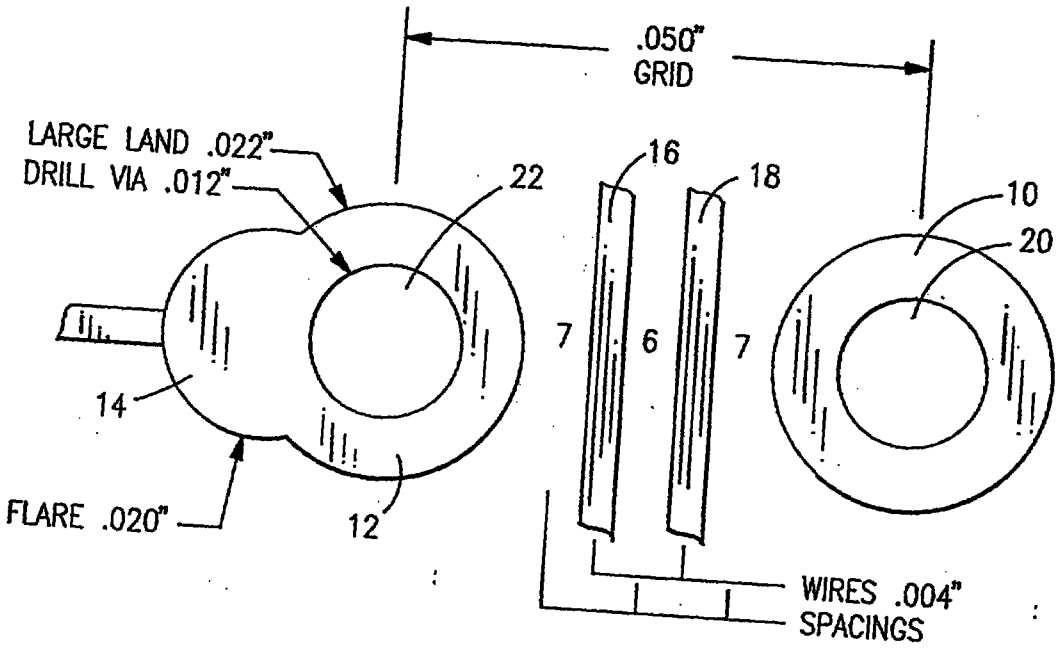
.050"
GRID
LARGE LAND .022"
DRILL VIA .012"
22
16
18
10
20
7
6
7
14
FLARE .020"
12
WIRES .004"
SPACINGS

FIG.1

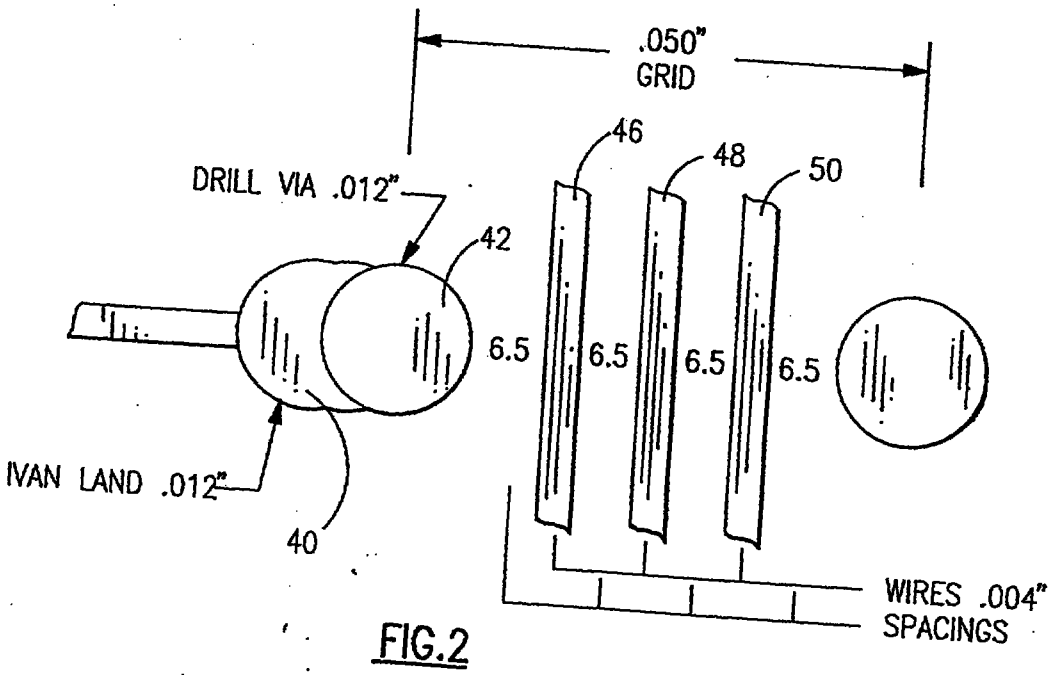
.050"
GRID
46
48
50
DRILL VIA .012"
42
6.5
6.5
6.5
6.5
IVAN LAND .012"
40
WIRES .004"
SPACINGS

FIG.2

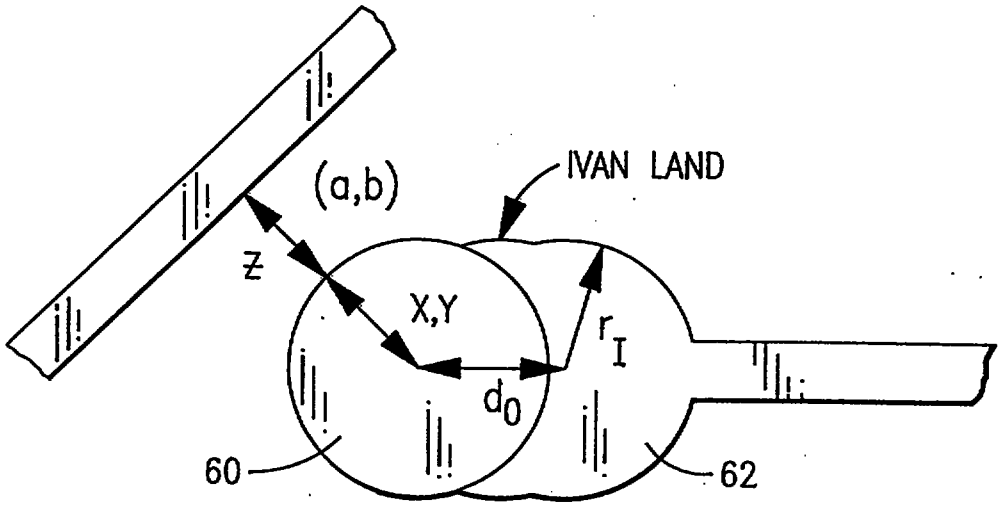

FIG.3

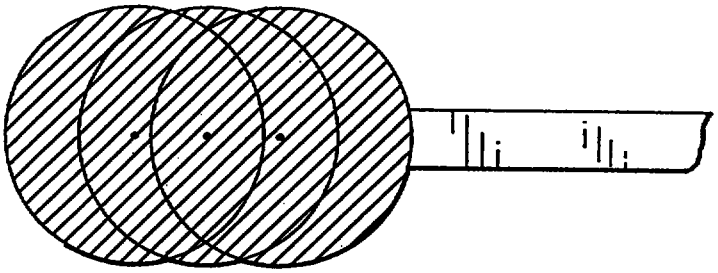

FIG.4

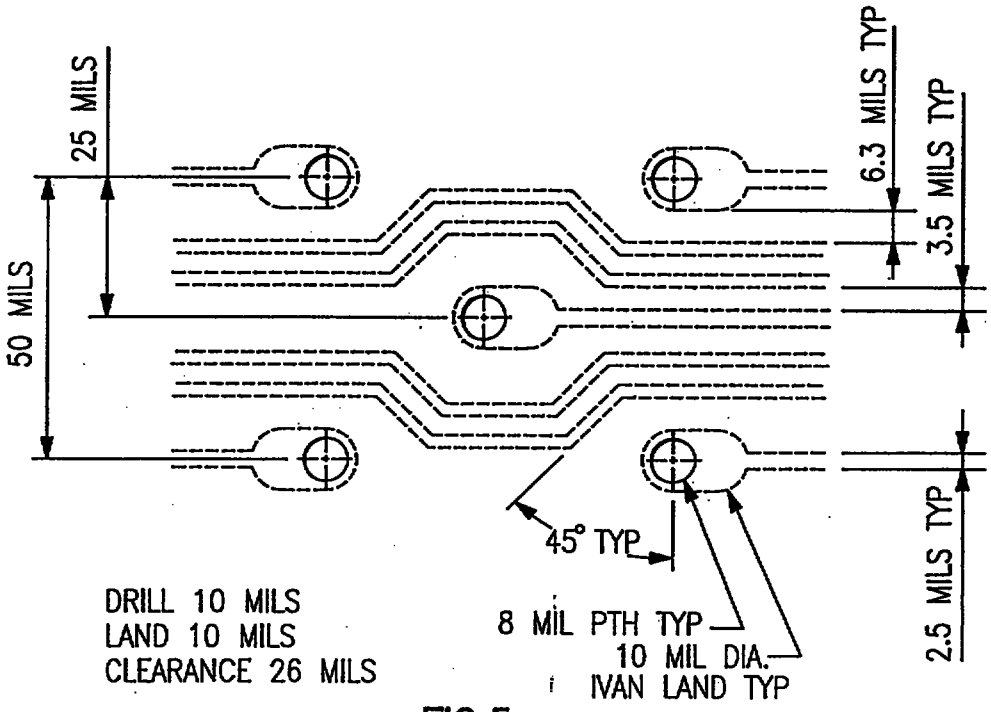
25 MILS
50 MILS
6.3 MILS TYP
3.5 MILS TYP
2.5 MILS TYP
45° TYP
8 MIL PTH TYP
10 MIL DIA.
IVAN LAND TYP
DRILL 10 MILS
LAND 10 MILS
CLEARANCE 26 MILS

FIG.5

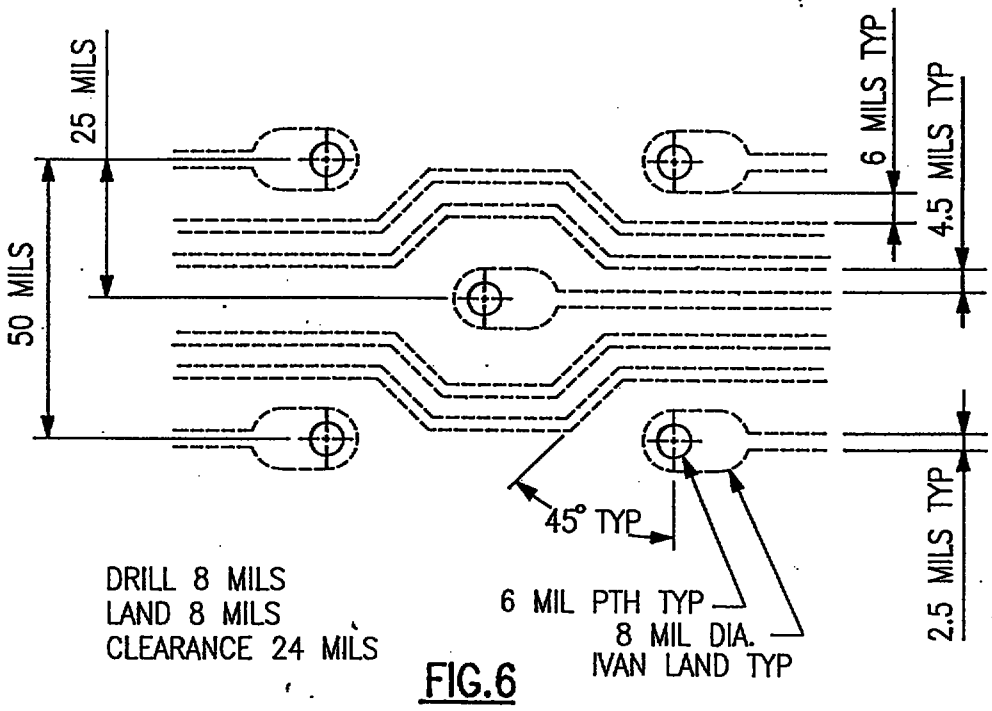
25 MILS
50 MILS
6 MILS TYP
4.5 MILS TYP
2.5 MILS TYP
45° TYP
6 MIL PTH TYP
8 MIL DIA.
IVAN LAND TYP
DRILL 8 MILS
LAND 8 MILS
CLEARANCE 24 MILS

FIG.6

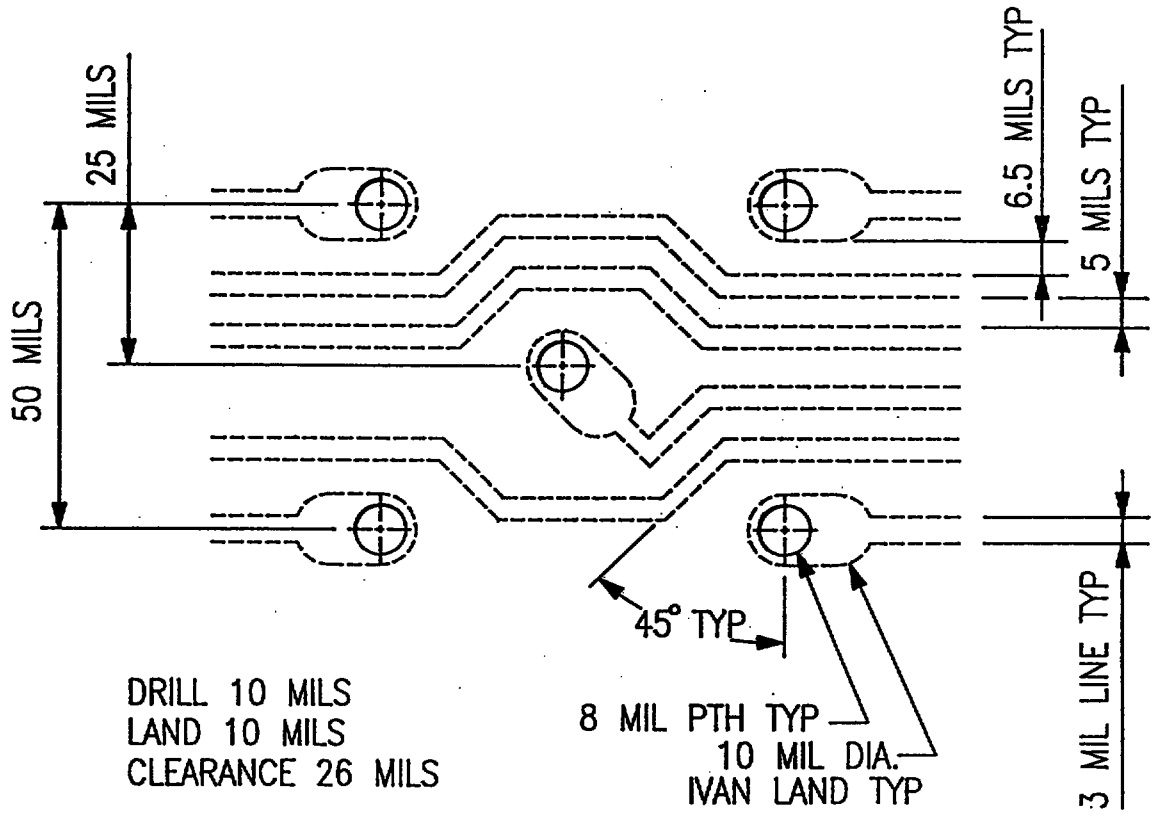
25 MILS
50 MILS
6.5 MILS TYP
5 MILS TYP
3 MIL LINE TYP
45° TYP
DRILL 10 MILS
LAND 10 MILS
CLEARANCE 26 MILS
8 MIL PTH TYP
10 MIL DIA.
IVAN LAND TYP

FIG.7

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NON-ANNULAR LANDS

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To overcome the failure rate of the connections, a land was created to connect the wire to a through hole. The land which is made of electrically conductive material, typically copper, is a circular or more specifically annular structure, that completely encircled the through hole. By providing lands the surface area of the connection between the

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Lands have been historically annular, to maximize the contact area between the edge of the plated through holes and the land. In addition, lands were circular in configuration to compensate for errors in drilling or photolithography that caused the lands to be offset from the through hole during the printed circuit board fabrication process.

In the quest for miniaturization of circuit boards and integrated circuit devices, designers have sought to place more and more electronic structures on the surface of circuit boards and devices. To accomplish this goal, designers require an ever increasing amount of space, that is "real estate," on the surface of a circuit board. In an attempt to increase the available "real estate", the diameter of conventional lands relative to the diameter of through holes was decreased. However, when the through holes were drilled, the drill bit often stripped the lands from the substrate, leaving an irregularity in the through hole which creates an unreliable plated through hole.

Indeed, as circuit board technology has developed, the land size has increased rather than decreased. Projections known as "flares" have been added to lands along the axis of the wire to further improve the reliability of the

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connection between the wire and the land. The addition of the flares to circular lands consumes even more real estate than the conventional lands.

It would be desirable to increase the available real estate on a substrate while preserving reliable connections between wires and through holes afforded by lands.

SUMMARY OF THE INVENTION

The present invention increases real estate by providing non-annular lands which do not completely encircle the through holes;, that is they do not extend 360° around the through hole. Preferably the non-annular lands contact no more than one side of the through holes thereby providing real estate not otherwise available using conventional lands. The present invention also relates to a method for producing such non-annular lands.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic diagram of a portion of a circuit board showing land configurations and wiring between holes of typical prior art configuration;

Figure 2 is a schematic diagram similar to Figure 1, showing the non-annular land of the present invention and wiring between holes;

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Figure 3 is a diagram showing the relationship of an non-annular land to a plated through hole;

Figure 4 is a plated through hole showing positioning of artwork in producing the non-annular land;

Figures 5, 6 and 7 show various wiring configurations with Non-annular lands of this invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention increases real estate by providing a new land shape while preserving reliable connections between through holes and wires. Instead of a 360° annular land which contacts the entire circumference of the plated through hole, the non-annular lands of the present invention contact only a portion, that is, less than 360° of the through holes. An non-annular land is positioned on the same side of the through hole as the wire that contacts the through hole and is preferably oval in shape.

By employing the non-annular land increased real estate is obtained. For example, referring to Figure 1, the conventional 360° annular lands 10 and the conventional 360° annular lands 12 with flares 14 can be seen connected to through holes 20 and 22. Where the through hole centers are spaced 0.05 inches apart, only two 0.004 inch wires 16 and 18

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can be accommodated in the space between through holes 20 and 22.

With reference to Figure 2, non-annular land 40 can be seen partially surrounding through hole 42. In the 0.05 inch space between the centers of through holes 42 and three 0.004 inch wires, wires 46, 48 and 50 may be accommodated. When epoxy-glass is the dielectric material used for the card, the minimum space between the wires, necessary to prevent shorts between the wires, is 2 mil. Thus the Non-annular lands provide a significant increase in real estate when compared to real estate available when using conventional lands.

Referring now to Figure 3, the preferred length of the non-annular land is preferably determined by calculating the offset distance d_o. The offset distance d_o represents the distance that the reticules, that is the preferred artwork, are offset from the center of the through hole during the photolithographic process.

The preferred offset distance d_o is determined by the following formula:

$$d_o = z + (r_h - r_I) + t_o - s$$

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wherein:

t_o is the tolerance of conductor generation process, that is the etching process (and t_o equals 0 where the tolerance is unknown);

s is the minimum spacing of conductor lines, also referred to herein as wires, which varies depending on the circuit board design;

z, is the minimum desired space between the nearest adjacent wire and the edge of the through hole 60;

r_h is the radius of through hole 60 as drilled;

r_I is the radius of the reticule used to form the non-annular land 62, preferably r_I is the same as r_H.

For example, in a system where: z is 6.5 r_h is 6 mil, s is desired to be a minimum of 2 mil, the t_o is 1.0 mil, r_I is 6 mil, then

$$d_o = 6.5 + (6 - 6) + 1.0 - 2.0$$

$$d_o = 5.5$$

Thus the center of the reticule should be offset 5.5 mil from the center of the through hole at the last exposure. Preferably between the first exposure in which the reticule is positioned over the intended through hole position, and the

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exposure at which the reticule is positioned 5.5 mil from the center of the through hole, the reticule is positioned at halfway or 2.75 mil from the center of the through hole and exposed.

As used herein, "length" refers to the dimension of the non-annular land along the axis of the wire connected to the non-annular land, as measured from the edge of the through hole to the edge of the wire. The non-annular land length is preferably 0.1 to 2 times, more preferably 0.5 to 0.75 times the value of z minus ($s + t_o$). While the non-annular land length could exceed 2 times the value of z minus ($s + t_o$), this defeats the objective of providing increased real estate. Smaller lengths, that is smaller than 0.1 times the value of z minus ($s + t_o$) result in an increased rate of failure for connections, and are less preferred. Typically, when such lengths smaller than 0.1 times the value of z minus ($s + t_o$) are employed, there is not enough dielectric material between the non-annular land and the adjacent wire so that a short occurs between the non-annular land and the adjacent wire.

The width of the non-annular land is the dimension of the land along the direction perpendicular to the length of the land. The width of the non-annular land is greater than the width of the wire. While the width of the Non-annular land may exceed the width of the drilled through hole.

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Preferably, the width of the Non-annular land is less than or equal to the drilled through hole width.

The lands are made of the same material as the wires, which are typically copper.

Producing the non-annular land

First the artwork is formed employing conventional photolithographic techniques. The image of the desired non-annular land is exposed on a photo-sensitive emulsion carrier on glass or other transparent substrate. The preferred method for forming the non-annular land is shown in Figure 4. A conventional circular reticule is centered, at the position corresponding to (x, y), which is the center of where the through hole is to be drilled. The emulsion is exposed to light, preferably UV light. Then the reticule is offset from the through hole center by the offset distance d_o calculated using the above Formulae. Thus, the reticule is centered at position corresponding to $(x + d_o/2, y)$ and exposed. Preferably, to obtain an even longer Non-annular land, the reticule is positioned at position corresponding to $(x + d_o, y)$ and exposed a second time. Thereafter the emulsion carrier is developed. Typically, the non-annular land need only be large enough to allow the actual through hole to be positioned at the minimum adjacent conductor spacing.

Alternatively, the custom artwork, that is, the exposure mask formed in the desired shape of the non-annular

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land may be used, rather than forming the artwork using a conventional circular reticule.

The artwork is then used in a traditional printed circuit photoimaging process, in which a photoimageable resist is applied to a substrate, and exposed to actinic radiation through the artwork. The photoresist is conventionally developed using conventional processes to form the desired pattern. Preferably subtractive processes are used in which the photoresist when developed, forms the final non-annular land shape. The unexposed photoresist is removed by conventional solvents, leaving the exposed photoresist in the desired pattern. An etchant is then used to remove metal not protected by exposed photoresist. The exposed photoresist is stripped leaving the final conductive pattern including the desired non-annular lands.

Alternatively, or additionally, conventional additive processes may be used. In such additive processes, the spaces between the photoresist, when developed, define the circuitization pattern. The circuitization is then formed in such spaces by conventional methods such as by additive plating. After the plating, the photoresist is stripped leaving the final conductive pattern including the desired non-annular lands.

Upon assembly of the "core" substrate into a composite structure, the cores are registered, that is

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aligned, to make the proper connection to the required layers. The assembly is then drilled to form the desired through holes and through holes are conventionally plated typically using electrolytic or electroless copper plating. Alternatively, the through holes may be filled with conductive paste. As a result, the plated through hole contacts the non-annular land as shown in Figure 3.

Example 1

A thin light card having an minimum spacing between lines of 2 mils and containing the non-annular land of the present invention was prepared as follows. A circular opaque reticule having a diameter of 0.011 inches was placed on a photosensitive emulsion which was deposited on a transparent substrate to create the artwork. The reticule was placed at centers of desired through holes and exposed to ultraviolet light. The reticules were offset by 3 mils from hole center, exposed, offset a second time by 3 mils and exposed. The reticules were removed and the emulsion developed to produce artwork. A conventional negative photoresist available under the name "Resiston" from DuPont Chemical Company was applied to 0.0014 inches layer of copper disposed on a card having grid dimensions of 0.050 x 0.025 inches. The photoresist was exposed to actinic radiation through the artwork and conventionally developed. The card was etched to define the

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Lands, then the photoresist was stripped. After completing several conventional fabrication steps including lamination, pinning and registration, the through holes were drilled using a 0.010 inch drill bit. The through holes were conventionally plated using electrolytic copper plating, to provide through holes having a diameter of 0.008 inches and a Land having a width of 0.010 inches and a length of 0.006 inches. The wiring pattern for a portion of the card is shown in Figure 5.

Example 2

A card having an s value of 2 mils and containing the non-annular land of the present invention was prepared as follows. A circular opaque reticule having a diameter of 0.009 inches was placed on a photosensitive emulsion which was deposited on a transparent substrate to create artwork. The reticule was placed at centers of desired through holes and exposed to ultraviolet light. The reticules were offset by 3 mils from the through hole center, exposed, offset a second time by 3 mils and exposed. The reticules were removed and the emulsion developed to produce artwork. A conventional negative photoresist available under the name Resiston from Dupont was applied to 0.0014 inch layer of copper disposed on a card having grid dimensions of 0.050 x 0.025 inches. The photoresist was exposed to actinic radiation through the artwork, and conventionally developed. The card was etched to

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define the Lands, then the photoresist was stripped. Next, the through holes were drilled using a 0.008 inch drill bit. The through holes were conventionally plated using electrolytic copper plating, to provide through holes having a diameter of 0.006 inches and a Land having an width of 0.008 inches and an length of 0.006 inches. The wiring pattern is shown in Figure 6.

Example 3

A card containing an non-annular land of the present invention was prepared as follows. A circular opaque reticule having a diameter of 0.011 inches was placed on a photosensitive emulsion which was deposited on a transparent substrate to create artwork. The reticule was placed at centers of desired through holes and exposed to ultraviolet light. The reticules were offset by 3 mils from the through hole center, exposed and offset a second time by 3 mils and exposed. The reticules were removed and the emulsion developed to produce artwork. A conventional negative photoresist available under the name "Resiston" from Dupont Chemical Company, was applied to 0.0014 inch layer of copper disposed on card having grid dimensions of 0.050 x 0.025 inches. The photoresist was exposed to actinic radiation through the artwork, and conventionally developed. The card was etched to define the Lands, then the photoresist was

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holes were drilled using a 0.010 inch drill bit. The through holes were conventionally plated using electrolytic copper plating, to provide through holes having a diameter of 0.008 inches and a Land having a width of 0.010 inches and a length of 0.006 inches. The wiring diagram is shown in Figure 7.

Evaluation of the non-annular lands

As shown in Figure 1, by using the non-annular lands the real estate is increased between through holes that are spaced 50 mils apart. As a result, this permits room for a third wire having a width of 0.004 inches to be added in addition to the other two wires thereby increasing the wireability density by 50%. In turn, this increased wiring capability on one surface, permits the number of wiring planes required, to be reduced in certain applications.

The reliability of the wire connections was determined by subjecting the cards to a simulated card assembly process. The cards were subjected to accelerated thermal cycling and insulation resistance tests to simulate the power on hours and thermal cycles associated with the on off cycling. There were no failures of the Non-annular lands.

Although certain embodiment of this invention have been shown and described, various adaptations and modifications can be made without departing from the scope of the invention as defined in the appended claims.

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CLAIMS:

1. In a circuit board having disposed thereon a wire, and at least one through hole which has an electrically conductive material disposed therein, the improvement comprising a land, partially surrounding the through hole and in connection with the conductive material and the wire.

2. A land as claimed in Claim 1, wherein the width of the land ranges from greater than the wire width to less than or equal to the through hole width.

3. A land as claimed in Claim 1, further comprising a second wire adjacent to the through hole having a length of from 0.1 to 2 times $z - (t_o + s)$, wherein z is the minimum desired space between the edge of the through hole and the adjacent wire and s is the minimum desired spacing of the conductor lines, and t_o is the tolerance of the etch process or 0.

4. A land as claimed in Claim 2, having a length of from 0.1 to 2 times $z - t_o + s$, wherein z is the minimum desired space between the edge of the through hole and the adjacent wire and s is the minimum desired spacing of the conductor lines, and t_o is the tolerance of the etch process or 0.

5. A land as claimed in any one of Claims 1-4, wherein the electrically conductive material comprises plated metal.

6. A land as claimed in any one of Claims 1-4, wherein the electrically conductive material comprises paste.

7. A land for a printed circuit board, said land being substantially as herein described with reference to Figs 2-7 of the accompanying drawings.

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8. A circuit board including a land as claimed in any one of Claims 1-7.

9. A circuit board having a portion thereof which is substantially as herein described with reference to any one of Figs 5-7 of the accompanying drawings.

10. A method for forming a land in a circuit board, said method comprising the steps of,

a. providing a substrate having wires disposed thereon;

b. providing positions for through holes in the substrate;

c. forming metal on the substrate over the positions for the through holes;

d. drilling through the metal at the desired through hole locations to provide through holes; and

e. disposing conductive material in said through holes;

to thereby provide lands which partially surround said through holes and which serve to connect the wire to the conductive material in the through hole.

11. The method as claimed in Claim 10, wherein the conductive material comprises plated metal.

12. The method as claimed in Claim 10, wherein the conductive material comprises electrically conductive paste.

13. The method as claimed in any one of Claims 10-12, wherein the length of the land is determined by the following formula $d_o = z + (r_h - r_I) + t_o - s$, wherein in z is the minimum desired space between the edge of the through hole and the nearest adjacent wire, t_o is the tolerance of the etch process or o, r_h is the radius of the through hole, r_I is the radius of the reticule used to form the Non-annular land, and d_o is the offset distance of the reticule.

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14. The method as claimed in any one of Claims 10-12, wherein the land has a length from 0.1 to 2 times $z + t_o - s$, wherein z is the minimum desired space between the edge of the through hole and the nearest adjacent wire and s is the minimum desired spacing of the conductor lines, and t_o is the tolerance of the etch process or 0.

15. The method as claimed in any one of Claims 10-12, wherein the width of the land ranges from greater than the wire width to less than or equal to the through hole width.

16. A method for forming a land in a circuit board, said method being substantially as herein described with reference to Figs 2-7 of the accompanying drawings.

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NON-ANNULAR LANDS

ABSTRACT:

The present invention discloses non-annular lands 40 which increase the available real estate on printed circuit boards. The non-annular lands 40 do not completely encircle the through holes 42. The non-annular lands 40 are non-annular, that is they do not extend 360° around the through hole 42. Preferably the non-annular lands contact no more than one side of the through holes 42 thereby providing real estate not otherwise available using conventional lands 10. The present invention also relates to a method for producing such non-annular lands 42.

Fig. 2

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CLAIMS:

1. In a circuit board having disposed thereon a wire, and at least one through hole which has an electrically conductive material disposed therein, the improvement comprising a land, partially surrounding the through hole and in connection with the conductive material and the wire.

2. A land as claimed in Claim 1, wherein the width of the land ranges from greater than the wire width to less than or equal to the through hole width.

3. A land as claimed in Claim 1, further comprising a second wire adjacent to the through hole having a length of from 0.1 to 2 times $(z - (t_o + s))$, wherein z is the minimum desired space between the edge of the through hole and the adjacent wire and s is the minimum desired spacing of the conductor lines, and t_o is the tolerance of the etch process or 0.

4. A land as claimed in Claim 2, having a length of from 0.1 to 2 times $(Z-(t_o + s))$, wherein z is the minimum desired space between the edge of the through hole and the adjacent wire and s is the minimum desired spacing of the conductor lines, and t_o is the tolerance of the etch process or 0.

5. A land as claimed in any one of Claims 1-4, wherein the electrically conductive material comprises plated metal.

6. A land as claimed in any one of Claims 1-4, wherein the electrically conductive material comprises paste.

7. A land for a printed circuit board, said land being substantially as herein described with reference to Figs 2-7 of the accompanying drawings.

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9. A circuit board having a portion thereof which is substantially as herein described with reference to any one of Figs 5-7 of the accompanying drawings.

10. A method for forming a land in a circuit board, said method comprising the steps of,

a. providing a substrate having wires disposed thereon;

b. providing positions for through holes in the substrate;

c. forming metal on the substrate over the positions for the through holes;

d. drilling through the metal at the desired through hole locations to provide through holes; and

e. disposing conductive material in said through holes;

to thereby provide lands which partially surround said through holes and which serve to connect the wire to the conductive material in the through hole.

11. The method as claimed in Claim 10, wherein the conductive material comprises plated metal.

12. The method as claimed in Claim 10, wherein the conductive material comprises electrically conductive paste.

13. The method as claimed in any one of Claims 10-12, wherein the length of the land is determined by the following formula $d_o = z + (r_h - r_I) + t_o - s$, wherein in z is the minimum desired space between the edge of the through hole and the nearest adjacent wire, t_o is the tolerance of the etch process or o, r_h is the radius of the through hole, r_I is the radius of the reticule used to form the Non-annular land, and d_o is the offset distance of the reticule.

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15. The method as claimed in any one of Claims 10-12, wherein the width of the land ranges from greater than the wire width to less than or equal to the through hole width.

16. A method for forming a land in a circuit board, said method being substantially as herein described with reference to Figs 2-7 of the accompanying drawings.

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connection between the wire and the land. The addition of the flares to circular lands consumes even more real estate than the conventional lands.

It would be desirable to increase the available real estate on a substrate while preserving reliable connections between wires and through holes afforded by lands.

SUMMARY OF THE INVENTION

According to one aspect of the invention there is disclosed a circuit board having disposed thereon a wire, and at least one through hole which has an electrically conductive material disposed therein, the circuit board further comprising a land, partially surrounding the through hole and in connection with the conductive material and the wire.

According to another aspect there is disclosed a land included in such a circuit board.

According to still another aspect of the invention there is disclosed a method for forming a circuit board, said method comprising the steps of:

a. providing a substrate having wires disposed thereon;

b. providing positions for through holes in the substrate;

c. forming metal on the substrate over the positions for the through holes;

d. drilling through the metal at the desired through hole locations to provide through holes; and

e. disposing conductive material in said through holes;

to thereby provide a circuit board having lands which partially surround said through holes and which serve to connect the wire to the conductive material in the through hole.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic diagram of a portion of a circuit board showing land configurations and wiring between holes of typical prior art configuration;

Figure 2 is a schematic diagram similar to Figure 1, shown the non-annular land of the present invention and wiring between holes;

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CLAIMS:

1. A circuit board having disposed thereon a wire, and at least one through hole which has an electrically conductive material disposed therein, the circuit board further comprising a land, partially surrounding the through hole and in connection with the conductive material and the wire.

2. A circuit board as claimed in claim 1, the width of the land ranges from greater than the wire width to less than or equal to the through hole width.

3. A circuit board as claimed in claim 1, further comprising a second wire adjacent to the through hole having a length of from 0.1 to 2 times $(z - (t_o + s))$, wherein z is the minimum desired space between the edge of the through hole and the adjacent wire and s is the minimum desired spacing of the conductor lines, and t_o is the tolerance of the etch process or 0.

4. A circuit board as claimed in claim 2, having a length of from 0.1 to 2 times $(z-(t_o + s))$, wherein z is the minimum desired space between the edge of the through hole and the adjacent wire and s is the minimum desired spacing of the conductor lines, and t_o is the tolerance of the etch process or 0.

5. A circuit board as claimed in any one of claims 1-4, wherein the electrically conductive material comprises plated metal.

6. A circuit board as claimed in any one of claims 1-4, wherein the electrically conductive material comprises paste.

7. A circuit board being substantially as herein described with reference to Figs. 2-7 of the accompanying drawings.

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8. A land included in a circuit board as claimed in any one of claims 1-7.

9. A circuit board having a portion thereof which is substantially as herein described with reference to any one of Figs. 5-7 of the accompanying drawings.

10. A method for forming a circuit board, said method comprising the steps of:

a. providing a substrate having wires disposed thereon;

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13. The method as claimed in any one of claims 10-12, wherein the length of the land is determined by the following formula $d_o = z + (r_h - r_I) + t_o - s$, wherein z is the minimum desired space between the edge of the through hole and the nearest adjacent wire, t_o is the tolerance of the etch process or o, r_h is the radius of the through hole, r_I is the radius of the reticule used to form the Non-annular land, and d_o is the offset distance of the reticule.

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According to another aspect there is disclosed a land included in such a circuit board.

According to still another aspect of the invention there is disclosed a method for forming a circuit board, said method comprising the steps of:

a. providing a substrate having wires disposed thereon;

b. providing positions for through holes in the substrate;

c. forming metal on the substrate over the positions for the through holes;

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5. A circuit board as claimed in any one of claims 1-4, wherein the electrically conductive material comprises plated metal.

6. A circuit board as claimed in any one of claims 1-4, wherein the electrically conductive material comprises paste.

7. A circuit board being substantially as herein described with reference to Figs. 2-7 of the accompanying drawings.

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10. A method for forming a circuit board, said method comprising the steps of:

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