

CLAIMS

~~What is claimed is:~~

1. A method for managing a processor pipeline, comprising:
~~——translating a program counter associated with an instruction block to be fetched to one or more execute permissions associated with the instruction block;~~
~~——associating the instruction block with comprising a speculative execution mode based at least in part on the one or more execute permissions;~~group of instructions and
~~——processing the instruction block relative to the speculative execution mode while the instruction block is in-flight within the processor pipeline.~~

~~2. The method recited in claim 1,~~ wherein the program counter associated with the instruction block points to a virtual address that corresponds to a page table entry storing the one or more execute permissions associated with the instruction block;

associating the instruction block with a speculative execution mode indicating the mode in which the block is expected to execute based at least in part on the one or more execute permissions; and

processing the instruction block relative to the speculative execution mode while the instruction block is in-flight within the processor pipeline.

~~3.2.~~ The method recited in claim ~~2~~1, wherein the page table entry that stores the one or more execute permissions is stored in an instruction-side translation lookaside buffer.

~~4~~3. The method recited in claim 1, wherein the speculative execution mode is a mode in which a memory page corresponding to the instruction block is executable in response to the one or more execute permissions indicating that the memory page is only executable in one mode.

~~5~~4. The method recited in claim 1, wherein the speculative execution mode matches an execution mode associated with a prior instruction block in the processor pipeline in response to the one or more execute permissions indicating that a memory page corresponding to the instruction block is executable in multiple modes.

~~6.5.~~ The method recited in claim 1, wherein the speculative execution mode matches a committed mode in response to the one or more execute permissions indicating that a memory page corresponding to the instruction block is executable in multiple modes.

~~76.~~ The method recited in claim 1, wherein the speculative execution mode includes information to signal a page fault upon the instruction block becoming an oldest block executing in the processor pipeline in response to the one or more execute permissions indicating that a memory page corresponding to the instruction block is not executable.

~~87.~~ The method recited in claim 1, further comprising:

——checking the speculative execution mode associated with the instruction block against a committed execution mode upon the instruction block becoming an oldest block executing in the processor pipeline; and

——restarting the instruction block in response to determining that the speculative execution mode mismatches the committed execution mode.

~~98.~~ The method recited in claim 1, further comprising:

——checking the speculative execution mode associated with the instruction block against a committed execution mode upon the instruction block becoming an oldest block executing in the processor pipeline; and

——committing the instruction block in response to determining that the speculative execution mode matches the committed execution mode.

~~109.~~ The method recited in claim ~~98~~, further comprising preventing at least one successor instruction block from committing in a same cycle as the instruction block in response to the instruction block changing the committed execution mode.

~~110.~~ The method recited in claim ~~109~~, further comprising flushing and restarting the at least one successor instruction block in response to the instruction block changing the committed execution mode to an execution mode that mismatches a speculative execution mode associated with the at least one successor instruction block.

~~111.~~ The method recited in claim ~~98~~, further comprising preventing at least one successor instruction block from committing in a same cycle as the instruction block in response to the at least one successor instruction block having a speculative execution mode that mismatches the committed execution mode.

~~112.~~ The method recited in claim 1, wherein the speculative execution mode is a user mode in which permitted instructions are restricted and memory access is limited to a virtual memory space allocated to the instruction block.

14. ~~The method recited in claim 1, space allocated to the instruction block or wherein the speculative execution mode is a supervisor mode in which privileged instructions are permitted to be executed and access to physical hardware resources is permitted.~~

15. ~~The method recited in claim 14, wherein the supervisor mode is one of a plurality of execution modes in which the privileged instructions are permitted to be executed and access to the physical hardware resources is permitted.~~

1613. An apparatus, comprising:
~~— a processor configured to fetch an instruction block, translate a program counter associated with the instruction block to one or more execute permissions associated with the instruction block, associate the instruction block with a speculative execution mode based at least in part on the one or more execute permissions, and process the instruction block relative to the speculative execution mode while the instruction block is in flight within a pipeline.~~

17. ~~The apparatus recited in claim 16, further comprising an instruction-side translation lookaside buffer (ITLB) configured to store the one or more execute permissions associated with the instruction block in a page table entry, wherein the program counter associated with the instruction block points to a virtual address that corresponds to the page table entry storing the one or more execute permissions associated with the instruction block.~~

18. ~~The apparatus recited in claim 16, wherein the processor is further configured to set the speculative execution mode to a mode in which a memory page corresponding to the instruction block is executable in response to the one or more execute permissions indicating that the memory page is only executable in one mode.~~

19. ~~The apparatus recited in claim 16, wherein the processor is further configured to set the speculative execution mode to one or more of a committed mode or an execution mode associated with a prior instruction block in the pipeline in response to the one or more execute permissions indicating that a memory page corresponding to the instruction block is executable in multiple modes.~~

20. ~~The apparatus recited in claim 16, wherein the processor is further configured to set the speculative execution mode to signal a page fault upon the instruction block becoming an oldest block executing in the pipeline in response to the one or more execute permissions indicating that a memory page corresponding to the instruction block is not executable.~~

21. — The apparatus recited in claim 16, wherein the processor is further configured to:

—— check the speculative execution mode associated with the instruction block against a committed execution mode upon the instruction block becoming an oldest block executing in the pipeline; and

—— restart the instruction block in response to determining that the speculative execution mode mismatches the committed execution mode.

22. — The apparatus recited in claim 16, wherein the processor is further configured to:

—— check the speculative execution mode associated with the instruction block against a committed execution mode upon the instruction block becoming an oldest block executing in the pipeline; and

—— commit the instruction block in response to determining that the speculative execution mode matches the committed execution mode.

23. — The apparatus recited in claim 22, wherein the processor is further configured to prevent at least one successor instruction block from committing in a same cycle as the instruction block in response to the instruction block changing the committed execution mode.

24. — The apparatus recited in claim 23, wherein the processor is further configured to flush and restart the at least one successor instruction block in response to the instruction block changing the committed execution mode to an execution mode that mismatches a speculative execution mode associated with the at least one successor instruction block.

25. — The apparatus recited in claim 22, wherein the processor is further configured to prevent at least one successor instruction block from committing in a same cycle as the instruction block in response to the at least one successor instruction block having a speculative execution mode that mismatches the committed execution mode.

26. — The apparatus recited in claim 16, wherein the speculative execution mode is a user mode in which permitted instructions are restricted and memory access is limited to a virtual memory space allocated to the instruction block.

27. — The apparatus recited in claim 16, wherein the speculative execution mode is a supervisor mode in which privileged instructions are permitted to be executed and access to physical

hardware resources is permitted.

28. ~~The apparatus recited in claim 27, wherein the supervisor mode is one of a plurality of execution modes in which the privileged instructions are permitted to be executed and access to the physical hardware resources is permitted.~~

29. ~~An apparatus, comprising:~~

~~——means for translating a program counter associated with an instruction block to be fetched to one or more execute permissions associated with the instruction block; the instruction block comprising a group of instructions and wherein the program counter associated with the instruction block points to a virtual address that corresponds to a page table entry storing the one or more execute permissions associated with the instruction block;~~

~~——means for associating the instruction block with a speculative execution mode indicating the mode in which the block is expected to execute based at least in part on the one or more execute permissions; and~~

~~——means for processing the instruction block relative to the speculative execution mode while the instruction block is in-flight within a processor pipeline.~~

3014. A computer-readable medium storing computer-executable instructions, the stored computer-executable instructions configured to cause ~~a processor~~ an apparatus according to claim 13 to:

~~——translate a program counter associated with an instruction block to be fetched to one or more execute permissions associated with the instruction block;~~

~~——associate the instruction block with a speculative execution mode based at least in part on the one or more execute permissions; and~~

~~——process the instruction block relative to the speculative execution mode while the instruction block is in-flight within a pipeline associated with the processor.~~

implement the method according to any of claims 1 to 12.