Forming Polysilicon Structures

Background

This invention relates generally to the formation of polysilicon structures including the formation of polysilicon gate electrodes.

Conventionally, polysilicon gate electrodes are formed by depositing polysilicon over a substrate that may be covered with a suitable gate dielectric. The polysilicon material is then doped, for example, using an ion implantation process.

It is then necessary to define the polysilicon electrodes from the doped polysilicon layer using etching techniques. However, etching doped polysilicon presents significant challenges. These challenges include known profile and differential etch bias issues.

Thus, there is a need to find a way to form polysilicon structures, such as gate electrodes, without necessitating the etching of heavily doped polysilicon material.

Brief Description of the Drawings

Figure 1 is an enlarged cross-sectional view of an embodiment of the present invention at an early stage of manufacture;

Figure 2 is an enlarged cross-sectional view corresponding to Figure 1 at a subsequent stage in accordance with one embodiment of the present invention;

Figure 3 is an enlarged cross-sectional view corresponding to Figure 2 at a subsequent stage in accordance with one embodiment of the present invention;

Figure 4 is an enlarged cross-sectional view at a subsequent stage in accordance with one embodiment of the present invention; and

Figure 5 is an enlarged cross-sectional view at a subsequent stage in accordance with one embodiment of the present invention.

Detailed Description

Referring to Figure 1, a semiconductor substrate may have a polysilicon material formed over a suitable gate dielectric. The substrate may, for example, be a silicon substrate and the gate dielectric may be an oxide, for example. The polysilicon material may then be patterned to form the polysilicon gate material 14 over a gate dielectric 12, all positioned over a substrate 10, as shown in Figure 1. Because the polysilicon material is

undoped or substantially undoped when etched, it may be more easily etched and patterned to define the shape shown in Figure 1.

By "substantially undoped," it is intended to refer to a polysilicon material that either has no doping or doping at levels substantially lower than the doping levels utilized to form doped polysilicon gate electrodes that are either n-type or p-type. Generally, these gate electrodes are considered heavily doped and have doping concentrations of greater than 1E18 atoms per cm^3.

The gate material 14 may be covered by a relatively thinner layer 16 and a relatively thicker layer 18. In one embodiment the layer 16 may be an insulator such as silicon dioxide. The layer 18 may, for example, be an insulator such as silicon nitride or a combination of layers of silicon nitride and silicon dioxide, as two examples.

The structure shown in Figure 2 may be subjected to a conventional planarization step such as a chemical mechanical planarization (CMP) operation. The planarization may utilize the thinner layer 16 as a planarization stop in one embodiment. Thus, as shown in Figure 2, the upper portion of the thicker layer 18 may be removed down to the height of the uppermost portion of the thinner layer 16.

The exposed portion of the thinner layer 16 may then be removed using any suitable technique. One suitable technique is a wet etch using hydrofluoric or H_3PO_4 etchant, for example. The resulting structure, shown in Figure 3, has the upper portion of the thinner layer 16 removed and possibly a little bit of the gate material 14. In case some of the gate material 14 is removed, the initial structure of the gate electrode 14 may be slightly higher than is needed to account for the ensuing loss of material.

In an embodiment in which polysilicon gate electrodes for complementary metal oxide semiconductor (CMOS) technologies are involved, a photodefinition process may be used to define n-type and p-type areas. The n-type areas may include n-type doped polysilicon gate electrodes and the p-type areas may include p-type doped polysilicon gate electrodes.

An ion implantation or other doping process may be utilized to appropriately dope the polysilicon material 14. For example, when the n-type areas are doped, a suitable dopant may be utilized to dope the gate material 14 in the p-type doped areas with the n-type areas covered and with the p-type areas covered, a suitable dopant may be utilized to

dope the n-type areas. It may be appreciated that since the doping is done after the definition of the gate material 14, the need to etch heavily doped polysilicon may be largely, if not completely, avoided.

Referring to Figure 4, a suitable etching process may be utilized to remove the thicker layer 18. For example, a wet etch may be utilized in one embodiment.

Referring to Figure 5, the horizontal portion of the thinner insulator 16 may then be removed using an anisotropic etch process, such as a dry etch in one embodiment. As a result, a portion of the thinner layer 16 may remain and this may function as a sidewall spacer in some embodiments.

Alternatively, the thinner layer 16 may be completely removed, for example, using an isotropic etch such as an isotropic wet etch.

In some embodiments, polysilicon material may be defined and patterned without the need to etch heavily doped polysilicon. As a result, the quality and feasibility of the etching process may be improved in some situations.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is:

1. A method comprising:
patterning a substantially undoped polysilicon material;
doping the patterned polysilicon material; and
covering the patterned polysilicon with a covering including a first thinner layer over a second thicker layer.

2. The method of claim 1 including forming a polysilicon gate electrode from said polysilicon material.

3. The method of claim 2 including forming n-type and p-type polysilicon gate electrodes from said polysilicon material.

4. The method of claim 1 including planarizing the covered polysilicon material.

5. The method of claim 4 including doping the polysilicon material after planarizing the covered polysilicon material.

6. The method of claim 5 including removing said first material after doping said polysilicon material.

7. The method of claim 1 including covering said polysilicon material with a first thinner layer formed of silicon dioxide.

8. The method of claim 7 including covering said first thinner layer with a second thicker layer including silicon nitride.

9. The method of claim 1 including removing said thicker layer and leaving at least a portion of said thinner layer.

10. The method of claim 1 including exposing said polysilicon material using planarization.

11. The method of claim 10 including planarizing said covered polysilicon material down to a planarization stop layer in said covering.

12. The method of claim 11 including removing said planarization stop layer to expose said polysilicon material and then implanting said polysilicon material.

13. A semiconductor structure comprising:

a substrate;

a patterned polysilicon material on said substrate, said patterned polysilicon material being substantially undoped; and

a cover material over said polysilicon material, said cover including a thicker layer over said polysilicon material and a thinner layer over said thicker material.

14. The structure of claim 13 wherein said cover material includes a first layer of silicon dioxide and a second layer of a different insulative material.

15. The structure of claim 14 wherein said polysilicon material is exposed through said cover material.

16. A method comprising:

patterning a substantially undoped polysilicon material;

covering the substantially undoped polysilicon material with a covering including a first thinner laver over a second thicker layer;

forming an opening through said covering; and

doping the patterned polysilicon material through said opening.

17. The method of claim 16 including planarizing said covering to form said opening.

18. The method of claim 17 including covering said polysilicon material with a first thinner layer formed of silicon dioxide.

19. The method of claim 18 including covering said first thinner layer with a second thicker layer including silicon nitride.

20. The method of claim 17 including removing said second thicker layer and leaving at least a portion of said first thinner layer.

21. The method of claim 20 including planarizing said covering through said second thicker layer down to the first thinner layer.

22. The method of claim 21 including forming said opening by etching through said first thinner layer to expose said polysilicon material.

23. The method of claim 22 including implanting said polysilicon material through said opening.