



Ferroelectric memory device, and readout method for such a device

Field of the invention

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The present invention relates to a ferroelectric memory device, and to a method for reading-out data stored by such a memory devices.

Background of the invention

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Ferroelectric random access memory (FeRAM) is starting to be utilized for certain products which make use of its non-volatility. Since it does not require any electric power to maintain the stored data, it is suitable for use in passive devices, such as IC tags or IC cards. The principle of storing and retrieving data is as follows. A single memory cell consists of a thin film of a ferroelectric material and a pair of electrodes which are deposited respectively on the top and bottom surfaces of the ferroelectric thin film. When a certain level of positive electric field (E) is applied between the top and bottom electrodes which is higher than the coercive field of the ferroelectric thin film (E_c) (i.e. $E > E_c$), the spontaneous polarization in the ferroelectric thin film aligns with the applied electric field. Suppose this state to be "1". Conversely, when a negative field ($-E$) stronger than $-E_c$ is applied (i.e. $|E| > |E_c|$), the spontaneous polarization aligns with the negative direction, which is opposite to the direction associated with state "1". Suppose this state to be "0". Thus a single cell can memorize one data bit, namely, state "1" and "0".

A conventional readout process is to apply a negative field $-E$ to between the electrodes. Suppose that the information "1" is stored in the memory cell. When the negative field $-E$ is applied between the electrodes of the cell, the field reverses the spontaneous polarization. At this time, an electric displacement current caused by the polarization reversal can be observed on the lead attached to the surface electrodes. Now, suppose that information "0" had been

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stored in the memory cell. In that case, when the negative field $-E$ was applied between the electrodes on the cell, the spontaneous polarization would not have been reversed by the field $-E$, because the polarization already pointed to the negative direction. Therefore, no electric displacement current could have
5 been observed in case of state "0". Thus, in summary, if an electric displacement current can be observed, it is considered that the stored information was "1", and in this way it is determined whether the stored data is "1" or "0".

10 Unfortunately, this process overwrites the information "0" on all the cells which have been read. Therefore, if it is desired for the memory to store the same information after the retrieval process, state "1" has to be rewritten to all those cells which were previously storing state "1". In other words, this readout process is considered as a destructive process.

15 Frequent repetition of polarization reversal causes deterioration of the ferroelectric thin film. As a result of the deterioration, the remnant polarization P_r becomes smaller after a number of polarization reversals. This phenomenon limits the number of rewrites to about 10^4 cycles. This is one of the major
20 reasons why FeRAM cannot currently replace other conventional memory devices, such as SRAM, DRAM or Flash memory.

In view of the foregoing problems with conventional processes and devices, there exists a need for a novel structure and readout method of FeRAM which
25 requires no destructive readout process.

Summary of the Invention

In general terms, the present invention aims to provide a new and useful
30 ferroelectric memory device, and new methods of retrieving data stored in a ferroelectric memory device.

In general terms, the present invention proposes that a ferroelectric capacitor of an FeRAM memory device is arranged in proximity to a heating device. When the data stored in the ferroelectric capacitor is to be retrieved, the heating device heats the ferroelectric capacitor. This, due to the pyroelectric effect, causes the ferroelectric capacitor to emit a charge with a polarity which is indicative of the polarization state of the ferroelectric capacitor, so measurement of this polarity permits the stored data to be determined. Thus, the data stored in a memory cell may be retrieved without overwriting. In many applications, this makes it possible to reduce the number of polarization reversals dramatically during expected usage of the FeRAM memory device, and thus helps to extend the life time of the device.

A first aspect of the invention is an FeRAM memory device having:

a plurality of memory cells, each memory cell comprising:

- (i) an element of ferroelectric material,
 - (ii) a pair of electrodes sandwiching the element of ferroelectric material,
- and

(iii) a heater element for generating heat;

voltage application means for applying an electrical voltage across the heater element, and

measurement means electrically coupled to the top and bottom electrodes for measuring the polarity of the electrical voltage generated by the ferroelectric material due to heating by the heater element.

The measurement means may, for example, be a capacitor electrically coupled via the electrodes to the ferroelectric material, and a voltmeter for measuring voltage developed across the capacitor. Alternatively, the voltmeter may be replaced by a comparator.

A second aspect of the invention is a method of retrieving data from an FeRAM memory device having a plurality of memory cells, each memory cell comprising:

(i) an element of ferroelectric material,
(ii) a pair of electrodes sandwiching the element of ferroelectric material,
and

(iii) a heater element for generating heat;

5 the method comprising:

(a) applying an electrical voltage across the heater element of one of the
memory cells,

(b) measuring the polarity of the electrical voltage generated by the
ferroelectric material due to heating of the ferroelectric material by the heater
10 element; and

(c) determining the polarization state of the ferroelectric material using
the measured polarity.

Brief description of the drawings

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Preferred features of the invention will now be described, for the sake of
illustration only, with reference to the following Figures in which:

Fig. 1 is a schematic, cross-sectional view of a memory cell of a memory device
20 which is an embodiment of the invention;

Fig. 2 is composed of Figs. 2(a) and 2(b) which are schematic views of the
memory cell of Fig. 1 in combination with a first set of readout circuitry, and
illustrate the readout process in this case that the memory cell is in a first
25 polarity state;

Fig. 3 is composed of Figs. 3(a) and 3(b) which are schematic views of the
memory cell of Fig. 1 in combination with the first set of readout circuitry, and
illustrate the readout process in this case that the memory cell is in a second
30 polarity state;

Figure 4 is a perspective view of the construction of a matrix of the memory cells of Fig. 1;

Fig. 5 is composed of Figs. 5(a) and 5(b) which are schematic views of the memory cell of Fig. 1 in combination with a second set of readout circuitry, and illustrate an alternative readout process; and

Fig. 6 is a schematic view of the memory cell of Fig. 1 in combination with a third set of readout circuitry.

Detailed Description of Preferred Embodiments

Referring firstly to Fig. 1, a cross-sectional view is shown of a memory cell of an FeRAM device which is an embodiment of the invention. The memory cells comprise a ferroelectric layer 1, two electrodes 2, 3 attached to respective surfaces of said ferroelectric layer 1, a heater layer 4, and two electrodes 5, 6 attached to respective surfaces of the heater layer 4. An electrically insulating (but heat conducting) layer 9 is located between the electrode 3 and the electrode 5. One suitable material to form the ferroelectric layer 1 is a copolymer of vinylidene fluoride and trifluoroethylene (P(VDF/TrFE)), but this layer may alternatively be formed from a different ferroelectric material, such as PZT. The heater layer 4 may be composed of NiCr alloy. More generally, it is preferred that the heater layer is composed of a material having a volume resistivity in the range $0.1 \mu\Omega m < R_v < 10 \mu\Omega m$.

Fig. 2 shows how data can be readout of such a device and a first set of components which may be used for this. Note that the memory device further includes components (not shown, but of conventional design) for controlling the voltages of the electrodes 2, 3 when data is to be written to the cell, and may optionally include also the circuitry for performing the conventional read-out process described above.

During the read-out process, the electrode 3 is connected to earth (note that this connection is usually via a switch (not shown) which is closed when the present read-out process is performed, but may be open at other times, e.g. to allow the electrode 3 to be at a non-zero potential when data is written to the cell). The top electrode 2 is connected to one terminal of a sensing capacitor 7. The other terminal of the capacitor 7 is grounded. A voltmeter 8 is arranged to detect the voltage across the capacitor 7.

Suppose that, as shown in Fig. 2(a), the ferroelectric layer 1 is initially polarized so that the electric dipole points upward. Without loss of generality we can assume that this corresponds to storing the digital information "1" in the memory cell. The dipole of the polarization attracts charged particles from the surroundings (e.g. particles in the ambient air or insulation layer) and the surface charge on the electrodes 2 and 3 induced by the dipole is kept neutralized. This state is one of electric equilibriums. Since the positive and negative charges are balanced at the electrode 2, no charge is observed in the sensing capacitor 7. In order to retrieve the stored data, an electric current is passed through the heater layer 4 using the electrodes 5 and 6. Once the heater layer 4 is heated up, the temperature of the ferroelectric layer 1 which is adjacent to the heater rises. Since the total amount of dipole in the ferroelectric layer changes sensitively according to the temperature, the surface charge on the electrodes 2 and 3 varies sharply while the temperature changes. In this case, as the temperature increases, the surface charge decreases. The decrease of the surface charge induces redundant charged particles on the electrode 2. As a result of this electric imbalance, a certain amount of charge is induced in the sensing capacitor 7 and it is detected by reading the voltmeter 8. The voltage V_p observed by the voltmeter is expressed by the following formula:

$$V_p = q/C$$

where q is imbalanced charge and C is a capacitance of the sensing capacitor.

The above-mentioned effect is called the pyroelectric effect and is utilized for the devices such as infrared ray sensors. In case the stored information is "1", a positive voltage V_p is observed by the voltmeter 8 (see Fig. 2(b)). Once the current to the heater layer is stopped, the temperature of the ferroelectric layer drops and the amount of polarization reverts to the initial state.

Turning now to Fig. 3, the situation is shown in which the ferrocapacitor initially has a dipole which is directed downward (i.e. the stored information is "0"), as shown in Fig. 3(a). In this case, when the heater layer 4 heats the ferroelectric layer 1, a negative voltage $-V_p$ is observed by the voltmeter 8 (as shown in Fig. 3(b)). Thus, by using the pyroelectric effect, it can be determined whether the stored data is "1" or "0" without any destruction of stored data.

Turning to Fig. 4, the possible structure of an array of memory cells of the kind illustrated in Fig. 1 is shown in a perspective view. There is a single layer of ferroelectric material extending through a plurality of the cells. Furthermore, there are a plurality of parallel top electrode lines 2, and a plurality of parallel bottom electrode lines 3 (transverse to the top electrode lines). Each memory cell is at the intersection of a top electrode line 2 with a bottom electrode line 3. Similarly, there is a single heater layer 4. Formed over it are a plurality of parallel top electrode lines 5, and formed beneath it are a plurality of bottom electrode lines 6 (transverse to the bottom electrode lines), such that there is an intersection between one of the top electrode lines 5 and one of the bottom electrode line 6 vertically below each of the memory cells. Thus, when the data stored in a given memory cell is to be measured, the corresponding portion of the heater layer 4 is heated by applying the correct voltages to the corresponding top electrode layer 5 and bottom electrode layer 6, and the voltages of the corresponding top electrode layer 2 and bottom electrode layer 3 are measured.

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Turning to Fig. 5 the memory cell of Fig. 1 is shown in combination with a second set of readout circuitry. The difference between the two sets of circuitry

is that the voltmeter 8 of Fig. 2(a) is replaced by a comparator 10 in Fig. 5(a). Fig. 5(a) corresponds to the state illustrated in Fig. 3(b) and Fig. 5(b) corresponds to the state illustrated in Fig. 2(b). The output of the comparator 10 is low ("L") in the case of Fig. 5(a), and high ("H") in the case of Fig. 5(b), and thus the output of the comparator 10 is indicative of the polarization of the ferroelectric layer 1.

Note that in case that the capacitance of the sensing capacitor (C) 7 is much smaller than that of the ferroelectric capacitor, the sensing capacitor 7 is useful to enhance the sensing voltage V_p (because $V_p = q/C$). However, when they are comparable (for example, when the area of one single memory cell is quite small) the sensing capacitor 7 is not required. For example, turning to Fig. 6, a variation of the arrangement of Fig. 5 is shown which is also an embodiment of the invention and in which the sensing capacitor 7 is omitted. The arrangement of Fig. 6 is illustrated at a time when its polarization state is the same as that of Fig. 5(b) and the heater layer 4 is activated. Similarly, an embodiment of the invention may be formed which is similar to that of Figs. 2 and 3, but in which the sensing capacitor 7 is omitted.

Although only a few embodiments of the invention have been discussed in detail, many variations are possible, as will be clear to a skilled reader, within the scope of the invention, as defined by the claims.

Claims

1. An FeRAM memory device having:
 - a plurality of memory cells, each memory cell comprising:
 - 5 (i) an element of ferroelectric material,
 - (ii) a top electrode and a bottom electrode sandwiching the element of ferroelectric material, and
 - (iii) a heater element for generating heat;
 - voltage application means for applying an electrical voltage across the
 - 10 heater element, and
 - measurement means electrically coupled to the top and bottom electrodes and arranged to measure the polarity of the electrical voltage generated by the ferroelectric material due to heating by the heater element.
- 15 2. A memory device according to claim 1 in which the measurement means further includes a voltmeter arranged to measure the voltage generated by the ferroelectric material.
3. A memory device according to claim 1 in which the measurement means
- 20 includes a comparator arranged to measure the polarity of the voltage between the electrodes.
4. A memory device according to claim 2 or claim 3 in which the measurement means includes a capacitor electrically coupled via the electrodes
- 25 to the ferroelectric material.
5. A memory device according to any preceding claim in which said memory cells are arranged in a two dimensional array, the top electrodes of multiple said memory cells being connected in a first set of parallel lines, and
- 30 the bottom electrodes of multiple said memory cells being connected in a second set of parallel lines transverse to the first set of lines.

6. A memory device according to any preceding claim in which the voltage application means comprises a first array of first heater electrodes and a second array of second heater electrodes, the two arrays of heater electrodes sandwiching a layer of heater material, each said heater element being a portion of the layer of heater material which is sandwiched by an intersection of a first heater electrode and a second heater electrode.
7. A method of retrieving data from an FeRAM memory device having a plurality of memory cells, each memory cell comprising:
- (i) an element of ferroelectric material,
 - (ii) a pair of electrodes sandwiching the element of ferroelectric material, and
 - (iii) a heater element for generating heat;
- the method comprising:
- (a) applying an electrical voltage across the heater element of one of the memory cells,
 - (b) measuring the polarity of the electrical voltage generated by the ferroelectric material due to heating of the ferroelectric material by the heater element; and
 - (c) determining the polarization state of the ferroelectric material using the measured polarity.