CLAIMS

1. A method of dicing a semiconductor wafer comprising a plurality of integrated circuits, the method comprising:

(a) forming a mask above the semiconductor wafer, the mask comprising:

(i) a water-soluble matrix based on a solid component and water;

(ii) a metal compound dissolved throughout the water-soluable matrix, the metal compound comprising:

(1) an aluminum cation or a tin cation;

(2) a potassium cation or a calcium cation; or

(3) a copper cation, a nickel cation, a silver cation, or a chromium cation; and

(b) patterning the mask and a portion of the semiconductor wafer with a laser scribing process to provide a patterned mask with gaps and corresponding trenches in the semiconductor wafer in regions between the integrated circuits.

2. The method of claim 1, further comprising:

plasma etching the semiconductor wafer through the gaps in the patterned mask to extend the trenches and to singulate the integrated circuits, wherein the patterned mask protects the integrated circuits during the plasma etching.

3. The method of claim 2, wherein plasma etching the semiconductor wafer comprises using a fluorine-based etch chemistry, and the metal compound is resistant to the fluorine-based etch chemistry.

4. The method of claim 1,

wherein the metal compound comprises an acetate anion; and

wherein the metal compound is dibasic.

5. The method of claim 1, wherein the metal compound comprises aluminum acetate dibasic stabilized by boric acid.

6. The method of claim 5, wherein the solid component of the water-soluble matrix is poly(vinyl alcohol) (PVA).

7. The method of claim 6, wherein the ratio by weight of the aluminum acetate dibasic to PVA is in the range of 1:2 to 1:3.

8. The method of claim 6, wherein the water-soluble matrix further comprises poly(vinyl pyrrolidone) (PVP).

9. The method of claim 8, wherein the ratio by weight of the aluminum acetate dibasic to PVA to PVP is 1:2:1.

10. The method of claim 1, wherein the solid component of the water-soluble matrix is poly(vinyl alcohol) (PVA), and wherein the water-soluble matrix further comprises poly(vinyl pyrrolidone).

11. The method of claim 2, wherein plasma etching the semiconductor wafer comprises plasma etching a single crystalline silicon wafer, and wherein a ratio of an etch rate of the single crystalline silicon wafer to an etch rate of the mask is approximately in the range of 36:1 – 140:1 during the plasma etching.

12. The method of claim 1, further comprising:
prior to forming the mask above the semiconductor wafer, performing a plasma or chemical pre-treatment on the semiconductor wafer to increase wettability and coating of the mask on the semiconductor wafer.

13. The method of claim 2, further comprising:
subsequent to plasma etching the semiconductor wafer, removing the patterned mask using an aqueous solution.

14. The method of claim 2, further comprising:
subsequent to patterning the mask and prior to plasma etching the semiconductor wafer through the gaps in the patterned mask to singulate the integrated circuits, cleaning the trenches in the semiconductor wafer with a plasma cleaning process.

15. The method of claim 1, wherein forming the mask above the semiconductor wafer comprises spin-coating the mask on the semiconductor wafer.