

PATENT SPECIFICATION (11)

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Invention is hereby given



(21) Application No. 21431/74 (22) Filed 14 May 1974 (19)
(31) Convention Application No. 361 377 (32) Filed 17 May 1973 in

(33) United States of America (US)

(44) Complete Specification published 6 Oct. 1976

(51) INT. CL.³ G11C 11/24 5/02

(52) Index at acceptance

G4C 1B 2JX 2K 5 6

H3T 1PX 2B2 2F1 2J 2T3F 3C2 3J 3X 4C 4E2N 4M 5E

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(54) IMPROVEMENTS IN OR RELATING TO MEMORY SYSTEMS

(71) We, TELETYPE CORPORATION, of 5555 Touhy Avenue, Skokie, Cook County, State of Illinois, United States of America, a Corporation organised under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to memory systems.

Random access MOSFET memories utilizing incremental charges to store information in an array of memory cells, each cell including one MOSFET device and one capacitance device, are known. Each row of the array of memory cells may include a sense-refresh amplifier for sensing the presence of an information-bearing charge on an addressed memory cell within that row. Each sense-refresh amplifier also periodically refreshes the information stored as charge on memory cells within that row. This periodic refreshing of the charge on memory cells counteracts the tendency of the charge to gradually dissipate from the capacitance device within that cell.

Typically, each sense-refresh amplifier circuit requires a source of multiphase clock signals in order to properly perform the sensing and refreshing functions in synchronism with the remainder of the memory. In practice, these signals are provided by coupling each amplifier to a number of clock circuits.

Each of these clock circuits requires additional area on the surface of a silicon chip and consumes additional electrical power. The surface area devoted to these clock circuits reduces the area available for memory cells. Electrical power dissipated by the clock circuits generates undesirable heat and necessitates larger power supplies than would be required by a memory requiring only a single phase clock circuit.

The capacitance device located in each memory cell must be coupled to a reference ground potential. Generally in MOSFET

memories the reference ground potential is provided by connecting each of these capacitance devices to a ground bus. Alternatively, the ground reference is established by coupling each capacitance device to the substrate upon which it is formed, thereby establishing a substrate ground.

Either of these two means of establishing the reference ground is undesirable since it significantly increases the surface area required by each memory cell. If ground buses are provided, additional area on the silicon chip surface must be provided to accommodate at least one ground bus for every two columns of memory cells. Similarly, if a substrate ground is used, each capacitance device requires an increased area on the chip surface in order to effectively couple the capacitance device to the substrate ground.

Thus, the known methods of establishing a reference ground result in an inefficient and costly consumption of chip surface area. The surface area required for the ground buses or for coupling each capacitance device to the substrate ground substantially limits the number of memory cells which can be placed on a chip of given area. Conversely, a memory of a given capacity will require more and/or larger chips than the optimum number as a result of the area which must be devoted to the reference ground. Clearly then, the known methods of providing the reference ground present major disadvantages with respect to efficient utilization of chip surface area, manufacturing cost, and undesirable complexity of the memory circuit.

According to one aspect of this invention a memory system includes a memory cell having capacitance for storing charge representative of binary data, and means for refreshing said data including a first and a second terminal, said first and second terminals being connected respectively to a first and a second capacitance of substantially equal value, said refreshing means being for providing on said terminals an initial ground

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potential and a second potential in response, in operation, to a clock signal having a first and second value respectively, said memory capacitance being connectable in parallel to one of said first and second capacitances, said one capacitance of the parallel combination of said memory capacitance and said one capacitance being in response to said second value clock signal charged from said initial ground potential towards said second potential at a slower or a faster rate than the charging rate of the other capacitance dependent upon the initial state of said memory capacitance, and said refreshing means being adapted to restore to said memory capacitance said initial state in response to the differential charging rate between said first and second capacitances.

Said refreshing means may include a first and a second gating device each having two controlled electrodes and a control electrode, the control electrode of each said device being connected to a respective one of said terminals and one of the controlled electrodes of the other said device, and the other one of said controlled electrodes of each said device being connected together, said first and second gating devices being adapted to respond to said differential charging rate between said first and second capacitances to restore said initial state to said memory capacitance.

Said refreshing means may include means for receiving said clock signal and a pair of resistive means, each for connecting said receiving means to a respective one of said terminals for providing thereat said initial ground potential and said second potential.

Said refreshing means may include a pair of resistive means each for connecting a constant potential to a respective one of said first and second terminals, and a third and a fourth gating device, each having two controlled electrodes and a control electrode, each said controlled electrode of said third and fourth gating devices being coupled to a respective said controlled electrode of said first and second gating devices and the control electrodes thereof being coupled together and being for receiving said clock signal, said pair of resistive means and said third and fourth gating devices being adapted to co-operate to provide said initial ground potential and said second potential on said first and said second terminals.

Each said resistive means may comprise a gating device.

Said memory cell may comprise a gating device having two controlled electrodes and a control electrode, said control electrode being connected to an address bus for enabling said gating device to connect said memory capacitance in parallel with said one capacitance, one of said controlled electrodes being connected to one of said first

and second terminals, the other controlled electrode having said memory capacitance and being connected to an address bus for enabling an adjacent memory cell.

Said system may include a first and a second plurality of said memory cells, a first conductor for connecting said first plurality of memory cells to said first terminal and a second conductor for connecting said second plurality of memory cells to said second terminal, the memory capacitance of a selected said cell of said first plurality of cells being, in operation, connected in parallel to said first capacitance, said first capacitance of the parallel combination of said memory capacitance and said first capacitance being in response to said second value clock signal charged from said initial ground potential towards said second potential at a slower or a faster rate than the charging rate of said second capacitance dependent upon the initial state of said memory capacitance, and said refreshing means being adapted to invert input data to be written on said selected memory cell of said first plurality in response to the differential charging rate between said first and second capacitances. Said system may include a plurality of address buses for selectively addressing said first and second pluralities of memory cells to connect a selected said memory cell therefrom to said first or said second conductor, each of said memory cells including a gating device having two controlled electrodes and a control electrode, said control electrode being connected to one of said address buses for enabling said gating device to connect the memory capacitance thereof to said refreshing means, one of said controlled electrodes being connected to one of said first and second terminals, the other controlled electrode having said memory capacitance and being connected to an adjacent one of said address buses for enabling an adjacent one of said memory cells.

According to another aspect of this invention there is provided a method of refreshing binary data on a memory cell having capacitance for storing charge representative of said data, said method including providing an initial ground potential to a first and a second capacitance of substantially equal value in response to a first value clock signal, providing a second potential to said first and second capacitances in response to a second value clock signal, connecting said memory capacitance in parallel with one of said capacitances such that said one capacitance of the parallel combination of said memory capacitance and said one capacitance is in response to said second value clock signal charged from said initial ground potential towards said second potential at a slower or faster rate than the charg-

ing rate of the other said capacitance dependent upon the initial state of said memory capacitance, and refreshing said memory cell to restore thereon said initial state in response to the differential charging rate between said capacitances.

The present invention will now be described by way of example with reference to the accompanying drawings in which:

Fig. 1 is a block diagram of a portion of a memory arrangement in accordance with the invention;

Fig. 2 is a graphical representation of the waveforms appearing at various points in the diagram of Fig. 1;

Fig. 3 is a schematic diagram of a sense-refresh amplifier;

Fig. 4 is a schematic diagram of a second embodiment of a sense-refresh amplifier; and

Fig. 5 illustrates a preferred topography of two of the memory cells of Fig. 3.

Referring to Fig. 1, there is illustrated a block diagram of a portion of an overall arrangement of a memory 11 which includes a plurality of memory cells 12 arranged in an orthogonal array. Each memory cell 12 represents a capability of the memory 11 to store one bit of information in the form of a binary "1" or "0".

The array of the memory cells 12 is organized into a plurality of rows and columns. The memory cells 12 within each column are coupled together by a Y address bus, for example Y_1 . Each column may be identified with a specific Y address by reference to one of a plurality of Y address buses, Y_1 to Y_j .

Further, the memory 11 is divided into a right bank or half 13 and a left bank or half 14, each bank having an equal number of the cells 12. The Y address buses Y_1 to Y_k are located on the left and the Y address buses Y_{k+1} to Y_j on the right. Since $j=2k$, the number of columns on each side is equal. The two halves 13 and 14 of the memory 11 are separated by a plurality of sense-refresh amplifiers 16₁ to 16_j.

The memory cell 12 within each row are coupled together by an input-output bus, for example input-output (I/O) bus X_1 . Each row may be identified with a specific X address by reference to one of a plurality of I/O buses X_1 to X_i . Each I/O bus is divided into a right and left half, such as a right half 17 and a left half 18 of the I/O bus X_1 . Both halves of each of the I/O buses X_1 to X_i are coupled to one of the plurality of sense-refresh amplifiers 16₁ to 16_j. For example, both the halves 17 and 18 of the I/O bus X_1 are coupled to the sense-refresh amplifiers 16₁. A clock signal input terminal 19 is coupled to each of the plurality of sense-refresh amplifiers 16₁ to 16_j.

Each of the plurality of I/O buses X_1 to

X_i is coupled to one of a plurality of transistors 21₁ to 21_i which are coupled to decoder circuits (not shown). Each of the plurality of Y address buses Y_1 to Y_j are also coupled to additional decoder circuits (not shown). The decoder circuits selectively drive the Y address buses and the plurality of transistors 21₁ to 21_i to address each of the plurality of memory cells 12. Write functions for all of the rows are provided by a first amplifier 22 having a write input 23, and a data input 24, and an output terminal 26. The output terminal 26 is selectively coupled through each of the transistors 21₁ to 21_i to each of the I/O buses X_1 to X_i by decoder circuits. Similarly, a read output is provided for each of the I/O buses X_1 to X_i by a second amplifier 27 having a head input 28, a data input 29 from the I/O buses, and an output terminal 31.

Associated with each of the halves 17 and 18 of the I/O bus X_1 is a distributed capacitance resulting from the inherent capacitance of the I/O bus X_1 . These distributed capacitances of the halves 17 and 18 may be treated as discrete capacitors, as indicated by load capacitors 33 and 34 shown in phantom in Fig. 3. Significantly, the value of the load capacitor 33 associated with the right half 17 of the I/O bus X_1 is equal to the value of the load capacitor 34 associated with the left half 18. The effect of transistors 21₁ to 21_i on the distributed capacitance of the right half 17 is balanced by a compensating circuit (not shown) coupled to the end of the left half of each of the I/O buses X_1 to X_i .

Referring to Fig. 2, there is shown a series of waveforms as they appear at various points in the memory 11 of Fig. 1. Two cycles in the operation of the memory 11 are shown. The first cycle includes the time interval from $t=t_0$ to $t=t_0^1$ and the second cycle includes the interval from $t=t_0^1$ to $t=t_1^1$. During these two cycles, only the first two Y address buses, Y_1 and Y_2 , are addressed. A complete working cycle of the memory 11 would require numerous additional cycles of the Y address buses. However, two cycles involving only the Y address buses Y_1 and Y_2 are sufficient to illustrate the operation of the memory 11.

Fig. 2A represents a single phase clock or timing signal, ϕ which is applied to each of the sense-refresh amplifiers 16₁ to 16_j (Fig. 1) by the clock input terminal 19 (Fig. 1). During the time intervals from t_0 to t_1 and from t_0^1 to t_1^1 , ϕ is at a potential of 0 volts. While $\phi=0$ volts, the sense-refresh amplifier 16₁ discharges the load capacitors 33 and 34 (Fig. 3) to ground potential.

During the time intervals from t_1 to t_0^1 and from t_1^1 to t_0^{11} , ϕ is at a potential of $-V$. The sense-refresh amplifier 16₁ sets an addressed memory cell 12 to the desired in-

formation storage level ("0" or "1") if a write signal is simultaneously applied to the write input 23 during these time intervals. If a write signal is not applied, the sense-refresh amplifier 16₁ refreshes the memory cell 12 to maintain its current information storage level during these time intervals. The internal operation of the sense-refresh amplifier 16₁ will be explained in further detail hereinafter.

Referring to Fig. 2B, assume that the Y address bus Y₁ (Fig. 1) has been addressed by the decoder circuits (not shown) during the first cycle at time $t=t_1$. If it is desired to write information into the memory cell 12 associated with the I/O bus X₁ (Fig. 1) during the first cycle, a $-V$ potential is applied to turn ON the transistor 21₁ at time $t=t_1$ as shown in Fig. 2E. At the same time a write signal and the data to be entered on the memory cell 12 will be applied to the write input 23 (Fig. 1) and data input 24 (Fig. 1). A write signal at the write input 23 causes the first amplifier 22 to send the data signal to the transistors 21. Since the write signal is present on the I/O bus X₁ at a time when the sense-refresh amplifier 16₁ is setting the addressed memory cell 12, the data signal from the data input 24 will be set into the memory cell, as explained later.

Referring now to Fig. 2C, during the second cycle, at time $t=t_1^1$, the Y address bus Y₂ (Fig. 1) is assumed to have been addressed by the decoder circuits (not shown). If it is desired to read information out of the memory cell 12 on the I/O bus X₁ (Fig. 1) during the second cycle, a $-V$ potential is applied to turn ON the transistor 21₁ at a time $t=t_1^1$ as shown in Fig. 2D. At the same time a read signal is applied to the read input 28 (Fig. 1) which enables the second amplifier 27, and the information to be read out of the addressed memory cell 12 appears at the output terminal 31 (Fig. 1). The $-V$ potential is applied to the transistor 21₁ at time $t=t_1^1$, subsequent to the refreshing of the information stored in the addressed memory cell 12. The read system will be explained in detail hereafter.

Referring to Fig. 3 there is shown a schematic diagram of the sense-refresh amplifier 16₁ of Fig. 1. The sense-refresh amplifier 16₁ is typical of each of the other amplifiers 16₁ to 16_n shown in Fig. 1. For purposes of clarity, only four memory cells 12 are shown coupled to the sense-refresh amplifier 16₁.

The memory cells 12 associated with the Y address buses Y₁ and Y₂ and with the left half 18 of the I/O bus X₁ are coupled to node 1 on one side of the sense-refresh amplifier 16₁. The memory cells 12 associated with the Y address buses Y_{k+1} and Y_{k+2} and with the right half 17 of the I/O bus X₁ are coupled to node 2 on the oppo-

site side of the sense-refresh amplifier 16₁.

Each of the memory cells 12 includes one transistor, such as transistors 36, 37, 38 and 39, and one storage capacitor such as storage capacitors 41, 42, 43 and 44.

The transistors 36, 37, 38 and 39 are desirably MOSFET devices, each having a control electrode, or gate, and a first and a second controlled electrode, or source and drain. For example, the transistor 36 has a gate 46 coupled to the Y address bus Y₁, a first controlled electrode 47 coupled to the left half 18 of the I/O bus X₁, and a second controlled electrode 48 coupled to a first electrode of the storage capacitor 41. It will be apparent from Fig. 3 that the remaining transistors 37, 38 and 39 are coupled to their respective Y address buses Y₂, Y_{k+2} and Y_{k+1}, to the I/O bus X₁, and to their respective storage capacitors 42, 43 and 44 in an identical manner.

A second electrode of the storage capacitor 41, associated with the Y address bus Y₁, is coupled by a lead 51 to the adjacent Y address bus Y₂. Similarly, the second electrode of the storage capacitor 42, associated with the Y address bus Y₂, is coupled by a lead 52 to the adjacent Y address bus Y₁.

Thus, it will be apparent that the storage capacitors included in each of the memory cells 12 have their second electrodes coupled to an adjacent one of the Y address buses Y₁ to Y_n.

As described above, at any selected time only one of the Y address buses Y₁ to Y_n is addressed by the decoder circuits (not shown). The remaining, non-addressed ones of the Y address buses Y₁ to Y_n are at ground potential. Hence, when the Y address bus Y₁ is addressed, the adjacent Y address bus Y₂ will be at ground potential. Since the storage capacitor 41 is coupled to the Y address bus Y₂ by the lead 51, the ground potential present on the Y address bus Y₂ provides the required reference ground for the storage capacitor 41 when the Y address bus Y₁ is addressed. In an identical manner, the storage capacitor in each of the memory cells 12 has its second electrode coupled to an adjacent one of the Y address buses Y₁ to Y_n, thereby providing each of the storage capacitors with a reference ground.

By providing the reference ground for each of the memory cells 12 in the manner described above, a substantial saving in substrate area is realized when the memory cells 12 are produced in integrated circuit form. As shown in Fig. 3, the memory cells 12 may be formed immediately adjacent to each other without interposing a conventional ground bus between adjacent ones of the Y address buses Y₁ to Y_n. Thus, by utilizing an adjacent Y address bus to provide the

reference ground for the memory cells 12 on any selected, addressed Y address bus, one ground bus for each pair of Y address buses can be eliminated. It will be apparent that this saving in surface area resulting from eliminating the conventional ground buses permits either a substantial reduction in the size of an integrated circuit memory array or a substantial increase in the number of memory cells which can be formed in an array of a particular size.

In Fig. 5, the various layers of metal, oxide and semiconductor material as they would actually appear on a semiconductor substrate forming two adjacent memory cells 12 of Fig. 3 are shown.

The left half 18 of the I/O bus X_1 is represented by a portion of a p-type diffusion region 54. The p-type diffusion regions shown in Fig. 5 are formed in one surface of an n-type substrate which underlies the entire circuit of Fig. 5. A p-type diffusion region 56 is shown adjacent to the diffusion region 54. A thin oxide region 57 extends between the diffusion regions 54 and 56 and forms the transistor 36 of Fig. 3. It will be understood that all regions in Fig. 5 which are not specifically noted as being thin oxide regions are covered with a thick oxide coating. This thick oxide coating separates the semiconductor material from all metal conductors and may be formed of, for example, silicon dioxide.

Similarly, another p-type diffusion region 58 is shown adjacent to the diffusion region 54. A thin oxide region 59 extends between the diffusion regions 54 and 58 and forms the transistor 37 of Fig. 3.

The Y address bus Y_1 is represented by a first metal conductor 61 (shown in dotted lines) which overlies the thin oxide region 57. The Y address bus Y_2 is similarly represented by a second metal conductor 62 (shown in dotted lines) which overlies the thin oxide region 59. As shown in Fig. 5 both the p-type diffusion regions 56 and 58 extend between the first and second metal conductors 61 and 62.

A thin oxide region 63 is formed between the diffusion region 56 and the overlying second metal conductor 62. The capacitive coupling through the thin oxide region 63 represents the storage capacitor 41. The coupling through the thin oxide layer 57 represents the coupling of the Y address bus Y_1 to the gate electrode 46 of the transistor 36.

Another thin oxide region 64 is formed between the diffusion region 58 and the overlying first metal conductor 61. The capacitive coupling through the thin oxide region 64 represents the storage capacitor 42 (Fig. 3).

The capacitance value of the storage capacitors 41 and 42 is determined by the

thickness and surface area of the thin oxide regions 63 and 64, respectively.

The diffusion regions 56 and 58 and the thin oxide regions 63 and 64, respectively, serve to couple the transistors 36 and 37 and the storage capacitors 41 and 42, respectively, to their adjacent Y address buses Y_2 and Y_1 , as shown in Fig. 3.

As described above, this coupling to adjacent Y address buses provides a suitable reference ground for the memory cells while requiring a minimum of surface area.

Thus, the topography of Fig. 5 represents one embodiment for the memory cells 12 of Fig. 3 wherein the reference ground for each of the memory cells is provided by coupling each of the storage capacitors to an adjacent one of the Y address buses Y_1 to Y_n . By providing the reference ground in this manner a substantial surface area saving per memory cell is realized.

Referring again to Fig. 3, the sense-refresh amplifier 16, includes a first transistor 66 and a second transistor 67 which are cross-coupled in a flip-flop circuit configuration.

The first transistor 66 has a gate or control electrode 68 which is cross-coupled to a first controlled electrode 69 of the second transistor 67 and is also coupled to the left half 18 of the I/O bus X_1 at node 1. Similarly, the second transistor 67 has a gate or control electrode 71 which is cross-coupled to a first controlled electrode 72 of the first transistor 66 and is also coupled to the right half 17 of the I/O bus X_1 at node 2.

Second controlled electrodes 73 and 74 of the first and second transistors 66 and 67, respectively, are coupled together and coupled to a ground conductor 76. The ground conductor 76 may be common to all the sense-refresh amplifiers 16, to 16_n.

Biasing voltages for the first and second transistors 66 and 67 are provided by third and fourth (load) transistors 77 and 78, respectively, which have second controlled electrodes 81 and 82 that are coupled to nodes 2 and 1 respectively. The third and fourth transistors 77 and 78 have gates 84 and 83, respectively, which are both coupled to a terminal 86. Advantageously, a constant DC voltage is applied to the terminal 86 to continuously bias the load transistors 77 and 78 in the ON state. Thus, the load transistors 77 and 78 function as load resistors for the sense-refresh amplifier 16.

First controlled electrodes 87 and 88 of the load transistors 77 and 78, respectively, are both coupled to the clock signal input terminal 19. Clock signals, such as those represented by the single phase clock signal ϕ shown in Fig. 2A, are, advantageously, applied to the clock signal input terminal 19 to control the operation and timing of the sense-refresh amplifier 16.

Referring to Fig. 4, there is shown an

alternative embodiment of a sense-refresh amplifier 16,¹ which may be used in the memory 11 of Fig. 1. The sense-refresh amplifier 16,¹ includes first and second transistors 91 and 92 which are cross-coupled to nodes 1¹ and 2¹ in a manner identical to that described for the sense-refresh amplifier 16, of Fig. 3.

Third and fourth, or load, transistors 93 and 94 are also coupled to the nodes 1¹ and 2¹ and to terminals 96 and 97 in the same manner as described for the load transistors 77 and 78 and the terminals 86 and 19 of Fig. 3. A first constant DC voltage is, advantageously, applied to the terminal 96 to bias the load transistors 93 and 94 in the ON state. A second constant DC voltage, which may be equal to the first constant DC voltage, is, advantageously, applied to the terminal 97 to apply a biasing voltage through the load transistors 93 and 94 to the first and second transistors 91 and 92. If the first and second constant DC voltages are equal, the terminals 97 and 96 can be the same terminal.

Clock or timing signals are coupled to the first and second transistors 91 and 92 through first and sixth transistors 98 and 99 respectively. Gates 101 and 102 of the fifth and sixth transistors 98 and 99 are both coupled to a clock signal input terminal 19¹.

As shown in Fig. 4, first and second controlled electrodes 103 and 104 of the fifth transistor 98 are respectively coupled to first and second controlled electrodes 106 and 107 of the third transistor 91. Similarly, first and second controlled electrodes 108 and 109 of the sixth transistor 99 are respectively coupled to first and second controlled electrodes 111 and 112 of the fourth transistor 92. The second controlled electrodes 104 and 107, and 109 and 112 are all coupled to a ground conductor 113.

Operation of the sense-refresh amplifier 16,¹ is identical to that of the sense-refresh amplifier 16, (Fig. 3). The clock signal applied to the clock signal input terminal 19¹, however, must be the inverse of the clock signal applied to the clock signal input terminal 19 (Fig. 3). Thus, the clock signal shown in Fig. 2A must be inverted before it is applied to the clock signal input terminal 19¹.

Further, the current amplitudes of the clock signal (Fig. 2A) applied to the terminal 19¹ can be much less than the current amplitudes of the clock signal ϕ required at the terminal 19 (Fig. 3). Since the clock signal drives the gates 101 and 102 of the fifth and sixth transistors 98 and 99, less clock signal power is required than in the sense-refresh amplifier 16, where the clock signal drives the first controlled electrodes 87 and 88 of the third and fourth transistors 77 and 78.

Referring again to Fig. 3, in operation, each refresh cycle of the sense-refresh amplifier 16 is initiated by applying the clock signal ϕ (Fig. 2A) to the clock signal input terminal 19 at time $t=t_0$. At time $t=t_0$, the clock signal is at ground potential, or 0 volts. This 0 volt potential is applied through the third and fourth, or load, transistors 77 and 78 to the nodes 1 and 2.

The load capacitors 33 and 34 which are coupled, respectively, to the right and left halves 17 and 18 of the I/O bus X_1 and to the gates 68 and 71 of the first and second transistors 66 and 67, are discharged through nodes 1 and 2 by the ground potential applied to the clock signal input terminal 19.

After the load capacitors 33 and 34 have had sufficient time to discharge to ground potential, the clock signal ϕ (Fig. 2A) returns at time $t=t_1$ to a potential of $-V$ volts, for example -12 volts. When the clock signal ϕ returns to $-V$ volts the load capacitors 33 and 34 begin charging through the load transistors 77 and 78, respectively.

At the same time, $t=t_1$, one of the Y address buses Y_1 to Y_i is addressed by the decoder circuits (not shown). For example, at time $t=t_1$, the Y address bus Y_1 may be addressed by applying a potential of $-V$ volts thereto (Fig. 2B). Since the gate 46 of the transistor 36 in the memory cell 12 is coupled to the Y address bus Y_1 , application of the $-V$ potential to the Y address bus Y_1 switches the transistor 36 ON. Similarly, all of the transistors in the memory cells 12 having their gates coupled to the Y address bus Y_1 will be switched ON, such that all cells 12 in the selected Y column will be refreshed at the same time corresponding to the time t_1 to t_2 in Fig. 2.

When the transistor 36 is switched ON, the storage or memory capacitor 41 is coupled through the transistor 36 to the left half 18 of the I/O bus X_1 , which effectively is an isolated circuit, and thus to node 1. The storage capacitor 41 is thereby coupled in parallel with the load capacitor 34.

If the storage capacitor such as 41 in the left bank or side 18 of the circuit is at substantially ground potential at the time t_1 , this represents the previous storage of a binary "1". In that case, at time t_1 , the load capacitor 34 will begin to charge toward the $-V$ potential of the negative clock pulse ϕ , but will charge at a slower rate than will the load capacitor 33, due to the combined capacitance of the storage capacitor 41 and the load capacitor 34 being larger than the capacitance of only the load capacitor 33.

Since the load capacitor 33 charges at a faster rate than the load capacitor 34, the gate 71 of the second transistor 67 will reach its threshold voltage (the voltage required to switch the transistor ON) first. After the second transistor 67 is switched ON, the

feedback associated with the flip-flop type circuit of the sense-refresh amplifier 16₁ holds the first transistor 66 OFF. In particular, the load capacitor 34 associated with the memory cell 12 which has been addressed is discharged to ground potential through the now ON transistor 67, and the selected storage capacitor 41 also returns to ground potential between times t_1 and t_2 , thus "refreshing" the 0 volt charge originally present on that capacitor. Charging of the load capacitor 33 from the negative ϕ clock pulse continues until the load capacitor 33 is charged to a potential of $-V$ volts, which charge is utilized after time t_2 in read out if the selected cell 12 is connected to the read amplifier 27, as will be explained hereafter.

At the time t_0^1 , the clock pulse ϕ returns to ground and the load capacitor 33 is discharged to the ground of the clock pulse, as previously described, during the first portion of the following cycle, such as t_0^1 to t_1^1 . Also at t_0^1 , the previously selected Y address bus, such as Y_1 , is de-energized, which turns off the selected transistor 36 and thus isolates the charge (ground) on the selected storage capacitor 41 for use in a later cycle.

If the storage capacitor 41 in the addressed memory cell 12 had previously been charged to a substantial negative voltage (representing the storage of a binary "0"), the load capacitor 34 will be charged after time t_1 faster than the load capacitor 33 in this case since the load capacitor 34 is charged from the clock pulse ϕ through the load transistor 78, and also from the charged storage capacitor 41 after the selected Y_1 transistor 36 turns ON.

Thus, the load capacitor 34 will be charged to the threshold voltage of the first transistor 66, and will switch the first transistor ON before the second transistor 67 reaches its threshold voltage. With the first transistor 66 ON and the second transistor 67 OFF, the load capacitor 34 and the storage capacitor 41 continue to charge from the clock pulse ϕ while the opposite load capacitor 33 is discharged to ground level by the now ON transistor 66.

When a time corresponding to t_2 has been reached, the storage capacitor 41 has been fully charged, or recharged, to a potential $-V_M$, representing a predetermined portion of the clock voltage applied through the load transistor 78 to the capacitor 41 in parallel with the load capacitor 34.

This charge $-V_M$ represents the desired level for storing a binary "0" in a cell 12 on the left side 18 of the circuit. This recharging to $-V_M$ restores the desired data charge on the capacitor such as 41 during each refresh cycle, thus compensating for any charge leakage which may have occurred

since the charge, or data, was entered, or since a previous refresh cycle.

At the time corresponding to t_0^1 , at the start of the next cycle, the clock pulse ϕ returns to ground, thus grounding the load capacitor 34, and the selected Y lead such as Y_1 is de-energized, thus isolating the data charge $-V_M$ on the capacitor 41 until a following cycle.

During subsequent cycles of the clock signal ϕ , the data stored in each of the memory cells 12 in the memory 11 is refreshed by one of the plurality of sense-refresh amplifiers 16₁ to 16_n, when its corresponding Y address bus Y_1 to Y_n is selected for energization in an address pattern or cycle desired. The storage capacitors such as 43, 44 on the right side 17 of the circuit are refreshed in exactly the same manner when the corresponding Y lead Y_{k+1} to Y_n is selected, except that on this side, a $-V_M$ charge indicates binary "1" and 0 volts indicates binary "0".

Considering now the writing process in more detail, the X- and Y- decoders (not shown) select a particular crosspoint in the X-Y memory matrix; for example, the transistor 36 and capacitor 41 for the combination of the X_1 I/O bus and the Y_1 address bus. In the example illustrated at the left of Fig. 2 (time t_0 to t_0^1), it is required to write a "1" at the crosspoint X_1, Y_1 . As previously explained, in this case, the X-decoder turns ON the X_1 input gating transistor 21₁ at time t_0 , and a "write" input is applied at the terminal 23 of the write amplifier 22, thus connecting the data input 24 to the X_1 bus and to node 2 of the sense-refresh amplifier 16₁. If a "1" is to be stored in the X_1, Y_1 capacitor 41 in the circuit illustrated in Fig. 3, a $-V$ data input signal is applied at the data input terminal 24 at time t_0 , thus driving the right half of the X_1 bus and node 2 negative as shown in the left portion of Fig. 2E.

From time t_0 to t_1 , this negative data input is gated to the ground of the clock pulse ϕ through the load transistor 77. At time t_1 , the clock pulse ϕ goes negative, and the combination of the clock pulse signal and the input data signal (both negative voltages) quickly charges the load capacitor 33 to a value exceeding the threshold voltage of the transistor 67 so as to turn that transistor ON.

At the time t_1 , the X_1, Y_1 transistor 36 also turns ON to connect the storage or memory capacitor 41 to node 1 and the clock pulse ϕ through the left load transistor 78, as previously explained in the description of the sense-refresh amplifier circuit. However, even if the capacitor 41 has been storing a $-V$ charge from previous writing and refresh cycles, the combination of the capacitor 41 and the clock pulse ϕ does not charge the left load capacitor 34 as fast as the com-

5 bination of the clock pulse and the input data signal charges the right load capacitor 33, thus the left transistor 67 invariably turns ON first when a negative write signal is applied at the data input terminal 24, regardless of the previous state of the memory capacitor 41. In this way, a fresh data input signal during a write cycle effectively obliterates the previous data-related charge on the capacitor 41.

10 As previously explained, once the left transistor 67 turns ON (rather than the right transistor 66), the transistor 66 cannot turn ON and the capacitors 41 and 34 discharge to ground 76 through the left transistor 67. Thus, at the end of this writing cycle (time t_0), the memory capacitor 41 is essentially uncharged, which in the example of Fig. 3 represents storage of a binary "1" at the crosspoint X_1, Y_1 . Thus, it should be appreciated that the sense-refresh amplifier 16, effectively inverts the input data signal stored in any cell 12 to the left of the amplifier 16, such that an input binary "1" signal ($-V$) is stored on the left bank capacitors, such as 41, as 0 volts. As will be explained later, during read out, the amplifier 16, again inverts the signal on the capacitor 41, such that a minus voltage, or "1" appears at the output terminal 31.

30 When a "0" is to be stored on a left bank capacitor such as 41 during a writing cycle, a "0" or ground potential is applied to the data input terminal 24 and connected to node 2 through the transistor 21, from a time corresponding to t_0 for a full cycle of the clock signal ϕ . In this case, at a time corresponding to t_1 , when the clock pulse goes negative and a selected Y transistor such as 36 turns ON, the clock signal ϕ at the right of the amplifier 16, is grounded to the 0 volt data signal at terminal 24. Thus, the right load capacitor 33 does not charge sufficiently to turn ON the left transistor 67, and the clock pulse charges the capacitors 34 and 41 in parallel until the right transistor 66 turns ON, after which the memory capacitor 41 continues to charge for the remainder of the cycle to a given fraction of the clock voltage, $-V_M$, which represents storage of a binary "0" in any of the left bank memory cells 12. Thus, the memory capacitor such as 41 charges fully to store a minus voltage regardless of its previous state when a 0 input is applied to the write input terminal 24 during a writing cycle, and the 0 input data signal is also inverted by the amplifier circuit 16.

60 When storing data signals on the right bank capacitors, such as 43 and 44, a charge corresponding to the input data signal is stored, rather than the complement. For example, if a "1" is to be stored on the capacitor 44 at the X_1, Y_{1+1} crosspoint, a $-V$ data input is applied to node 2 as pre-

viously described. At a time corresponding to t_1 , ϕ goes negative and the combination of the clock voltage and applied negative data signal turns the left transistor 67 ON before the right transistor 66 can turn ON, regardless of the previous state of the memory capacitor 44. Thus, the capacitor 44 is free to charge fully through the transistor 39 during the remainder of the cycle, to store a negative voltage indicating a binary "1".

75 If a binary "0" is to be stored on the capacitor 44, a ground input is applied to node 2 and the left transistor 67 cannot turn ON. Instead the right transistor 66 is selected, which further serves to ground the capacitor 44 when the selected Y transistor 39 turns ON, at a time corresponding to t_1 . Thus, the capacitor 44 stores essentially zero volts, or a binary "0" at the end of the writing cycle, regardless of its previous state.

80 In this manner, the sense-refresh amplifiers, such as 16, set the addressed memory cell 12 in accordance with the data input at 24 during each write cycle by charging or discharging the memory capacitors such as 41 to 44, regardless of their previous states, while inverting the data stored in the left half 14 of the array.

90 To read out the data stored on a selected one of the memory capacitors, such as 41 to 44, the state of the load capacitor 33 is effectively sampled after the refresh portion of the cycle has been completed, as from time t_2 to t_3 in the example previously discussed in connection with Figs. 2C and 2D. In that example, the Y_2 address bus is energized at time t_1 (Fig. 2C) and the charge stored on the memory capacitor 42 of the Y_2, X_1 cell 12 is refreshed during the time t_1 to t_2 as previously described, either to store a preset charge $-V_M$ from the clock pulse representing a binary "0", or to be effectively grounded through the transistor 67, representing binary 1. In both cases, the load capacitor 33 at the time t_2 stores a voltage inverse to that of the memory capacitor 42 as described in connection with the refresh operation.

105 At the time t_2 , on read out, the selected X-gating transistor 21 is turned ON, such as transistor 21, for the X_1 (Fig. 2D). This connects the X_1 bus to the input 29 of the read amplifier 27, as previously described, and when a "read" signal is also applied to the terminal 28 of that amplifier, the output signal at the terminal 31 represents the signal then stored on the load capacitor 33, which in turn represents the complement of the signal stored on the selected X_1, Y_2 crosspoint memory capacitor 42.

120 Thus, an inverted data signal stored on a left bank capacitor such as 42, as described in the previous sections, is effectively re-inverted by the sense-refresh amplifier 16 on read out, in that the signal on node 2 (capa-

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citor 33) at the end of the refresh portion of the cycle is the complement of the signal stored on the memory capacitor 42.

When a right bank memory cell 12 is to be read, for example capacitor 44 associated with the Y_{k+1} , X_1 crosspoint, the charge on the capacitor 44 at the end of the refresh portion of the cycle (corresponding to time t_2) is of the same sense as that on the load capacitor 33, as previously described. That is, both are effectively grounded through transistor 66 when a "0" has been stored, or both are charged negative from the clock pulse ϕ when a "1" has been stored (transistor 67 is ON instead of transistor 66). In this case, when the transistor 21₁ is turned ON at a time corresponding to t_2 to read, the output signal at terminal 31 represents the combination of the charges on the load capacitor 33 and the selected memory capacitor 44, which as explained above are either both 0 volts for binary "0", or both a minus voltage for binary "1".

After reading, in all cases, at the next time corresponding to t_0 , the previously selected column transistor such as 36-39 turns OFF to isolate and preserve the signal stored on the corresponding memory capacitor 41-44, and the clock pulse ϕ returns to ground so as to discharge to the ϕ pulse ground whichever load capacitor 33 or 34 had been charged in the previous cycle.

During each read cycle, all memory capacitors in the selected column $Y_1 \dots Y_i$ are refreshed, although only the capacitor at the selected X crosspoint is read after the refresh portion of the cycle. On writing, all memory capacitors in the selected column are also refreshed, except for the one at the selected X crosspoint where fresh data is entered as previously described.

In view of the foregoing description of the operation of two specific embodiments of the invention, it should be apparent that an extremely fast acting, random-access memory has been provided, using a single capacitance (such as 41) and access transistor (such as 36) for each memory cell 12, with a minimum of circuit components and power required, and with only a single pulse of a single-phase clock required for the operation of the memory system (other than address inputs).

One significant advantage, and saving in circuit components conductors, and integrated circuit real estate, resides in the use of the right half 17 of each I/O bus, such as X_1 , for all external input and outputs to the memory ("write" amplifier 22 and "read" amplifier 27), and using the sense/refresh amplifiers such as 16, as inverters to write on the left bank of cells and to reinvert upon read out from the left bank 18.

Thus, in essence, the left half 18 of each I/O bus, such as X_1 , serves only as an input/

output conductor or bus to connect any selected memory cell 12 in the left bank to node 1 of the amplifier 16₁, but is otherwise not connected or connectable to any external circuits at its outer end. By contrast, the right half 17 of the I/O bus serves as an I/O conductor for the right bank of cells, connected at its inner end to node 2 of the inverter/amplifier 16₁, but is also connectable at its outer end (through the X-decoder gate or transistor 21₁) to the external read and write circuits, which constitute the only data inputs to and outputs from the memory.

Although, the invention has been described using p-channel, enhancement-mode transistors, wherein negative clock and data signals are utilized to turn ON the transistors to manipulate the data, other types of field-effect transistors using the inverse of such signals, or using positive and ground signals to operate the transistors, as well as complementary transistor systems using a mixture of p- and n-channel devices may be used.

Further details on the construction and operation of such field-effect transistor circuits, as well as examples of decoder circuits and gates which may be used in combination with this invention are described in G.B. Patent Specification Nos. 1,302,105, 1,310,930, 1,312,502 and 1,324,793.

WHAT WE CLAIM IS:—

1. A memory system including a memory cell having capacitance for storing charge representative of binary data, and means for refreshing said data including a first and a second terminal, said first and second terminals being connected respectively to a first and a second capacitance of substantially equal value, said refreshing means being for providing on said terminals an initial ground potential and a second potential in response, in operation, to a clock signal having a first and second value respectively, said memory capacitance being connectable in parallel to one of said first and second capacitances, said one capacitance of the parallel combination of said memory capacitance and said one capacitance being in response to said second value clock signal charged from said initial ground potential towards said second potential at a slower or a faster rate than the charging rate of the other capacitance dependent upon the initial state of said memory capacitance, and said refreshing means being adapted to restore to said memory capacitance said initial state in response to the differential charging rate between said first and second capacitances.

2. A system as claimed in claim 1 wherein said refreshing means includes a first and a second gating device each having two controlled electrodes and a control electrode, the

citor 33) at the end of the refresh portion of the cycle is the complement of the signal stored on the memory capacitor 42.

When a right bank memory cell 12 is to be read, for example capacitor 44 associated with the Y_{k+1} , X_1 crosspoint, the charge on the capacitor 44 at the end of the refresh portion of the cycle (corresponding to time t_2^1) is of the same sense as that on the load capacitor 33, as previously described. That is, both are effectively grounded through transistor 66 when a "0" has been stored, or both are charged negative from the clock pulse ϕ when a "1" has been stored (transistor 67 is ON instead of transistor 66). In this case, when the transistor 21₁ is turned ON at a time corresponding to t_2^1 to read, the output signal at terminal 31 represents the combination of the charges on the load capacitor 33 and the selected memory capacitor 44, which as explained above are either both 0 volts for binary "0", or both a minus voltage for binary "1".

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In view of the foregoing description of the operation of two specific embodiments of the invention, it should be apparent that an extremely fast acting, random-access memory has been provided, using a single capacitance (such as 41) and access transistor (such as 36) for each memory cell 12, with a minimum of circuit components and power required, and with only a single pulse of a single-phase clock required for the operation of the memory system (other than address inputs).

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Thus, in essence, the left half 18 of each I/O bus, such as X_1 , serves only as an input/

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Although, the invention has been described using p-channel, enhancement-mode transistors, wherein negative clock and data signals are utilized to turn ON the transistors to manipulate the data, other types of field-effect transistors using the inverse of such signals, or using positive and ground signals to operate the transistors, as well as complementary transistor systems using a mixture of p- and n-channel devices may be used.

Further details on the construction and operation of such field-effect transistor circuits, as well as examples of decoder circuits and gates which may be used in combination with this invention are described in G.B. Patent Specification Nos. 1,302,105, 1,310,930, 1,312,502 and 1,324,793.

WHAT WE CLAIM IS:—

1. A memory system including a memory cell having capacitance for storing charge representative of binary data, and means for refreshing said data including a first and a second terminal, said first and second terminals being connected respectively to a first and a second capacitance of substantially equal value, said refreshing means being for providing on said terminals an initial ground potential and a second potential in response, in operation, to a clock signal having a first and second value respectively, said memory capacitance being connectable in parallel to one of said first and second capacitances, said one capacitance of the parallel combination of said memory capacitance and said one capacitance being in response to said second value clock signal charged from said initial ground potential towards said second potential at a slower or a faster rate than the charging rate of the other capacitance dependent upon the initial state of said memory capacitance, and said refreshing means being adapted to restore to said memory capacitance said initial state in response to the differential charging rate between said first and second capacitances.

2. A system as claimed in claim 1 wherein said refreshing means includes a first and a second gating device each having two controlled electrodes and a control electrode, the



control electrode of each said device being connected to a respective one of said terminals and one of the controlled electrodes of the other said device, and the other one of said controlled electrodes of each said device being connected together, said first and second gating devices being adapted to respond to said differential charging rate between said first and second capacitances to restore said initial state to said memory capacitance.

3. A system as claimed in claim 1 or 2 wherein said refreshing means includes means for receiving said clock signal and a pair of resistive means, each for connecting said receiving means to a respective one of said terminals for providing thereat said initial ground potential and said second potential.

4. A system as claimed in claim 2 wherein said refreshing means includes a pair of resistive means each for connecting a constant potential to a respective one of said first and second terminals, and a third and a fourth gating device, each having two controlled electrodes and a control electrode, each said controlled electrode of said third and fourth gating devices being coupled to a respective said controlled electrode of said first and second gating devices and the control electrodes thereof being coupled together and being for receiving said clock signal, said pair of resistive means and said third and fourth gating devices being adapted to cooperate to provide said initial ground potential and said second potential on said first and second terminals.

5. A system as claimed in claim 3 or 4 wherein each said resistive means comprises a gating device.

6. A system as claimed in any one preceding claim wherein said memory cell comprises a gating device having two controlled electrodes and a control electrode, said control electrode being connected to an address bus for enabling said gating device to connect said memory capacitance in parallel with said one capacitance, one of said controlled electrodes being connected to one of said first and second terminals, the other controlled electrode having said memory capacitance and being connected to an address bus for enabling an adjacent memory cell.

7. A system as claimed in any one preceding claim including a first and a second plurality of said memory cells, a first conductor for connecting said first plurality of memory cells to said first terminal and a second conductor for connecting said second plurality of memory cells to said second

terminal, the memory capacitance of a selected said cell of said first plurality of cells being, in operation, connected in parallel to said first capacitance, said first capacitance of the parallel combination of said memory capacitance and said first capacitance being in response to said second value clock signal charged from said initial ground potential towards said second potential at a slower or a faster rate than the charging rate of said second capacitance dependent upon the initial state of said memory capacitance, and said refreshing means being adapted to invert input data to be written on said selected memory cell of said first plurality in response to the differential charging rate between said first and second capacitances.

8. A system as claimed in claim 7 including a plurality of address buses for selectively addressing said first and second pluralities of memory cells to connect a selected said memory cell therefrom to said first or said second conductor, each of said memory cells including a gating device having two controlled electrodes and a control electrode, said control electrode being connected to one of said address buses for enabling said gating device to connect the memory capacitance thereof to said refreshing means, one of said controlled electrodes being connected to one of said first and second terminals, the other controlled electrode having said memory capacitance and being connected to an adjacent one of said address buses for enabling an adjacent one of said memory cells.

9. A method of refreshing binary data on a memory cell having capacitance for storing charge representative of said data, said method including providing an initial ground potential to a first and a second capacitance of substantially equal value in response to a first value clock signal, providing a second potential to said first and second capacitances in response to a second value clock signal, connecting said memory capacitance in parallel with one of said capacitances such that said one capacitance of the parallel combination of said memory capacitance and said one capacitance is in response to said second value clock signal charged from said initial ground potential towards said second potential at a slower or faster rate than the charging rate of the other said capacitance dependent upon the initial state of said memory capacitance, and refreshing said memory cell to restore thereon said initial state in response to the differential charging rate between said capacitances.

10. A memory system substantially as



herein described with reference to the accompanying drawings.

11. A method of refreshing binary data on a memory cell substantially as herein described with reference to the accompanying drawings.
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Printed for Her Majesty's Stationery Office by Burgess & Son (Abingdon), Ltd.—1976.
Published at The Patent Office, 25 Southampton Buildings, London, WC2A 1AY
from which copies may be obtained.

