CLAIMS

1. A data path interface circuit for a memory, comprising:

a writing path module, connected to an internal port and an external port of the memory respectively, and configured to transmit data to the internal port from the external port;

a reading path module, connected to the internal port and the external port respectively, and configured to transmit the data to the external port from the internal port;

a first delay module, connected to the external port and the internal port respectively, and configured to obtain the data from the external port or the internal port, perform delay processing on the data, and transmit delayed data to the writing path module or the reading path module respectively; and

a delay control module, connected to the first delay module and configured to receive a signal instruction input by an external electronic device and generate a control signal on an output end, according to the signal instruction, said control signal being configured to control delay time for the first delay module to perform the delay processing;

wherein the first delay module comprises:

a selection unit, input ends of the selection unit being connected to the external port and the internal port respectively, and a control end of the selection unit being configured to receive the signal instruction; and

a temporary storage unit, a data input end of the temporary storage unit being connected to an output end of the selection unit, an output end of the temporary storage unit being connected to the writing path module and the reading path module, and a control end of the temporary storage unit being connected to the output end of the delay control module for receiving the control signal and being configured to store a signal on its data input end in response to the control signal.

2. The data path interface circuit of claim 1, wherein the temporary storage unit comprises at least one of a latch, a flip-flop or a register; and a control end of the temporary storage unit comprises at least one of a clock drive end, a set end or a reset end.

3. The data path interface circuit of claim 1, wherein the writing path module comprises:

a writing buffer unit, an input end of the writing buffer unit being connected to an output end of the temporary storage unit, an output end of the writing buffer unit being connected to the internal port, and a control end of the writing buffer unit being configured to receive the signal instruction; and

wherein the reading path module comprises:

a reading buffer unit, an input end of the reading buffer unit being connected to the output end of the temporary storage unit, an output end of the reading buffer unit being connected to the external port, and a control end of the reading buffer unit being configured to receive the signal instruction.

4. The data path interface circuit of claim 1, wherein the delay control module comprises:

a delay chain, an input end of the delay chain being configured to receive the signal instruction, the delay chain being configured to delay and output the signal instruction; and

a control signal generation circuit, an input end of the control signal generation circuit being connected to an output end of the delay chain, an output end of the control signal generation circuit being connected to the control end of the temporary storage unit, and the control signal generation circuit being configured to generate a control signal according to a signal output from the delay chain.

5. The data path interface circuit of claim 4, wherein the delay chain is a programmable delay chain.

6. The data path interface circuit of claim 4, wherein the control signal comprises at least one of a pulse signal, a signal rising edge or a signal falling edge.

7. The data path interface circuit of claim 1, wherein the first delay module and the delay control module are configured with two operating modes comprising a delay mode and a quick mode; wherein in a case of the delay mode, the first delay module and the delay control module are valid; in a case of the quick mode, the delay control module is invalid, and transmission delay on the data by the first delay module is zero; and wherein the data path interface circuit further comprises:

a mode selection module, connected to the first delay module and the delay control

module respectively, and configured to receive the signal instruction, and control the operating modes of the first delay module and the delay control module according to the signal instruction.

8. The data path interface circuit of claim 7, wherein the signal instruction comprises at least one of a write instruction, a read instruction or a mode selection coding instruction.

9. A memory, comprising:

the data path interface circuit of any one of claims 1 to 8;

a data processing module, connected to the external port of the data path interface circuit, and configured to process the data; and

a memory block, connected to the internal port of the data path interface circuit, and configured to store the data.

10. The memory of claim 9, further comprising:

a second delay module, connected to the memory block, and configured to receive the signal instruction and generate a memory block control signal according to the signal instruction, wherein the memory block control signal is configured to control time when the data enters the memory block.

11. The memory of claim 10, wherein delay time generated on the memory block control signal by the second delay module is matched with the delay time generated on the data by the data path interface circuit.

12. The memory of claim 9, wherein the memory block comprises at least two memory sub blocks connected to a same memory block control circuit.

13. The memory of claim 12, wherein the memory block control circuit comprises at least one of a row decoding circuit, a column decoding circuit or a redundancy circuit.

14. The memory of claim 12, wherein the memory comprises a plurality of data path interface circuits and a plurality of memory blocks, the data path interface circuits being arranged in one-to-one correspondence to the memory blocks;

wherein external ports of the plurality of data path interface circuits are connected to a same data processing module, and internal ports of the plurality of data path interface circuits

are connected to a plurality of the memory sub blocks.

15. The memory of claim 14, wherein transmission time of the data from an output end of the data processing module to any of the memory sub blocks is matched with each other.

16. The memory of claim 14, wherein transmission time of the data from any of the memory sub blocks to the data processing module is matched with each other.

17. The memory of claim 14, wherein the memory comprises two data processing modules connected to the plurality of data path interface circuits respectively;

wherein when the memory is in a mode that one data processing module is valid, the data processing module is controlled to enable for transmitting data; and when the memory is in a mode that multiple data processing modules are valid, a set number of the data processing modules are controlled to enable for synchronously transmitting data to the different memory blocks.

18. A memory system, comprising:

the memory of any one of claims 9 to 17;

an electronic device; and

a processing module controller, connected to the memory and the electronic device respectively, and configured to enable a corresponding number of the data processing modules in the memory according to system information of the electronic device.