



ABSTRACT

Title: Configurable logic array

A configurable semi-conductor integrated circuit comprising an area thereof formed with a plurality of logic circuits at discrete sites or cells (cc) respectively defining a matrix array of cells. The matrix array of cells is subdivided at least into zones (each comprising a matrix array of cells) and further comprising a porting arrangement for each zone and a hierarchical routing resource structure comprising:-

- (i) global connection parts (G, X) having selectable connections with the porting arrangement of each zone,
- (ii) medium connection parts (M) extending from the porting arrangement and selectably connectable with at least some of the cells in a zone, and
- (iii) local direct connection paths comprising a restricted signal=translation system.

The application also describes a configurable semi-conductor integrated circuit comprising a matrix array of core cells (cc), each of the cells having a first simple function in common and at least one subsidiary function, there being at least two different subsidiary functions, the core cells being grouped in tiles comprising a matrix array of the core cells

smaller than the whole array and wherein each tile has at least one of each different subsidiary functions and wherein the tiles of core cells are arranged so as to uniformly cover the array. Preferably there are four cells to a tile and the preferred subsidiary functions are:- wired-OR, XOR, D-type flip flop and latch function.

The above features are preferably combined to produce a particularly advantageous construction of configurable semi-conductor integrated circuit.