CLAIMS

1. A semiconductor device, comprising:

a planar silicon layer formed on a silicon substrate;

first and second pillar-shaped silicon layers formed on the planar silicon layer;

a gate insulating film formed around the first pillar-shaped silicon layer;

a first gate electrode formed around the gate insulating film;

a second gate insulating film formed around the second pillar-shaped silicon layer;

a second gate electrode formed around the second gate insulating film;

a gate line connected to the first and second gate electrodes, wherein a center line of the gate line is displaced by a predetermined distance from an imaginary line joining a center point of the first pillar-shaped silicon layer to a center point of the second pillar-shaped silicon layer; and wherein the thickness of each of the first and second gate electrodes being smaller than half of a distance between the first pillar-shaped silicon layer and the second pillar-shaped silicon layer so that a portion of the gate line between the first and second pillar-shaped silicon layers also mutually connects the first and second gate electrodes, the predetermined distance being a predetermined

amount excluding zero;

an upper surface of the gate line being located at a lower position than upper surfaces of the first and second gate electrodes;

a first n-type diffusion layer formed in an upper portion of the first pillar-shaped silicon layer;

a second n-type diffusion layer formed in a lower portion of the first pillar-shaped silicon layer and in an upper portion of the planar silicon layer;

a first p-type diffusion layer formed in an upper portion of the second pillar-shaped silicon layer; and

a second p-type diffusion layer formed in a lower portion of the second pillar-shaped silicon layer and in a~~n~~ second upper portion of the planar silicon layer.

2. The semiconductor device according to claim 1, wherein the thickness of an~~the~~ insulating film sidewall formed on a side wall of the first n-type diffusion layer is larger than the total thickness ~~the sum of the thicknesses~~ of the first gate electrode.

3. The semiconductor device according to claim 1, further comprising silicides formed on the first and second n-type diffusion layers and the first and second p-type diffusion layers.