159159

G00002

METHOD AND APPARATUS FOR FLIP-CHIP PACKAGING PROVIDING TESTING CAPABILITY

TECHNICAL FIELD

The present invention relates generally to packaging of semiconductor dice and, more specifically, to packaging of flip chip configured semiconductor dice employing an interposer substrate having recesses in one or both sides thereof for receiving discrete conductive elements projecting from the semiconductor dice.

BACKGROUND ART

Chip-On-Board ("COB") or Board-On-Chip ("BOC") technology is used to attach a semiconductor die directly to a carrier substrate such as a printed circuit board ("PCB"), or an interposer may be employed and attachment may be effected using flip chip attachment, wire bonding, or tape automated bonding ("TAB").

Flip chip attachment generally includes electrically and mechanically attaching a semiconductor die by its active surface to an interposer or other carrier substrate using a pattern of discrete conductive elements therebetween. The discrete conductive elements are generally disposed on the active surface of the die during fabrication thereof, but may instead be disposed on the carrier substrate. The discrete conductive elements may comprise minute conductive bumps, balls or columns of various configurations. Each discrete conductive element is placed corresponding to mutually aligned locations of bond pads (or other I/O locations) on the semiconductor die and terminals on the carrier substrate when the two components are superimposed. The semiconductor die is thus electrically and mechanically connected to the carrier substrate by, for example, reflowing conductive bumps of solder or curing conductive or conductor-filled epoxy bumps. A dielectric underfill may then be disposed between the die and the carrier substrate for environmental protection and to enhance the mechanical attachment of the die to the carrier substrate.

Wire bonding and TAB attachment techniques generally begin with attaching a semiconductor die by its back side to the surface of a carrier substrate with an appropriate adhesive, such as an epoxy or silver solder. In wire bonding, a plurality of fine wires are discretely attached to bond pads on the semiconductor die and then

extended and bonded to corresponding terminal pads on the carrier substrate. A dielectric encapsulant such as a silicone or epoxy may then be applied to protect the fine wires and bond sites. In TAB, ends of metal traces carried on a flexible insulating tape such as a polyimide are attached, as by thermocompression bonding, directly to the bond pads on the semiconductor die and corresponding terminal pads on the carrier substrate.

Higher performance, lower cost, increased miniaturization of components, and greater packaging density of integrated circuits are ongoing goals of the computer industry. As new generations of integrated circuit products are released, the number of components used to fabricate them tends to decrease due to advances in technology even though the functionality of the products increase. For example, on the average, there is approximately a ten percent decrease in components for every product generation over the previous generation having equivalent functionality.

Recent trends in packaging are moving with increasing rapidity toward flip chip attachment due to improved electrical performance and greater packaging density. However, flip chip attachment is not without problems, such as the high cost for a third metal reroute of bond pads from the middle or periphery of a die to a two-dimensional array which, in turn, may result in overlong and unequal length electrical paths. In addition, many conventional flip chip techniques exhibit a lack of consistent reliability of the interconnections between the chip and the interposer or other carrier substrate as a result of the increased miniaturization as well as difficulties in mutual alignment of the die and carrier substrate to effect such interconnections. Effective rerouting of bond pads may also be limited by die size. Another hindrance to flip chip packaging has been difficulty in electrically testing completed flip chip semiconductor device assemblies using existing test probe equipment. Thus, even if a semiconductor die in the assembly is a so-called "known good die,", the assembly itself may exhibit defects which are not easily detected and which may, even if detected, be at a stage in the fabrication process subsequent to encapsulation, rendering rework of the assembly difficult if not impossible.

Further, flip chip packages for a bumped semiconductor die employing an interposer may be undesirably thick due to the combined height of the die and interposer. This is due to the use in conventional packaging techniques of relatively costly interposers comprising dual conductive layers having a dielectric member

sandwiched therebetween, the bumped semiconductor die resting on and connected to traces of the conductive layer on one side of the interposer and electrically connected to traces of the conductive layer on the opposing side, conductive vias extending therebetween. Finally, underfilling a flip chip attached semiconductor die to a carrier substrate with dielectric filler material can be a lengthy and often unreliable process, and the presence of the underfill makes reworking of defective assemblies difficult if not impossible.

Other difficulties with conventional packages include an inability to accommodate die size reductions, or "shrinks," as a given design progresses through several generations without developing new interposer designs and tooling. As more functionality is included in dice, necessitating a greater number of inputs and outputs (I/Os), decreased spacing or pitch between the I/Os places severe limitations on the use of conventional interposers. In addition, with conventional packages, a die is not tested until package assembly is complete, resulting in excess cost since a defective die or die and interposer assembly is not detected until the package is finished.

For example, United States Patent 5,710,071 to Beddingfield et al. discloses a fairly typical flip chip attachment of a semiconductor die to a substrate and a method of underfilling a gap between the semiconductor die and substrate. In particular, the semiconductor die is attached face down to the substrate, wherein conductive bumps on the die are directly bonded to bond pads on the upper surface of the substrate, which provides the gap between the die and substrate. The underfill material flows through the gap between the semiconductor die and the substrate via capillary action toward an aperture in the substrate, thereby expelling air in the gap through the aperture in the substrate in an effort to minimize voids in the underfill material. However, such an underfilling method still is unnecessarily time consuming due to having to underfill the entire semiconductor die. Further, the flip chip attachment technique disclosed in United States Patent 5,710,071 exhibits difficulties in aligning the conductive bumps with the bond pads on the substrate and requires the expense of having a third metal reroute in the substrate.

Therefore, it would be advantageous to improve the reliability of interconnections between a chip and a carrier substrate such as an interposer by achieving accurate alignment of the interconnections, an improved underfill process, and

the elimination of the necessity for a third metal reroute, while reducing total assembly height in combination with the ability to employ commercially-available, widely-practiced semiconductor device fabrication techniques and materials as well as existing test equipment.

DISCLOSURE OF INVENTION

The present invention relates to methods and apparatus for assembling, testing and packaging individual and multiple semiconductor dice with an interposer substrate in a flip chip type arrangement and, further, the present invention relates to an interposer substrate having multiple recess patterns for mounting semiconductor dice with differently spaced and sized conductive bump configurations. The present invention provides a flip chip semiconductor device assembly substantially reduced in height or thickness and with improved mechanical and electrical reliability of the interconnections between a semiconductor die and a carrier substrate in comparison to conventional flip chip assemblies, while also improving the alignment capability of attaching the semiconductor die to the interposer substrate. The present invention also eliminates the requirement of a third metal reroute necessitated in most flip chip assemblies and eliminates the need for underfilling or reduces the time for underfilling if optionally effected. In addition, the present invention facilitates relatively simple and efficient testing of the semiconductor assembly.

The flip chip semiconductor device assembly of the present invention includes an interposer substrate having a first surface and a second surface, wherein at least one of the first surface and the second surface includes multiple recesses formed therein and arranged in at least two different recess patterns for attaching one or more conductively bumped semiconductor die thereto. The one or more conductively bumped semiconductor die may be assembled face (or active surface) down to the interposer substrate in a flip chip type arrangement so that the conductive bumps of the semiconductor die or dice are disposed in a corresponding recess pattern. Conductive elements in the recesses are interconnected by traces to test pads that are exposed proximate a periphery on at least one of the first and second surfaces of the interposer substrate. Such test pads allow easy access for probe testing the electrical integrity of the one or more semiconductor dice mounted to the interposer substrate.

In this manner, the recesses of the at least two different recess patterns are spaced, sized and configured to substantially receive the conductive bumps on the conductively bumped semiconductor die or dice to an extent so that an active surface of each semiconductor die lies immediately adjacent a surface of the interposer substrate. An adhesive element in the form of a liquid or gel adhesive or an adhesive-coated tape may optionally be disposed between the semiconductor die and adjacent interposer substrate surface. As such, there is a reduction in the height of the flip chip assembly due to the conductive bumps being substantially or even completely received in the recesses, which allows for the conductive bumps on the die to be formed larger for increased reliability without increasing the height of the flip chip assembly while also removing the need for a third metal reroute on the semiconductor die. Furthermore, such a flip chip semiconductor device assembly may eliminate the need for underfilling between a semiconductor die and the interposer substrate. If underfilling is employed, the present invention reduces the time for underfilling the assembly and amount of dielectric filler required, since any space in a recess proximate a conductive bump is minimal and vertical space, or standoff, between the semiconductor die and adjacent interposer substrate surface is at least reduced and in some instances greatly reduced due to the presence of the adhesive element.

In a first embodiment, the interposer substrate includes multiple recesses formed in a first recess pattern on the first surface thereof and a second recess pattern on the second surface thereof. The first and second recess patterns are configured such that semiconductor dice having differently spaced and arranged conductive bump configurations thereon (including different sized semiconductor dice) may each be mounted to the interposer substrate. In this manner, the interposer substrate of the first embodiment may facilitate mounting two semiconductor dice thereto by mounting a first die on the first surface of the interposer substrate and mounting a second die on the second surface of the interposer substrate.

In a second embodiment, the interposer substrate includes multiple recesses formed in a first recess pattern and a second, different recess pattern in the first surface thereof. Such first and second recess patterns enable semiconductor dice having differently spaced and arranged conductive bump configurations thereon (including differently sized dice) may be alternatively mounted to a first surface of the interposer

substrate. In this manner, the interposer substrate of the second embodiment facilitates the option of mounting different sized dice and/or semiconductor dice having differently spaced conductive bump configurations.

In a third embodiment, the interposer substrate includes multiple recesses formed in a first and second, different recess pattern on the first surface of the interposer substrate and a third and fourth, different recess pattern on the second surface of the interposer substrate. The first and second recess patterns are configured so that semiconductor dice having differently spaced and arranged conductive bump configurations thereon (including different sized semiconductor dice) may be optionally mounted to a first surface of the interposer substrate and the third and fourth recess patterns are configured so that semiconductor dice having differently spaced and arranged conductive bump configurations thereon (including different sized semiconductor dice) may be optionally mounted to a second surface of the interposer substrate In this manner, the interposer substrate of the third embodiment facilitates the option of mounting different sized dice and/or semiconductor dice having differently spaced conductive bump configurations on both the first surface and the second surface of the interposer substrate.

In a fourth embodiment, the interposer substrate includes multiple recesses formed in first, second, third and fourth different recess patterns in the first surface of the interposer substrate Such recess patterns each are configured and sized so that semiconductor dice having differently spaced conductive bump configurations thereon (including different sized semiconductor dice) may be optionally mounted to a first surface of the interposer substrate. Thus, the interposer substrate of the fourth embodiment facilitates the option of mounting different sized dice and/or semiconductor dice having differently spaced conductive bump configurations on the first surface of the interposer substrate.

The recess patterns referred to in the interposer substrate of the previous embodiments may be staggered and/or aligned with respect to each other. Also, the recess patterns may include some recess patterns that are staggered with respect to each other and some recess patterns that are aligned with respect to each other.

Turning to another aspect of the present invention, the conductive bumps utilized for interconnecting the semiconductor die and the interposer substrate may be

bonded to conductive elements in the recesses by reflowing the conductive bumps, curing the conductive bumps, ultrasonic bonding, or thermal compression, depending upon the bump material employed. In addition, non-solid conductive material such as a conductive paste may be provided on the conductive bumps or within the recesses prior to disposing the conductive bumps in the recesses. Alternatively, unattached conductive bumps may be provided in the conductive paste in the recesses, after which, the die may be aligned and attached to the conductive bumps As such, in addition to providing a more reliable electrical connection between the conductive bumps and the conductive interconnect, the conductive paste compensates for any non-coplanarity due to various conductive bump sizes, recess depths and planarity variation in the surfaces of the semiconductor die and interposer substrate. The adhesive element, as previously mentioned, on the first surface and/or the second surface of the interposer substrate may also compensate and act as a height controller for any irregularities in the coplanarity between a semiconductor die and the interposer substrate.

The flip chip semiconductor device assembly of the present invention may also include relatively large solder balls or other conductive elements attached to a surface of the interposer substrate, interconnecting with the conductive elements and the conductive bumps of the semiconductor die. The solder balls act as interconnects to another substrate, such as a printed circuit board. The flip chip semiconductor device assembly may also be fully or partially encapsulated by an encapsulation material or, the semiconductor die or dice may be left exposed

The flip chip semiconductor device assembly of the present invention may also be assembled at a wafer level, wherein a wafer scale interposer substrate includes at least two different recess patterns. As such, the wafer scale interposer substrate may facilitate assembly with different wafers having different conductive bump configurations which correspond with the at least two different recess patterns in the wafer scale interposer substrate. In this manner, optional wafers with different conductive bump configurations may be attached face down to the interposer substrate with conductive bumps on the wafer disposed and submerged in recesses formed in the wafer scale interposer substrate. The wafer and wafer scale interposer substrate may then be singulated or diced into individual flip chip semiconductor device assemblies Partial Encapsulation of these assemblies may be performed at the wafer level and optionally

completed subsequent to being diced into individual flip chip semiconductor device assemblies.

The interposer substrate may be fabricated from a flexible, tape-like material including at least one flexible dielectric member and at least one conductive member laminated thereto. The at least one flexible dielectric member may include a polyimide layer. The at least one conductive member is patterned into traces by etching or printing conductive ink and may include conductive elements at recess locations in the form of conductive pads linked by the conductive traces to test pads and other conductive pads for external connection of the assembly to other like assemblies or to higher level packaging. The multiple recesses are formed in at least one of the first and second surfaces of the at least one flexible dielectric member by etching, mechanical drilling or punching or laser ablation, wherein each of the recesses extend at least to a portion of a conductive element and are sized and configured to receive the conductive bumps on the semiconductor die. The interposer substrate of the present invention may also be formed of other interposer substrate materials, including non-flexible materials, such as a BT resin, FR4, FR5 and ceramics.

The interposer substrate may comprise a single flexible dielectric member having conductive layers comprising conductive traces on opposing sides thereof or may comprise a single conductive layer laminated between two dielectric members. In either instance, recesses may extend from either side of the interposer substrate through a dielectric member to expose portions of conductive elements.

In another aspect of the present invention, the flip chip semiconductor device assembly is mounted to a circuit board in a computer or a computer system. In the computer system, the circuit board is electrically connected to a processor device which electrically communicates with an input device and an output device.

Other features and advantages of the present invention will become apparent to those of skill in the art through a consideration of the ensuing description, the accompanying drawings and the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

While the specification concludes with claims particularly pointing out and distinctly claiming that which is regarded as the present invention, the advantages of this

invention may be ascertained from the following description of the invention when read in conjunction with the accompanying drawings, wherein:

FIG. 1 is a simplified top view of a first embodiment of an interposer substrate illustrating a first recess pattern and a second, different recess pattern (shown in broken lines) formed in the interposer substrate according to the present invention;

FIG. 2 is a simplified cross-sectional side view taken along line 2 in FIG. 1, illustrating multiple recesses in a first surface and a second surface of the interposer substrate according to the present invention;

FIG. 3 illustrates mounting a first die and a second die face down to respective first and second surfaces of the interposer substrate to form a flip chip semiconductor device assembly, according to the present invention;

FIG. 4 illustrates applying dielectric filler material to the flip chip semiconductor device assembly according to the present invention;

FIG. 5 illustrates testing the flip chip semiconductor device assembly according to the present invention,

FIG. 6 illustrates mounting a flip chip semiconductor device assembly according to the present invention to another substrate with conductive elements therebetween;

FIG. 7 illustrates applying encapsulation material with a dispenser and encapsulation member to the semiconductor assembly according to the present invention mounted to another substrate as shown in FIG. 6;

FIG. 8 illustrates a fully encapsulated flip chip semiconductor device assembly mounted to another substrate as shown in FIG. 6;

FIG. 9 is a simplified top view of a second embodiment of an interposer substrate according to the present invention, illustrating a first recess pattern and a second, different recess pattern formed in the same surface of the interposer substrate;

FIG. 10 is a simplified cross-sectional side view taken along line 9 in FIG. 9;

FIG. 11 is a simplified cross-sectional side view of a semiconductor die mounted face down to an interposer substrate with conductive bumps disposed in one of the first recess pattern and the second recess pattern to form a flip chip semiconductor device assembly according to the present invention under test;

FIG 12 is a simplified cross-sectional side view of multiple flip chip semiconductor device assemblies of the second embodiment attached with conductive

elements extending therebetween with the bottom interposer substrate attached to another substrate, according to the present invention;

FIG. 13 is a simplified top view of a third embodiment of an interposer substrate, illustrating a first, second, third (shown in broken lines) and fourth (shown in broken lines) recess pattern formed in the interposer substrate, according to the present invention;

FIG. 14 is a simplified top view of a fourth embodiment of an interposer substrate, illustrating first, second, third and fourth different recess patterns formed in a first surface of an interposer substrate, according to the present invention;

FIG. 15 is a simplified block diagram of the semiconductor assembly of the present invention integrated in a computer system,

FIG. 16 is a simplified cross-sectional side view of a fifth embodiment of a semiconductor device assembly according to the present invention; and

FIG. 17 is a simplified side view of a sixth embodiment of a semiconductor device assembly according to the present invention.

BEST MODE OR MODES FOR CARRYING OUT THE INVENTION

Embodiments of the present invention will be hereinafter described with reference to the accompanying drawings. It would be understood that these illustrations are not to be taken as actual views of any specific apparatus or method of the present invention, but are merely exemplary, idealized representations employed to more clearly and fully depict the present invention than might otherwise be possible. Additionally, elements and features common between the drawings figures retain the same numerical designation.

FIGS. 1 and 2 depict a first embodiment of an interposer substrate 110 of the present invention, wherein FIG. 1 illustrates a simplified top plan view of interposer substrate 110 and FIG. 2 illustrates a simplified cross-sectional view of interposer substrate 110 taken along line 2 in FIG. 1. Interposer substrate 110 includes a first surface 112 and a second surface respective 114, wherein each surface may include multiple recesses 120 formed therein and respective first and second die attach sites 142 and 144, respective first and second adhesive elements 152 and 154 provided on the respective first and second die attach sites 142 and 144, and test pads 134 exposed

proximate a periphery 116 of the first surface 112 and second surface 114 of the interposer substrate 110.

Interposer substrate 110 is preferably, but not limited to, a flexible substrate, wherein interposer substrate 110 may include a dielectric member 136 disposed between conductive layers each comprising a plurality of conductive elements configured as the aforementioned traces 130. The dielectric member 136 may be formed from any known substrate material and is preferably formed of, by way of example, a flexible laminated polymer or polyimide layer, such as UPILEX, produced by Ube Industries, Ltd., or any other polymer-type layer. The interposer substrate 110 may also be made of a bismaleimide triazine (BT) resin, FR 4, FR 5 or any type of substantially flexible material or non-flexible material, such as a ceramic or epoxy resin.

The conductive layers are preferably formed of copper, or a copper alloy, but may be any suitable electrically conductive material. The conductive layers may include traces 130 extending to conductive pads 132 for connection to conductive bumps of a semiconductor die, conductive pads 133 for use in externally connecting the interposer substrate 110 and test pads 134 for electrical testing of the interposer substrate 110 with one or more semiconductor dice connected thereto Such traces 130 may be formed subtractively as by masking and etching a conductive layer, additively by printing with conductive ink, or by utilizing any suitable method known in the art Once the traces 130 are patterned, a protective solder mask 138 may be formed and patterned over the traces 130, leaving conductive pads 133 exposed for formation of conductive bumps such as solder balls thereon As implied above, the conductive traces, which may, for example, comprise copper or a copper alloy, may be adhered to the dielectric substrate member of UPILEX, BT resin, FR 4 or, FR 5 laminate material, or other substrate materials, using adhesives as known in the art.

According to the first embodiment of the present invention, the first surface 112 and the second surface 114 of interposer substrate 110 each include multiple recesses 120 or vias formed therein in a preselected pattern and a predetermined sizing. Such recesses 120 may be formed by patterning, utilizing a chemical wet etch or dry etch, mechanical drilling or punching, laser ablation, or by utilizing any method known in the art and suitable with the type of materials employed for the interposer substrate 110 Optionally, the recesses 120 are preferably formed to expose at least portions of

conductive pads 132 of the traces 130, which may in some instances comprise the trace ends. It is also contemplated that electroless plating may, optionally, be formed on walls of the recesses 120.

In this manner, each of the multiple recesses 120 extends to a conductive layer, or more specifically, to the traces 130 or conductive pads 132 defining the conductive layer. The conductive traces 130, conductive pads 132 and conductive pads 133 of a conductive layer on the first surface 112 may be interconnected through dielectric member 136 of interposer substrate 110 to other conductive traces 130, conductive pads 132 or conductive pads 133 on the second surface 114 of interposer substrate 110 by conductively plated vias 135, as known in the art. Such conductive pads 133 may be located substantially directly below conductive pads 132 or, optionally, the conductive pads 133 may be at various predetermined locations remote from conductive pads 132 and connected thereto by the conductive traces 130. The conductive traces 130 also extend to test pads 134 proximate the periphery 116 of the interposer substrate 110, test pads being located on one or both surfaces 112 and 114 of interposer substrate 110, as desired It will be understood that elements of the conductive layer on one side of dielectric member 136 will be offset from those on the other side thereof in the areas wherein recesses 120 are formed through dielectric member 136.

Each plurality of recesses 120 in the first surface 112 and the second surface 114 of interposer substrate 110 is formed in a preselected pattern to correspond with a particular bond pad configuration formed on an active surface of a semiconductor die for attaching thereto. In particular, the recesses 120 in FIG. 1 are configured in two groups, defining a first recess pattern 122 and a second, different recess pattern 124 (broken lines), each to correspond with a peripheral semiconductor die bond pad configuration, wherein the first recess pattern 122 may be on the first surface 112 of interposer substrate 110 and the second recess pattern 124 may be on the second surface 114 of interposer substrate 110. The first recess pattern 122 is depicted to encompass a larger periphery than the second recess pattern 124. That is, the recesses 120 of the first recess pattern 122 are closer to a periphery 116 of interposer substrate 110 than the recesses 120 of the second recess pattern 124. Other preselected recess patterns known in the art and having equal utility in the practice of the present invention may, by way of example, include an I-shaped pattern, a single or double central row recess pattern, or

any recess other pattern configured to correspond and match with a any particular semiconductor die bond pad configuration. In addition, the multiple recesses 120 themselves may be formed in any suitable shape, such as square, rectangular or circular, and may include tapered side walls so that the openings or mouths of the recesses 120 are larger than the bottoms thereof. Optionally, through the use of conductive vias 135 connecting conductive traces 130 on one surface of interposer substrate with conductive traces on an opposing surface of interposer substrate 110, a recess of the first recess pattern 122 may be electrically connected to a recess of second recess pattern 124 and to a common test pad 134.

FIG. 2 depicts a first adhesive element152 and a second adhesive element 154 disposed on the first surface 112 and the second surface 114, respectively, of the interposer substrate 110. The first adhesive element 152 and the second adhesive element 154 may be disposed on a center portion of interposer substrate 110 at respective first and second die attach sites 142 and 144 of the respective first and second surfaces 112 and 114 of the interposer substrate 110 at a location or locations on such surfaces unoccupied by the recesses 120. The first and second adhesive elements 152 and 154 may comprise any suitable adhesive material as known in the art, such as epoxy, acrylic, or a polyimide adhesive. Both the first and second adhesive elements 152 and 154 may also comprise, without limitation, a dielectric tape such as a polyimide tape bearing adhesive on both side thereof with the tape surface facing away from interposer substrate 110 being covered with a release layer until adherence to a semiconductor die is desired. Each of first and second adhesive elements 152 and 154 may preferably be, but is not limited to, about 25 μm in thickness.

Referring to FIG. 3, there is illustrated a first semiconductor die 160 and a second semiconductor die 170 mounted face down to the first surface 112 and second surface 114, respectively, of interposer substrate 110 to form a flip chip semiconductor device assembly 180. Semiconductor die 160 includes an active surface 162 and a back surface 164, wherein the active surface 162 includes a plurality of bond pads bearing electrically conductive bumps 166 thereon. Such conductive bumps 166 formed on the first semiconductor die 160 are arranged in a configuration wherein the recesses 120 of the first recess pattern 122 in the first surface 112 of interposer substrate 110 are sized and arranged to correspond with the bump configuration of the first semiconductor die

160 so that the recesses 120 on first surface 112 and the conductive bumps 166 are substantially a mirror image of each other Likewise, the second semiconductor die 170 includes an active surface 172 and a back surface 174, wherein the active surface 172 includes a plurality of bond pads bearing electrically conductive bumps 176 thereon. As with the first die 160, the conductive bumps 176 formed on the second semiconductor die 170 are arranged in a configuration, wherein the recesses 120 of the second recess pattern 124 in the second surface 114 of interposer substrate 110 are sized and arranged to correspond with the bump configuration of the second semiconductor die 170 so that the recesses 120 on second surface 114 and the conductive bumps 176 are substantially a mirror image of each other.

Conductive bumps 166 and 176 preferably comprise, but are not limited to, conductive balls, pillars or columns The material of conductive bumps 166 and 176 may include, but is not limited to, any known suitable metals or alloys thereof, such as lead, tin, copper, silver or gold. Conductive or conductor-filled polymers may also be employed, although gold and PbSn solder bumps are currently preferred. The conductive bumps 166 and 176 may be of uniform characteristics throughout or include, for example, a core of a first material (including a nonconductive material) having one or more conductive layers of other materials thereon. Conductive bumps 166 and 176 are preferably formed on the active surface of each semiconductor die at a wafer level, but such is not required. Conductive bumps 166 and 176 may be formed by metal evaporation, electroplating, stencil printing, gold stud bumping by wire bonders, solder reflow or any suitable method known in the art depending, of course, on the material or materials selected for formation thereof

As depicted in FIG. 3, interposer substrate 110 is mounted to the first semiconductor die 160 and the second semiconductor die 170 to form flip chip semiconductor device assembly 180, wherein such assembly 180 provides that each of the first die 160 and the second die 170 and the respective conductive bumps 166 and 176 of first semiconductor die 160 and second semiconductor die 170 are substantially received in a corresponding recess 120 of respective first recess pattern 122 and second recess pattern 124 of interposer substrate 110 and electrically contact the bond pads 132 at the bottom of each of the recesses 120 The first and second semiconductor dice 160 and 170 may be initially attached by the first and second adhesive elements 152 and 154

on the first and second surfaces 112 and 114, respectively, of the interposer substrate 110 The conductive bumps 166 and 176 on the respective first and second semiconductor die 160 and 170 may then be bonded to the conductive pads 132 or trace ends in the recesses 120 of interposer substrate 110 by, for example, reflowing the conductive bumps 166 and 176 (in the case of solder bumps) and/or curing the conductive bumps 166 and 176 (in the case of conductive or conductor-filled polymer bumps) as known in the art. Other methods of bonding known in the art may utilized, such as ultrasonic or thermal compression, with suitable conductive bump materials

To assist mounting and bonding the first and second dice 160 and 170 to the interposer substrate 110, a non-solid conductive material in the form of a conductive paste 156 may be provided in the recesses 120 as depicted in FIGS. 2 and 3. Such conductive paste 156 may be disposed in each of the recesses 120 by, for example, overlying the first and second surfaces 112 and 114 of interposer substrate 110 with a stencil (not shown) patterned with openings corresponding with the patterns of recesses and spreading the conductive paste 156 over the stencil to fill the recesses 120 in the interposer substrate 110 with a spread member (not shown). The conductive paste 156 may include, but is not limited to, eutectic solder, conductive epoxy, or any conductive material known in the art. The recesses 120 may be partially or completely filled, as desired. Of course, the surfaces of interposer substrate 110 having recesses 120 opening thereon may also merely be filled with conductive paste 156 and the excess removed, without the use of a stencil.

In another method, the conductive paste 156 may first be disposed on the conductive bumps 166 and 176 prior to assembling the respective first and second die 160 and 170 to the interposer substrate 110 by dipping the conductive bumps 166 and 176 in a pool of conductive paste 156 or by depositing, dispensing or otherwise transferring the conductive paste to the conductive bumps 166 and 176. In still another approach, conductive bumps such as 166 or 176, unattached to a semiconductor die, may be disposed in the conductive paste 156 which is in the recesses 120 corresponding to a particular recess pattern. A semiconductor die having a bond pad configuration with a substantially mirror image of the particular recess pattern may then be aligned with and bonded to the conductive bumps

If employed, the conductive paste 156 supplements the conductive bumps 166 and 176 in electrical and mechanical interconnection between both the first and second die 160 and 170 and the traces 130 of interposer substrate 110. Further, the conductive paste 156 ensures mechanical and electrical interconnection even if some of the conductive bumps 166 and 176 are inconsistent in height or the recesses 120 are inconsistent in depth, *i.e.*, non-coplanar, wherein the conductive paste 156 is disposed in the recesses 120 between the conductive pads 132 and the conductive bumps 166 and 176. The conductive bumps 166 and 176 and the conductive paste 156 may then be bonded to the conductive pads 132 or trace ends in the recesses 120 of interposer substrate 110 as previously described.

It will be well appreciated by one skilled in the art that, since the conductive bumps 166 and 176 are substantially received within the recesses 120 of the interposer substrate 110 itself when bonded to conductive pads 132, the height of the semiconductor assembly 160 is minimized. Therefore, the conductive bumps 166 and 176 may be formed of a larger size than in conventional flip chip assemblies without increasing the height of the flip chip semiconductor device assembly 180, resulting in an increase of the electrical and mechanical reliability and performance of the interconnections between the interposer substrate 110 and the first and second semiconductor die 160 and 170. In addition, the first and second adhesive elements 152 and 154 (if used) on the respective first and second surfaces 112 and 114 of the interposer substrate 110 as well as the conductive paste 156 in the recesses 120 (if used) may compensate for any irregularities due to various conductive bump sizes, recess depths and planarity variation in the surfaces of the interposer substrate 110 and the first semiconductor die 160 and second semiconductor die 170

Further, the recesses 120 in the interposer substrate 110 provide an inherent improved alignment capability in comparison to a conventional flip chip type semiconductor assembly because the conductive bumps 166 and 176 easily slide into their respective corresponding recesses 120 to ensure proper alignment with conductive pads 132 and proper attachment of first and second semiconductor dice 160 and 170 to interposer substrate 110 For example, the recesses 120 may be formed in the interposer substrate 110 to be approximately 125 μm in diameter or width and the conductive bumps 156 formed on the semiconductor die 150 may be about 75 μm in diameter or

width. Thus, the dimensions of the recesses 120 accommodate inconsistencies in dimensions and locations of the conductive bumps 156 therein, facilitating die alignment.

As shown in FIG. 4, a dielectric encapsulation material 182 such as what is commonly termed an "underfill" material) may be optionally applied along the periphery of the first die 160 and the second die 170 adjacent interposer substrate 110 to fill around the conductive bumps 166 and 176, respectively. The method employed to apply the encapsulation material 182 is preferably by pressurized dispensing from dispenser 184, but may include any method known in the art, such as gravity and vacuum-assisted dispensing. In this manner, the encapsulation material 182 may be applied to fill any gaps around the conductive bumps 166, 176 in recesses 120 and the area around first and second adhesive elements 152 and 154. Alternatively, a non-flow film or a non-flow paste may be used as the dielectric encapsulation material 182. The non-flow material, which may comprise a thermoset or thermoplastic material, is applied prior to assembly of the semiconductor dice to the interposer substrate 110 The fim or paste, or even a combination of the two forms, allows conductive bumps 166, 176 to penetrate therethrough and effect an electrical connection. Suitable nonconductive films include UF511 and UF527 from Hitachi Chemical, Semiconductor Material Division, Japan. The encapsulation material 182 may be self-curing through a chemical reaction, or a cure accelerated by heat, ultraviolet light or other radiation, or other suitable means in order to form a solid mass in the recesses 120 Such encapsulation material 182 provides enhanced mutual securement of the components of assembly 180, precludes shorting between conductive elements thereof, and protects the conductive elements from environmental elements, such as moisture and dust. Further, compared to underfilling of conventional flip chip assemblies, underfilling of the flip chip semiconductor device assembly 180 of the present invention requires less time since the encapsulation material is only directed to fill any gaps around the conductive bumps 166, 176 in recesses 120 and the area around adhesive elements 152 and 154

FIG. 5 depicts testing the semiconductor assembly 180 of the present invention and specifically testing for the electrical integrity of the interconnections between the interposer substrate and the respective first die 160 and second die 170 as well as functionality of the assembly 180 with test pads 134 provided proximate a periphery 116

of the interposer substrate 110. Such test pads 134 are interconnected with the first die 160 and second die 170 through the traces 130, bond pads 132 and respective conductive bumps 166, 176 so that testing members 188 (one shown) such as test probes may be placed on a surface of each test pad 134 and electrical tests performed by conventional test equipment associated therewith (not shown) to determine proper interconnection of the semiconductor assembly 180. The test pads 134 may be placed on both the first surface 112 and second surface 114 of the interposer substrate 110 at the periphery 116 thereof on a portion of the interposer substrate 110 which is "off-site" from where the first semiconductor die 160 and second semiconductor die 170 are mounted on the interposer substrate 110. Such a test pad configuration enables the sharing of test tooling, and hence reduces cost.

FIG. 6 depicts a flip chip semiconductor device assembly 180 of the present invention interconnected to terminal pads 194 of another substrate 190, such as a circuit board, with conductive elements 192 therebetween. The flip chip semiconductor device assembly 180 may also be stacked with one or more other superimposed semiconductor assemblies 180 with conductive elements 192 therebetween, wherein the bottom assembly 180 may be interconnected to terminals pads 194 substrate 190. Interconnection of the conductive elements 192 to interposer substrates 110 may be provided by bonding to the conductive pads 133 exposed on the either the first or second surfaces 112, 114 of the interposer substrate 110. The conductive elements 192 may be bonded to the bond posts 133 prior or subsequent to dispensing the encapsulation material 182

Once the conductive elements 192 are bonded to the interposer substrate 110 and the encapsulation material 182 has been provided thereto, complete encapsulation of the flip chip semiconductor device assembly 180 may be effected, as depicted in FIGS. 7 and 8. In particular, first semiconductor die 160 and second semiconductor die 170 may then be either partially or fully encapsulated by an encapsulation member 186 with an encapsulation material 182. In the case of partially encapsulating the first die 160 and second die 170, an encapsulation material 182 may be dispensed by dispenser 184 about the periphery thereof so that the back surfaces 164, 174 of the first die 160 and second die 170 are left exposed In the case of fully encapsulating the dice, encapsulation material 182 may be provided by dispensing, spin-coating, glob-topping, transfer

molding, pot molding or any suitable method known in the art It is preferred that such encapsulation material 182 be applied to the back surfaces 164 and 174 of the respective first die 160 and the second die 170 (which may be provided at the wafer level) prior to dispensing encapsulation material 182 about the periphery of first die 160 and the second die 170 in order to facilitate fully encapsulating each of the dice in the semiconductor assembly 180.

FIGS. 9 and 10 depict a second embodiment of the interposer substrate 210 of the present invention, wherein FIG. 9 illustrates a top plan view of a first recess pattern 222 and a second, different recess pattern 224 and FIG. 10 illustrates a cross-sectional side view of the interposer substrate 210 taken along line 10 in FIG. 9 As in the first embodiment, interposer substrate 210 includes a first surface 212 and a second surface 214, an adhesive 252 provided on a die attach site 242 on the first surface 212 and traces 230 extending from the bottoms of multiple recesses 220 to test pads 234 on the interposer substrate 210 As such, the second embodiment is substantially similar to the first embodiment in many respects, except the interposer substrate 210 of the second embodiment includes both a first recess pattern 222 and a second recess pattern 224 formed in the first surface 212 of the interposer substrate 210 It should be noted that a recess 220 of the first recess pattern 222 and a recess 220 of the second recess pattern 224 each expose a portion of a common conductive trace extending peripherally outward from a recess 220 of first recess pattern 222 and past a recess 220 of second recess pattern 224 to a test pad 234.

As depicted in FIG 10, conductive paste 256 may be provided in the recesses, after which a semiconductor die 260 may be mounted and bonded to the interposer substrate 210 as shown in FIG. 11 to provide a flip chip semiconductor device assembly 280 of the present invention. As in the first embodiment, encapsulation material 182 may also be dispensed along a periphery of the die 260 to fill the space around and proximate the conductive bumps 266. Further, testing members 188 may also be used to test the electrical integrity and functionality of the flip chip semiconductor device assembly 280 by placing the testing members 188 directly on the test pads 234 exposed proximate a periphery 216 on the first surface 212 of the interposer substrate 210 Such a locale for testing pads provide easy access and reduce the cost for testing

According to the present invention, the first and second recess patterns 222 and 224 in the first surface 212 of the interposer substrate provide versatility in that semiconductor dice of different size and/or different bumped configurations may optionally be mounted to the first surface of the interposer substrate. Such versatility provides that the first recess pattern 222 and the second recess patterns 224 share a common die attach site, namely, die attach site 242, optionally bearing an adhesive element 252 Further, as in the first embodiment, the recesses 220 are sized and configured to substantially completely receive the conductive bumps 266 of the semiconductor die 260 so that the active surface 262 of the die 260 lies immediately adjacent the first surface 212 of the interposer substrate 210. As such, the semiconductor assembly 280 of the present invention provides a reduced height compared to conventional flip chip assemblies

FIG 12 depicts the semiconductor assembly 280 of the second embodiment stacked with one or more other assemblies 280, wherein the bottom assembly 280 is interconnected to a substrate 290 with conductive elements 292 therebetween The one or more other assemblies 280 may include a semiconductor die 260 with a bumped configuration to fit either the first recess pattern and/or the second recess pattern. As such, the first and second recess pattern 222 and 224 on the first surface 212 of the interposer substrate 210 provides optional attachment of different sized semiconductor die and/or semiconductor die with differently sized and configured recess patterns for mounting to a common die attach site 242 on the interposer substrate 210

As in the first embodiment, the semiconductor assembly 280 attached by conductive elements 292 to the terminal pads 294 of substrate 290, either stacked with other assemblies 280 or individually on the substrate 290, may then be either fully encapsulated or partially encapsulated by an encapsulation member 186 and/or by a dispenser 184, as previously described in FIGS. 7 and 8.

FIG. 13 depicts a top plan view of a third embodiment of the interposer substrate 310 of the present invention. As in the first embodiment, interposer substrate 310 includes a first surface 312 and a second surface 314 with a respective first adhesive element 352 and a second adhesive element 354 thereon, and traces 330 extending from multiple recesses 320 to testing pads 334 exposed on first and second surfaces 312 and 314 of the interposer substrate 310. Each adhesive element 352 and 354 is provided on

a first die attach site 342 and a second die attach site 344 on respective first and second surfaces 312 and 314 of interposer substrate 310 As such, the third embodiment is also similar to the first embodiment in many respects, except the interposer substrate 310 of the third embodiment includes both a first recess pattern 322 and a second recess pattern 326 in the first surface 310 of the interposer substrate 310 and a third recess pattern 324 and a fourth recess pattern 328 in the second surface of the interposer substrate 310 Further, a first adhesive element 352 and a second adhesive element (under first adhesive element 352) are disposed on a center portion of respective first surface 312 and second surface 314 or another portion on the first and second surfaces 312 and 314 unoccupied by recesses 120.

As depicted in FIG. 13, the recesses 320 in the first recess pattern 322 and the second recess pattern 326 may be staggered with respect to the recesses in the third recess pattern 324 and the fourth recess pattern 328 Further, the recesses 320 in the first recess pattern 322 may be relatively more inwardly disposed with respect to the recesses 320 in the second recess pattern 326. Likewise, the recesses 320 in the third recess pattern 324 may be relatively more inwardly disposed with respect to the recesses 320 in the fourth recess pattern 328. With this arrangement, interposer substrate 310 provides versatility to mount different sized die in a stacked arrangement on a single interposer substrate 310. That is, the interposer substrate 310 of the present invention provides that various sized semiconductor die and/or semiconductor die having different conductive bump configurations may be optionally mounted on both the first surface 312 and the second surface 314 of the interposer substrate 310. Further, such optional mounting of semiconductor dice provides that the first recess pattern 322 and second recess pattern 326 share a common die attach site, namely, die attach site 342 as well as common conductive traces 330 extending to a set of test pads 334 Likewise, the third recess pattern 324 and the fourth recess pattern 328 also share a common die attach site, specifically, die attach site 344 as well as common conductive traces 330 extending to a set of test pads 334. The mounting and bonding of the first and second dice may be effected as previously described with respect to the first and second embodiments of the present invention

Further, as in the previous embodiments and as noted above, interposer substrate 310 includes test pads 334 fanned out from recesses 320 proximate a periphery 316 of

interposer substrate 310 and exposed on the first surface 312 and/or the second surface 314 of interposer substrate 310. As such, subsequent to mounting semiconductor die to interposer substrate 310 on the first surface 312 and/or the second surface 314 thereof, the resulting flip chip semiconductor device assembly may be tested to determine the mechanical and electrical integrity of the interconnections between the semiconductor dice and the interposer substrate 310.

FIG. 14 depicts a top plan view of a fourth embodiment of the interposer substrate 410 of the present invention. As in the first embodiment, interposer substrate 410 includes a first surface 412 and a second surface 414 with an adhesive element 452 on the first surface 412, and traces 430 extending from multiple recesses 420 to testing pads 434 exposed on the first surface 412 of the interposer substrate 410. As such, the fourth embodiment is similar to the first embodiment in many respects, except the interposer substrate 410 of the fourth embodiment includes a first recess pattern 422, a second recess pattern 426, a third recess pattern 424 and a fourth recess pattern 428 each formed in the first surface 412 of the interposer substrate 410.

As depicted in FIG. 14, the recesses 420 in the first recess pattern 422 and the second recess pattern 426 may be staggered with respect to the recesses 420 in the third recess pattern 424 and the fourth recess pattern 428. Further, the recesses 420 in the first recess pattern 422 may be inwardly located with respect to the recesses in the second recess pattern 426 opening onto the same conductive traces 430. Likewise, the recesses 420 in the third recess pattern 424 may be inwardly aligned with respect to the recesses in the fourth recess pattern 428 opening onto the same conductive traces 430. With this arrangement, interposer substrate 410 provides versatility to mount different sized die thereon. That is, interposer substrate 410 provides versatility in that various sized semiconductor dice and/or semiconductor dice having different conductive bump configurations may be optionally mounted on the first surface 412 of interposer substrate 410, wherein each recess pattern includes a common die attach site 442. The mounting of the semiconductor die may be employed as previously described with respect to the first and second embodiments of the present invention

Further, as in the previous embodiments, interposer substrate 410 includes test pads 434 fanned out from recesses 420 proximate a periphery 416 of interposer substrate 410 and exposed on the first surface 412 of interposer substrate 410. Test

pads 434 are each common to two recess patterns, as shown in FIG 14. As such, subsequent to mounting semiconductor die to the first surface 412 of interposer substrate 410, the resulting flip chip semiconductor device assembly may be tested to ensure that electrical interconnection has been successfully made and satisfactory functionality is exhibited, as described previously with respect to the first and second embodiments.

Similar to that described in each of the previous embodiments, the interposer substrate of the present invention may also be assembled at a wafer level, wherein the interposer substrate is a wafer scale interposer substrate includes at least two different recess patterns. As such, the wafer scale interposer substrate may facilitate assembly with different wafers having different bumped configurations which correspond with the at least two different recess patterns in the wafer scale interposer substrate. In this manner, optional wafers with different bumped configurations may be attached face (active surface) down to the wafer scale interposer substrate with conductive bumps on the wafer disposed and substantially received in recesses formed in the interposer substrate. The wafer and interposer substrate may then be singulated or diced into individual semiconductor assemblies Partial encapsulation of the semiconductor dice on the wafer or wafers may be performed at the wafer level and completed subsequent to being diced into individual flip chip semiconductor device assemblies according to the present invention.

As illustrated in block diagram form in FIG. 15, an exemplary flip chip semiconductor device assembly 580 of the present invention as previously described herein with respect to various embodiments, mounted to a circuit board 590, such as previously-discussed substrate 190, in an electronic system, such as a computer system 502. In the computer system 502, the circuit board 590 is connected to a processor device 504 which communicates with an input device 506 and an output device 508 The input device 506 may include a keyboard, mouse, joystick, cell phone, PDA system, or any other electronic input device. The output device 508 may include a monitor, a printer, a storage device, such as a disk drive, a cell phone, PDA system, or any other electronic output device. The processor device 504 may be, but is not limited to, a microprocessor or a circuit card including hardware for processing computer

instructions. Additional structure for an electronic system, such as a computer system 502 would be readily apparent to those skilled in the art.

Yet another embodiment of the present invention is depicted in FIG. 16 of the drawings. Interposer substrate 610 is comprised of a single conductive layer sandwiched between two dielectric members 636. The conductive layer may be patterned into a plurality of conductive traces 630 including conductive pads 632, which may comprise trace ends, exposed through a plurality of recesses 620 formed through both dielectric members 636. It is contemplated that the conductive layer may be provided as a sheet or film of copper adhered to one dielectric member 636 and conductive traces 630 formed by etching the copper, subsequent to which a second dielectric member is superimposed on the conductive traces, although the invention is not so limited. Recesses 620 may be preformed in one or both dielectric members 636, or formed in one or both dielectric member 636 after the laminated structure of interposer substrate 610 is formed

As also depicted in FIG. 16, a first semiconductor die 660 and a second semiconductor die 760 are respectively connected to conductive traces 630 by conductive bumps 666 and 676, which extend into recesses 620 to contact conductive pads 632. A conductive paste (not shown) may be disposed in recesses 620 or conductive bumps 666 and 676 dipped therein to enhance the connections between conductive bumps 666, 676 and the conductive pads 632 at the bottoms of recesses 62, as previously discussed with respect to other embodiments. Furthermore, semiconductor dice 660 and 670 may be respectively adhered to exterior surfaces of interposer substrate 610 by adhesive elements 652 and 654, again as previously discussed If desired, a dielectric encapsulant material 682, which may be any previously disclosed herein or otherwise suitable for use, may be introduced between each semiconductor die 660, 670 and its adjacent dielectric member 636 to fill the standoff area therebetween as well as any portions of recesses 620 unfilled by conductive bumps 666 and 676. Further, and if desired, semiconductor dice 660 and 670 may be encapsulated about their peripheries and back sides as shown in broken lines to provide a fully encapsulated package 680. As with other embodiments, enlarged conductive bumps may be formed at appropriate locations on one or both sides of interposer substrate 610 through other

recesses in a dielectric member 636 for connection of the semiconductor device package 680 to other packages or to a carrier substrate (not shown).

In lieu of stacking semiconductor packages 680, however, it is contemplated that either approach to the present invention, comprising a flexible interposer substrate using dual conductive layers having a dielectric member interposed therebetween or a single conductive layer interposed between two dielectric members, may be employed to implement a folded interposer substrate package according to the present invention. An exemplary embodiments of a dual-sided folded interposer substrate packages is disclosed in FIG. 17.

FIG. 17 depicts an interposer substrate 710, which may comprise either a dual conductive layer or single conductive layer interposer substrate according to the present invention, folded over upon itself in two portions 710a and 710b, with back-to-back semiconductor dice 760a and 760b therebetween and a third semiconductor die 760c on portion 710a. All three semiconductor dice 760a-c are flip-chip configured with conductive bumps 766 projecting therefrom into recesses (not shown for clarity) in interposer substrate 710 as discussed with respect to previous embodiments. The standoff areas between each semiconductor die 760 and its adjacent portion of interposer substrate 710 may be filled with an encapsulant material 782, as may the peripheries and back sides of the semiconductor dice 760a-c, and the bight area 790 of the fold between interposer substrate portions 710a and 710b Enlarged conductive elements 792 may be employed to connect the interposer substrate 710 to higher-level packaging, such as a carrier substrate in the form of a printed circuit board Exemplary folded interposer substrate package 780a results. Folded interposer substrate package 780a may be formed by respectively connecting semiconductor dice 760a and 760b to the same side of interposer substrate 710 in unfolded or planar form over then-laterally-adjacent portions 710a and 710b, then folding the substrate 710 and adhering semiconductor dice 760a and 760b back-to-back, after which semiconductor die 760c is connected to interposer substrate portion 710b and encapsulation and bumping with enlarged conductive elements may be completed. Semiconductor dice 760a-c may be of the same type or origin or of different types or origin, as desired, and perform the same or different functions

While the present invention has been disclosed in terms of certain exemplary embodiments and variations thereof, those of ordinary skill in the art will recognize and appreciate that the invention is not so limited Additions, deletions and modifications to the disclosed embodiments may be effected without departing from the scope of the invention as claimed herein. Similarly, features from on embodiment may be combined with those of another while remaining within the scope of the invention. For example, features of the fourth embodiment may be combined with the second embodiment, wherein the first surface of the interposer may include four recess patterns and the second surface of the interposer substrate may include two recess patterns. Further, any number of recess patterns may be provided on the first surface and/or the second surface of the interposer substrate for optional semiconductor die attachment thereto.

CLAIMS

What is claimed is.

1. An article for use in mounting at least one flip chip semiconductor die having a plurality of conductive bumps projecting therefrom, comprising:

an interposer substrate having a first surface and a second surface and comprising a dielectric member having at least one conductive layer thereon comprising a plurality of conductive traces, said interposer substrate including a plurality of recesses formed in at least one of said first and second surfaces, each recess exposing at a bottom thereof at least a portion of a conductive trace, said plurality of recesses arranged in at least a first recess pattern and a second, different recess pattern.

2 The article of claim 1, wherein said first recess pattern is formed in said first surface of said interposer substrate and said second recess pattern is formed in said second surface of said interposer substrate.

3. The article of claim 1, wherein each of said plurality of recesses is sized and configured to substantially receive a conductive bump of the at least one flip chip semiconductor die so that an active surface of the at least one semiconductor die lies immediately adjacent at least one of said first surface and said second surface of said interposer substrate.

4. The article of claim 1, wherein recesses of said plurality arranged in said first recess pattern are each located closer to a periphery of said interposer substrate than recesses of said plurality arranged in said second recess pattern.

5. The article of claim 1, wherein said at least said first recess pattern and said second recess pattern are formed in said first surface of said interposer substrate

6. The article of claim 5, wherein said at least said first recess pattern and said second recess pattern share a common first die attach site

7 The article of claim 1, wherein each of said recesses of said plurality arranged in said first recess pattern exposes at least a portion of a conductive trace exposed by one of said recesses of said plurality arranged in said second recess pattern and each recess of said first pattern is more peripherally located on said interposer substrate than a recess arranged in said second recess pattern exposing at least a portion of the same trace.

8. The article of claim 5, wherein said second surface of said interposer substrate includes recesses arranged in at least a third recess pattern.

9. The article of claim 8, wherein recesses of said at least said third recess pattern are arranged differently then said recesses of said first recess pattern and said second recess pattern.

10. The article of claim 8, wherein said recesses of said at least said third recess pattern are staggered with respect to said recesses of said first recess pattern and said second recess pattern

11. The article of claim 5, wherein said second surface of said interposer substrate includes a third recess pattern and a fourth recess pattern, and wherein said at least said third recess pattern and said fourth recess pattern share a common second die attach site.

12. The article of claim 11, wherein said recesses of said third recess pattern are spaced and configured differently than said recesses of said fourth recess pattern

13. The article of claim 11, wherein said recesses of each of said third recess pattern and said fourth recess pattern are spaced and configured differently than said recesses of each of said first recess pattern and said second recesses pattern

14. The article of claim 11, wherein said recesses of said third recess pattern and said fourth recess pattern are staggered with respect to said recesses of said first recess pattern and said second recess pattern

15. The article of claim 5, wherein said first surface of said interposer substrate includes at least a third recess pattern arranged differently than said recesses of said first recess pattern and said second recess pattern

16. The article of claim 15, wherein said recesses of said at least said third recess patten are staggered with respect to said recesses of said first recess pattern and said second recess pattern.

17. The article of claim 5, wherein said plurality of recesses in said first surface of said interposer substrate includes a third recess pattern and a fourth recess pattern.

18. The article of claim 17, wherein said recesses of each of said third recess pattern and said fourth recess pattern are arranged differently than said recesses of each of said first recess pattern and said second recess pattern.

19. The article of claim 17, wherein said recesses of each of said third recess pattern and said fourth recess pattern are staggered with respect to said recesses of each of said first recess pattern and said second recess pattern.

20. The article of claim 17, wherein said recesses of said third recess pattern are substantially more peripherally located with respect to recesses of said fourth recess pattern.

21 The article of claim 1, further comprising a die attach site having an adhesive element positioned on at least one of said first surface and said second surface of said interposer substrate

22. The article of claim 1, further comprising test pads proximate a periphery of said interposer substrate, each of said test pads conductively connected to a said conductive trace and exposed on at least one of said first surface and said second surface of the interposer substrate.

23. The article of claim 1, wherein said interposer substrate comprises a flexible tape.

24. The article of claim 1, wherein said interposer substrate comprises at least one of a polymer material, BT, FR4 laminate, FR5 laminate and ceramic.

25. A semiconductor assembly comprising:

at least one semiconductor die having an active surface and a back surface, said active surface having conductive bumps thereon; and

an interposer substrate having a first surface and a second surface and comprising a dielectric member having at least one conductive layer thereon including a plurality of conductive traces, said interposer substrate including a plurality of recesses formed in at least one of said first and second surfaces, each recess exposing at a bottom thereof at least a portion of one of said conductive traces, said plurality of recesses arranged in at least a first recess pattern and a second, different recess pattern on said interposer substrate, said plurality of conductive bumps of said at least one semiconductor die being received within at least one of said at least a first recess pattern and a second recess pattern.

26. The assembly of claim 25, wherein said conductive bumps on said at least one semiconductor die are disposed in said at least one of said first recess pattern and said second recess pattern so that said active surface of said at least one semiconductor die lies adjacent said at least one of said first surface and said second surface of said interposer substrate.

27. The assembly of claim 25, wherein said first surface of said interposer substrate includes said at least said first recess pattern and said second recess pattern and said plurality of conductive bumps of said at least one semiconductor die are arranged to match at least one of said at least a first recess pattern and a second recess pattern.

28. The assembly of claim 27, wherein said second surface of said interposer substrate includes at least a third recess pattern and a fourth recess pattern and said at least one semiconductor die comprises a second semiconductor die with a plurality of conductive bumps arranged to match at least one of said third recess pattern and said fourth recess pattern

29. The assembly of claim 25, wherein said plurality of recesses of said first recess pattern are closer to a periphery of said interposer substrate than said plurality of recesses of said second recess pattern.

30. The assembly of claim 25, wherein each recess of said first recess pattern and exposes at least a portion of a conductive trace also exposed by a recess of said second recess pattern and is relatively more outwardly located on said interposer substrate.

31. The assembly of claim 25, wherein said recesses of said at least a first recess pattern and a second recess pattern are staggered with respect to each other.

32. The assembly of claim 28, wherein said recesses of said at least a first recess pattern and a second recess pattern are staggered with respect to said recesses of said at least a third recess pattern and a fourth recess pattern.

33. The assembly of claim 25, further comprising a die attach site having at least one adhesive element thereon positioned on at least one of said first surface and said second surface of said interposer substrate and said at least one semiconductor die is adhered to the die attach site by said at least one adhesive element.

34. The assembly of claim 25, further comprising test pads proximate a periphery of said interposer substrate, each of said testing pads being conductively connected to a said conductive trace and exposed on at least one of said first surface and said second surface of said interposer substrate

35. The assembly of claim 25, wherein said interposer substrate comprises a flexible tape.

36. The assembly of claim 25, wherein said interposer substrate comprises at least one of a polymer material, BT, FR4 laminate, FR5 laminate and ceramic.

37. The assembly of claim 25, further comprising dielectric filler material proximate said conductive bumps received in said recesses.

38. The assembly of claim 25, further comprising a circuit board conductively connected to conductive traces of said interposer substrate by conductive elements disposed therebetween

39. The assembly of claim 38, further comprising an encapsulation material at least partially encapsulating said at least one semiconductor die.

40. The assembly of claim 27, wherein said at least a first recess pattern and a second recess pattern share a common first die attach site.

41. The assembly of claim 28, wherein said at least a third recess pattern and a fourth recess pattern share a common second die attach site.

42 A method of assembling a semiconductor assembly, the method comprising:

providing at least one semiconductor die having an active surface and a back surface, said active surface having a plurality of conductive bumps projecting therefrom;

providing an interposer substrate having a first surface and a second surface and comprising a dielectric member having at least one conductive layer thereon including a plurality of conductive traces, said interposer substrate having a plurality of recesses formed in at least one of said first and second surfaces and exposing at a bottom thereof at least a portion of one of said conductive traces, said recesses arranged in at least a first recess pattern and a second, different recess pattern, and

disposing said plurality of conductive bumps of said at least one semiconductor die in at least one of said at least a first recess pattern and a second recess pattern so that said active surface lies adjacent at least one of said first surface and said second surface of said interposer substrate.

43. The method of claim 42, wherein said providing said interposer substrate comprises providing said interposer substrate with said first surface including both said first recess pattern and said second recess pattern.

44. The method of claim 43, wherein said disposing further comprises matching a configuration of conductive bumps of said at least one semiconductor die to one of said at least a first recess pattern and a second recess pattern.

45. The method of claim 44, wherein said disposing comprises mounting said at least one semiconductor die over said at least one of said at least a first recess pattern and a second recess pattern on a first die attach site commonly shared by said at least a first recess pattern and a second recess pattern

46. The method of claim 43, wherein said providing said interposer substrate comprises providing said interposer substrate with said second surface including at least a third recess pattern and a fourth recess pattern.

47. The method of claim 46, wherein said disposing comprises matching a configuration of conductive bumps of said at least one semiconductor die to at least one of said at least a third recess pattern and a fourth recess pattern.

48 The method of claim 47, said disposing comprises mounting said at least one semiconductor die over said at least one of said at least a first third pattern and a fourth recess pattern on a second die attach site commonly shared by said at least a third recess pattern and a fourth recess pattern.

49. The method of claim 43, wherein said providing said interposer substrate comprises providing said interposer substrate with said first surface including at least a third recess pattern and a fourth recess pattern.

50 The method of claim 49, wherein said disposing comprises matching a configuration of conductive bumps of said at least one semiconductor die to said at least one of a first recess pattern, a second recess pattern, a third recess pattern and a fourth recess pattern.

51. The method of claim 50, wherein said disposing comprises mounting said at least one semiconductor die to over said at least one of said first recess pattern, said second recess pattern, said third recess pattern and said fourth recess pattern on a first die attach site commonly shared by each of said first recess pattern, said second recess pattern, said third recess pattern and said fourth recess pattern.

52. The method of claim 42, wherein said disposing comprises attaching said active surface of said at least one semiconductor die to an adhesive element on a die attach site on at least one of said first surface and said second surface of said interposer substrate.

53 The method of claim 42, further comprising electrically testing at least interconnections between said at least one semiconductor die and conductive traces of said interposer substrate by positioning a testing member on test pads conductively

connected to said conductive traces and exposed on at least one of said first surface and said second surface proximate a periphery of said interposer substrate.

54 The method of claim 42, further comprising dispensing encapsulation material proximate conductive bumps of said conductive bumped configuration in a space defined between said active surface of said at least one semiconductor die and said at least one of said first surface and said second surface of said interposer substrate

55. The method of claim 42, further comprising at least partially encapsulating said at least one semiconductor die and said interposer substrate with encapsulation material.

56. The method of claim 42, further comprising mounting said second surface of said interposer substrate to another substrate with conductive elements disposed therebetween.

57. A method of fabricating a substrate for mounting at least one semiconductor die in a flip chip arrangement thereto, the method comprising:

providing an interposer substrate having a first surface and a second surface and a dielectric member having at least one conductive layer thereon including a plurality of conductive traces;

forming a plurality of recesses in at least one of said first surface and said second surface of said interposer substrate arranged in a first recess pattern and a second, different recess pattern to expose at least portions of said conductive traces at recess bottoms and to a depth into said interposer substrate sufficient to substantially receive therein conductive bumps on an active surface of the at least one semiconductor die.

58. The method of claim 57, wherein said forming comprises sizing said recesses so that the conductive bumps on the at least one semiconductor die are receivable therein such that the active surface of the at least one semiconductor die lies adjacent said at least one of said first surface and said second surface of said interposer substrate

59. The method of claim 57, wherein said forming comprises forming said at least said first recess pattern and said second recess pattern in said first surface of said interposer substrate so that each of said first recess pattern and said second recess pattern share a common first die attach site for mounting the at least one semiconductor die thereto.

60. The method of claim 59, wherein said configuring comprises forming said recesses of said first and second recess patterns so that each recess of said first recess pattern exposes at least a portion of a conductive trace exposed by a recess of said second recess pattern and placing each recess of said first recess pattern relatively outwardly with respect to said recess of said second recess pattern exposing at least a portion of the same conductive trace.

61 The method of claim 59, wherein said forming comprises forming a third recess pattern and a fourth recess pattern in said second surface of said interposer substrate so that each of said third recess pattern and said fourth recess pattern share a common second die attach site for mounting said at least one semiconductor die thereto

62. The method of claim 61, wherein said configuring comprises forming said recesses of said third and fourth recess patterns so that each recess of said third recess pattern exposes at least a portion of a conductive trace exposed by a recess of said fourth recess pattern and placing each recess of said third recess pattern relatively outwardly with respect to said recess of said fourth recess pattern exposing at least a portion of the same conductive trace

63. The method of claim 61, wherein said configuring comprises staggering said recesses of said third recess pattern and said fourth recess pattern with respect to said recesses of said first recess pattern and said second recess pattern

64. The method of claim 59, wherein said forming comprises forming at least a third recess pattern in said first surface of said interposer substrate so that each of said first recess pattern, said second recess pattern and said third recess pattern share said common first die attach site for mounting said at least one semiconductor die thereto

65. The method of claim 59, wherein said forming comprises forming a third recess pattern and a fourth recess pattern in said first surface of said interposer substrate so that each of said first recess pattern, said second recess pattern, said third recess pattern and said fourth recess pattern share said common first die attach site for mounting said at least one semiconductor die thereto.

66. The method of claim 57, further comprising forming an adhesive element on a die attach site on said at least one of said first surface and said second surface of said interposer substrate.

67 The method of claim 57, further comprising forming test pads proximate a periphery of said interposer substrate and exposed on said at least one of said first surface and said second surface of said interposer substrate so that each test pad is in communication with one of said conductive traces

68. An electronic system comprising:

a processor device coupled to an input device and an output device; and

a semiconductor assembly coupled to at least one of said processor device, said input device and said output device, said semiconductor assembly comprising.

at least one semiconductor die having an active surface and a back surface, said active surface having conductive bumps thereon, and

an interposer substrate having a first surface and a second surface and comprising a dielectric member having at least one conductive layer thereon including a plurality of conductive traces, said interposer substrate including a plurality of recesses formed in at least one of said first and second surfaces, each recess exposing at a bottom thereof at least a portion of one of said conductive traces, said plurality of recesses

arranged in at least a first recess pattern and a second, different recess pattern on said interposer substrate, said plurality of conductive bumps of said at least one semiconductor die being received within at least one of said at least a first recess pattern and a second recess pattern

69. The system of claim 68, wherein said plurality of conductive bumps on said at least one semiconductor die are disposed in said at least one of said first recess pattern and said second recess pattern so that said active surface of said at least one semiconductor die lies adjacent said at least one of said first surface and said second surface of said interposer substrate.

70 The system of claim 68, wherein said first surface of said interposer substrate includes said at least said first recess pattern and said second recess pattern and said plurality of conductive bumps of said at least one semiconductor die are arranged to match at least one of said at least a first recess pattern and a second recess pattern

71. The system of claim 70, wherein said second surface of said interposer substrate includes at least a third recess pattern and a fourth recess pattern and said plurality of conductive bumps of said at least one semiconductor die are arranged to match at least one of said at least a third recess pattern and a fourth recess pattern.

72. The system of claim 68, further comprising a die attach site having an adhesive element thereon positioned on at least one of said first surface and said second surface of said interposer substrate for mounting said at least one semiconductor die thereto.

73 The system of claim 68, further comprising test pads proximate a periphery of said interposer substrate, each of said testing pads in communication with one of said conductive traces and exposed on at least one of said first surface and said second surface of said interposer substrate

74. The system of claim 68, wherein said interposer substrate comprises a flexible tape.

75. The system of claim 68, wherein said interposer substrate comprises at least one of a polymer material, BT, FR4 laminate, FR5 laminate and ceramic.

76. The system of claim 68, further comprising dielectric filler material disposed proximate said plurality of conductive bumps disposed in said plurality of recesses.

77. The system of claim 68, further comprising an encapsulation material at least partially encapsulating said at least one semiconductor die and said interposer substrate.

78. The system of claim 70, wherein said at least said first recess pattern and said second recess pattern share a common first die attach site.

79. The system of claim 71, wherein said at least said third recess pattern and said fourth recess pattern share a common second die attach site.

80. An interposer substrate, comprising:

a conductive layer comprising a plurality of conductive traces,

first and second dielectric members respectively disposed over opposing sides of the conductive layer; and

at least one recess extending from an exterior surface of the first dielectric member to expose a portion of a conductive trace of the plurality, and

at least one recess extending from an exterior surface of the second dielectric member to expose a portion of a conductive trace of the plurality.

81. An interposer substrate, comprising:

a dielectric member;

a first plurality of conductive traces on one side of the dielectric member,

a second plurality of conductive traces on an opposing side of the dielectric member,

at least one recess extending from a surface of the dielectric member on the one side thereof to expose a portion of a conductive trace on the opposing side of the dielectric member; and

at least one recess extending from a surface of the dielectric member on the opposing side thereof to expose a portion of a conductive trace on the first side of the dielectric member.

82. A semiconductor device assembly, comprising:

a flexible interposer substrate including at least one conductive layer comprising a plurality of conductive traces and at least one dielectric member, the at least one dielectric member having a plurality of recesses extending from an exterior surface of each of two opposing sides of the interposer substrate through the at least one dielectric member to expose portions of conductive traces of the plurality;

the plurality of recesses being arranged in at least three patterns, at least two of the at least three patterns located on one side of the interposer substrate and at least one of the at least three patterns being located on an opposing side of the interposer substrate in substantial superimposition to at least one of the at least two patterns; and

at least three semiconductor dice of flip-chip configuration having a plurality of conductive elements projecting therefrom, wherein each semiconductor die is operably coupled to at least some of the plurality of conductive traces by conductive elements received in a pattern of recesses;

the interposer substrate being folded so that at least two of the semiconductor dice operably coupled to conductive traces through patterns of recesses on the one side of the interposer substrate are oriented in substantially superimposed back-to-back relationship between portions of the interposer substrate and at least a third semiconductor die is located in substantial superimposition to the at least two semiconductor dice on the opposing side of the interposer substrate.