FIG. 1

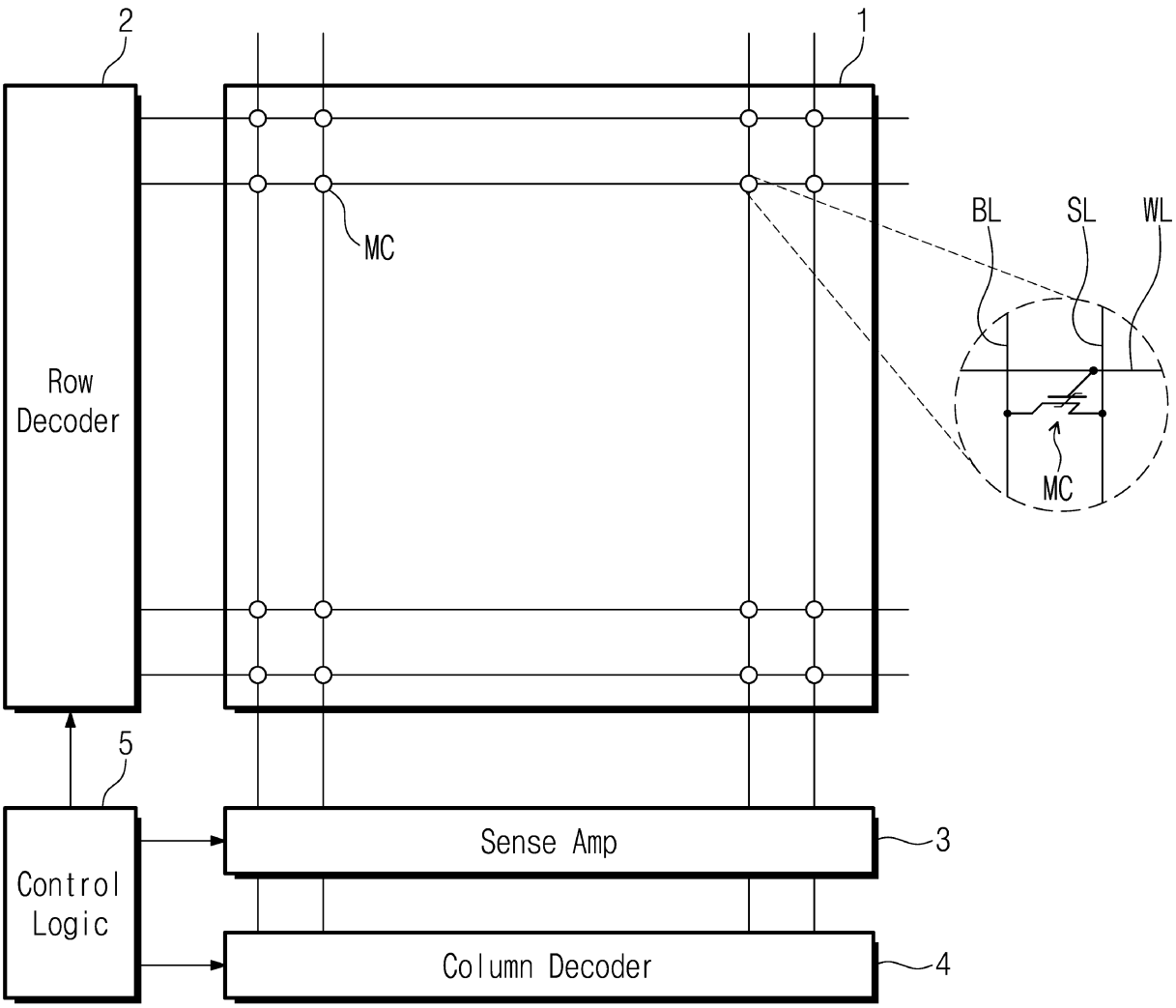

2
1
Row Decoder
MC
BL
SL
WL
MC
5
Control Logic
Sense Amp
3
Column Decoder
4

FIG. 2

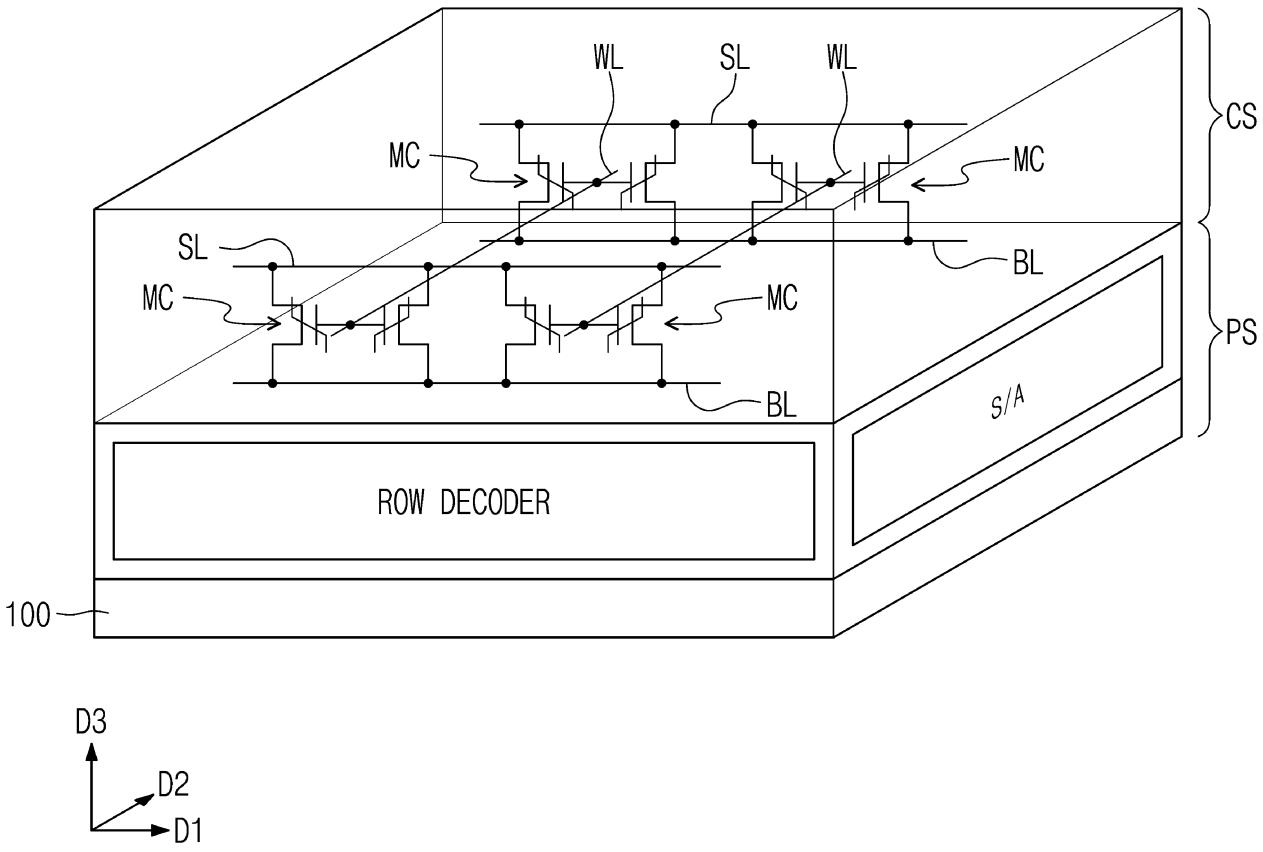


FIG. 3

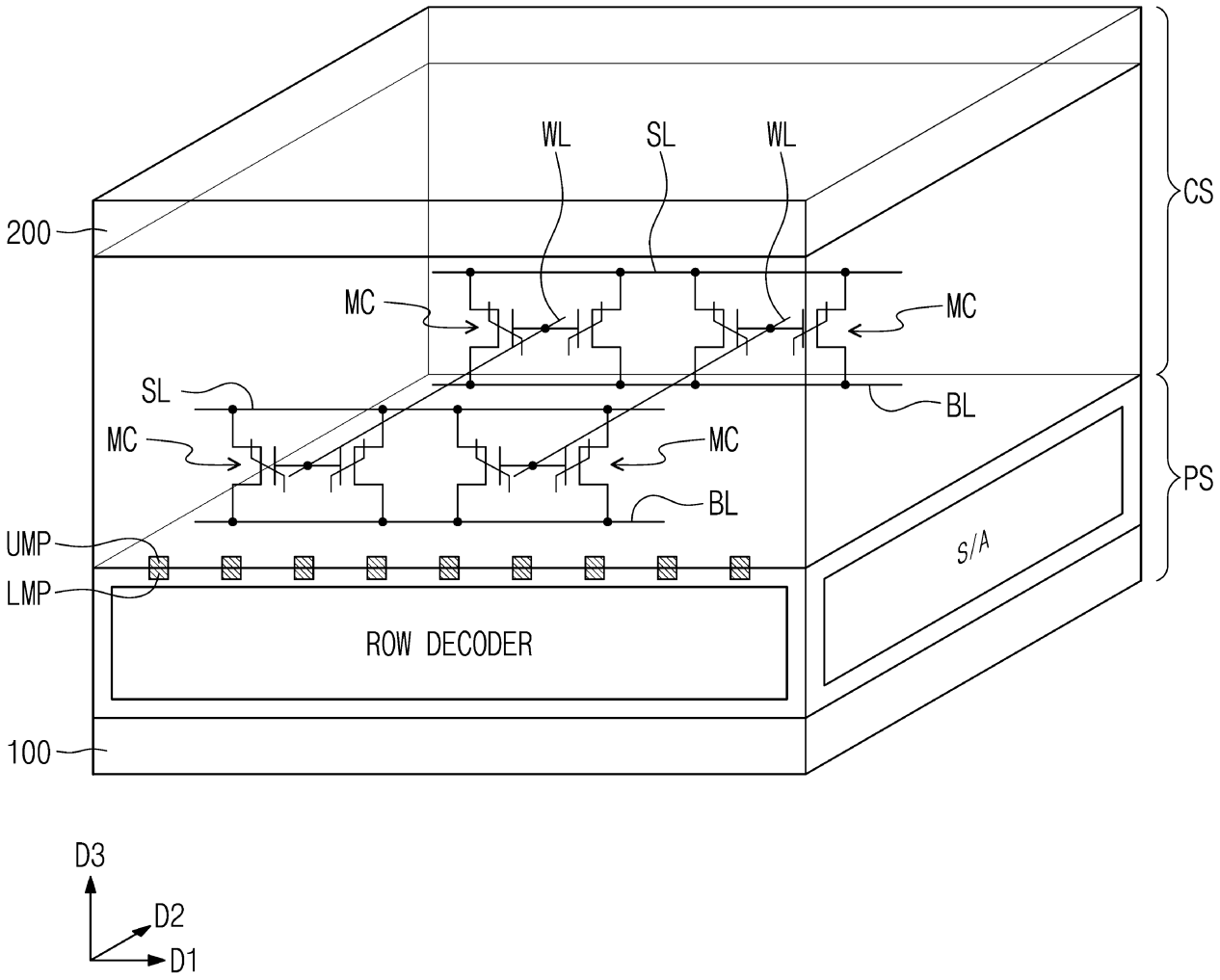

WL
SL
WL
CS
200
MC
MC
SL
BL
MC
MC
PS
BL
UMP
S/A
LMP
ROW DECODER
100
D3
D2
D1

FIG. 4

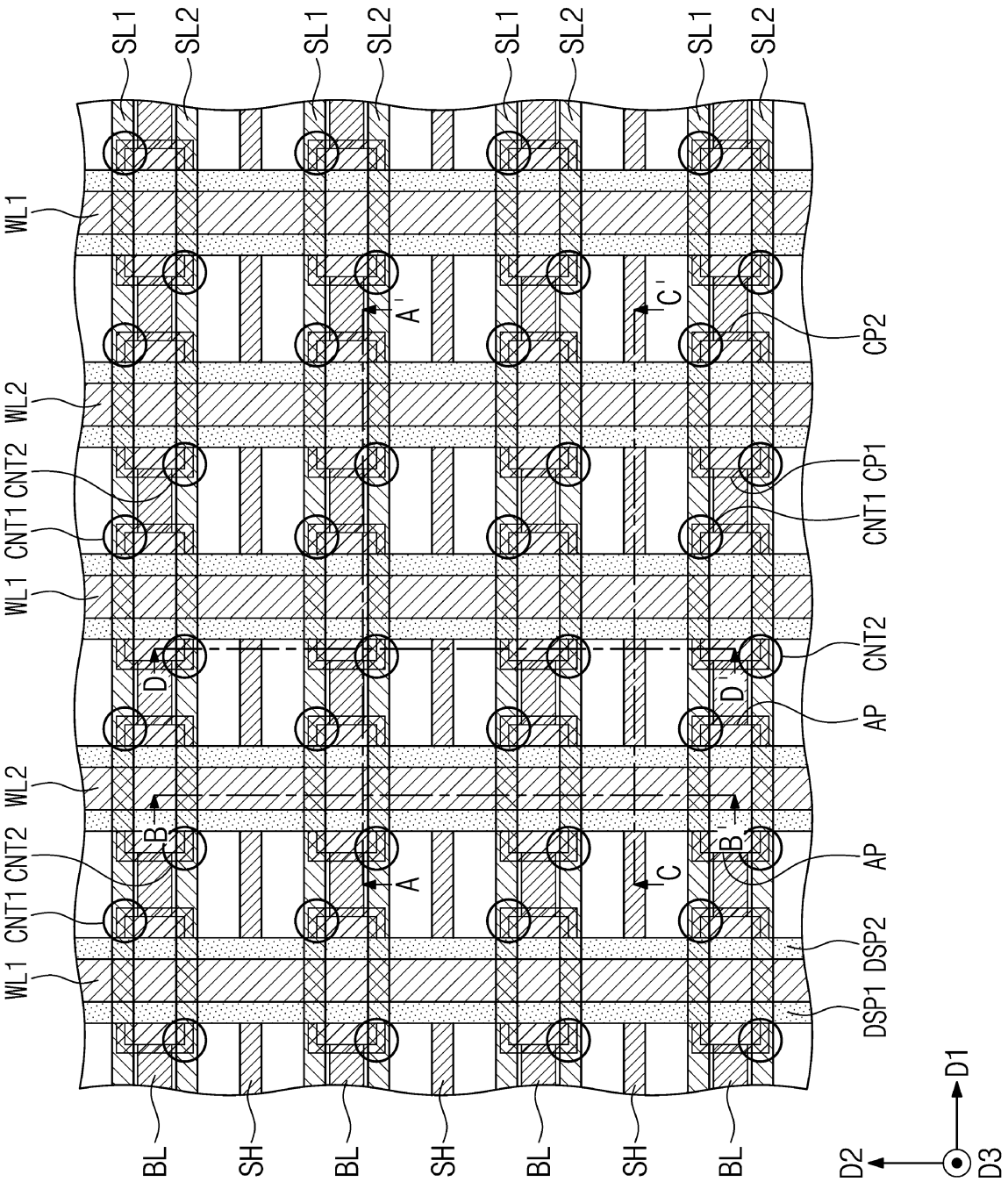

SL1
SL2
WL1
WL2
CNT1
CNT2
CP1
CP2
AP
DSP1
DSP2
BL
SH
A
A'
B
B'
C
C'
D
D'
D1
D2
D3

FIG. 5A

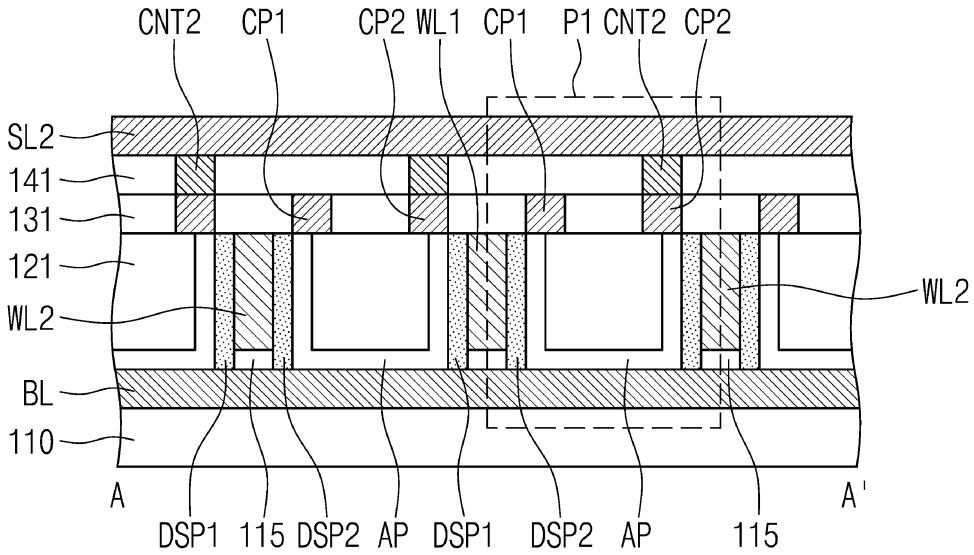

CNT2
CP1
CP2
WL1
CP1
P1
CNT2
CP2
SL2
141
131
121
WL2
WL2
BL
110
A
A'
DSP1
115
DSP2
AP
DSP1
DSP2
AP
115

FIG. 5B

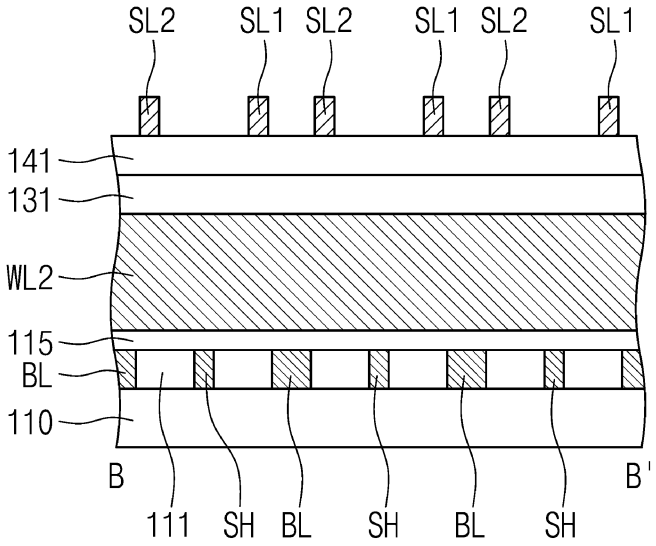

SL2
SL1
SL2
SL1
SL2
SL1
141
131
WL2
115
BL
110
B
B'
111
SH
BL
SH
BL
SH

FIG. 5C

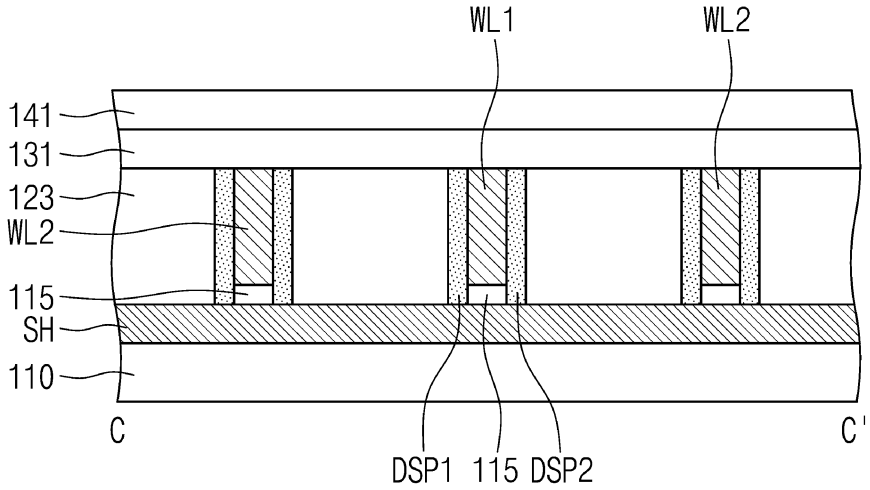

WL1
WL2
141
131
123
WL2
115
SH
110
C
C'
DSP1
115
DSP2

FIG. 5D

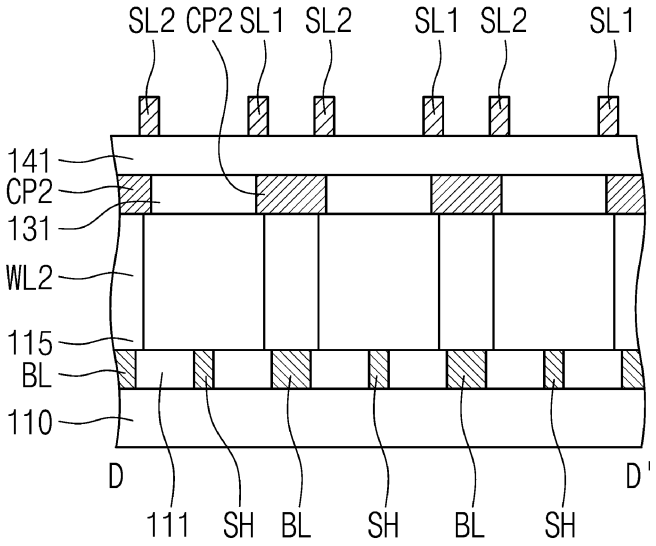

SL2
CP2
SL1
SL2
SL1
SL2
SL1
141
CP2
131
WL2
115
BL
110
D
D'
111
SH
BL
SH
BL
SH

FIG. 6

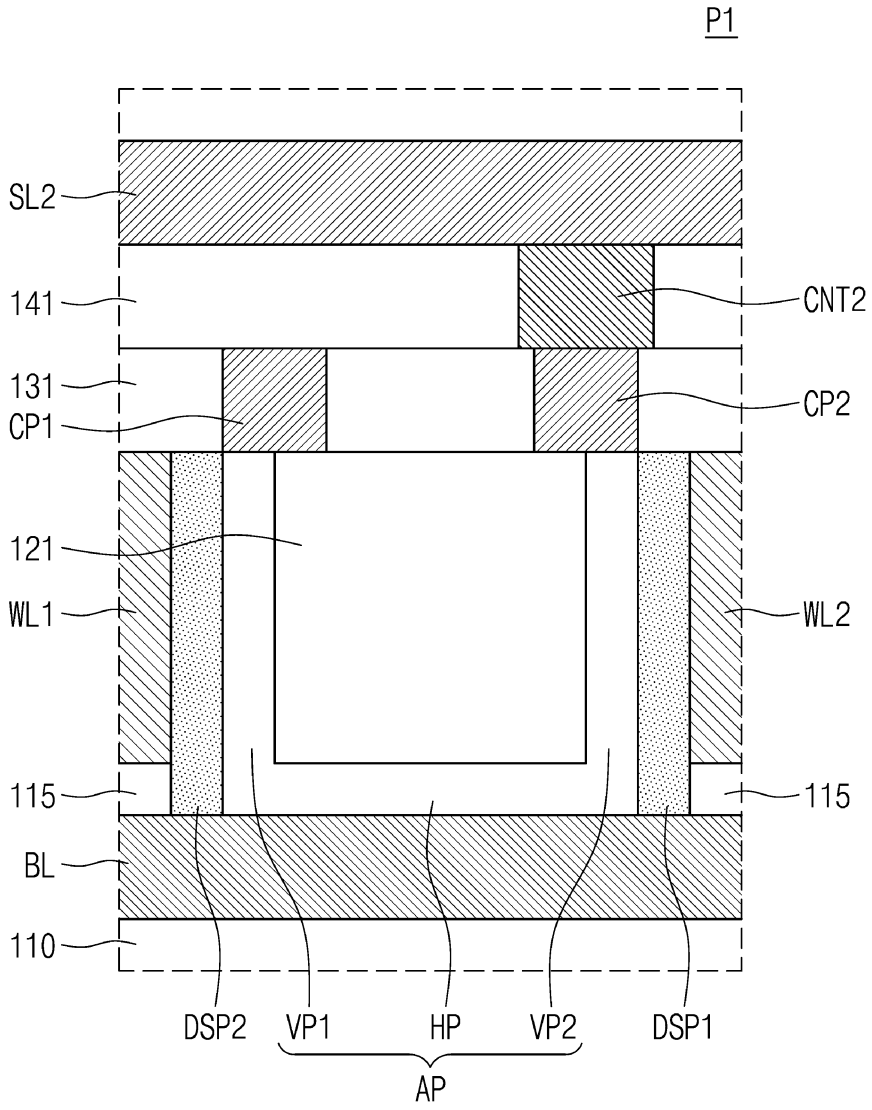

P1
SL2
141
CNT2
131
CP1
CP2
121
WL1
WL2
115
115
BL
110
DSP2
VP1
HP
VP2
DSP1
AP

FIG. 7

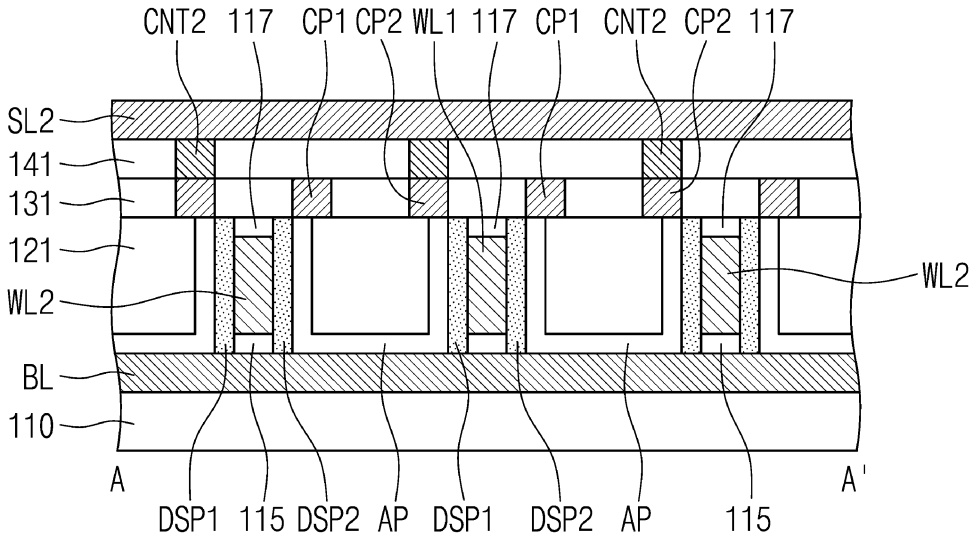

CNT2
117
CP1
CP2
WL1
117
CP1
CNT2
CP2
117
SL2
141
131
121
WL2
WL2
BL
110
A
A'
DSP1
115
DSP2
AP
DSP1
DSP2
AP
115

FIG. 8

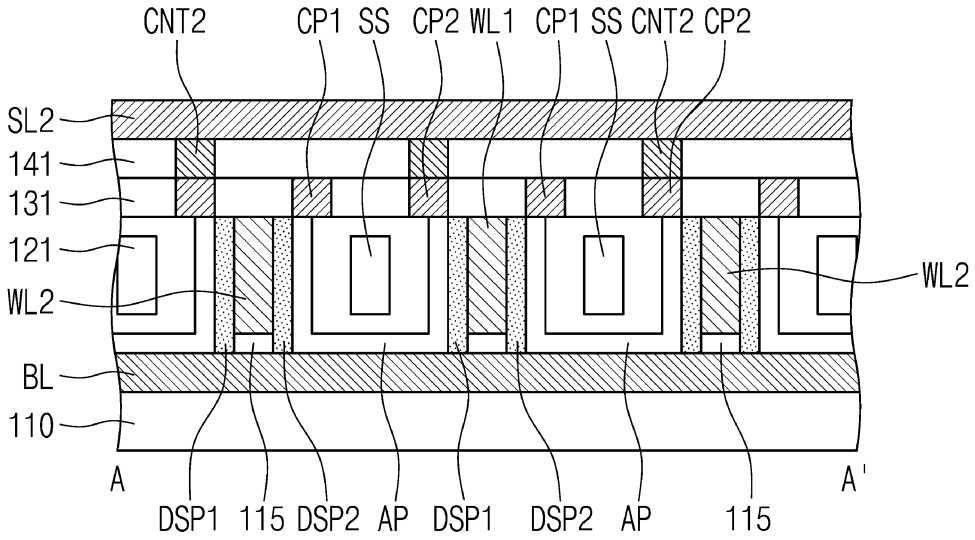

CNT2
CP1
SS
CP2
WL1
CP1
SS
CNT2
CP2
SL2
141
131
121
WL2
WL2
BL
110
A
A'
DSP1
115
DSP2
AP
DSP1
DSP2
AP
115

FIG. 9

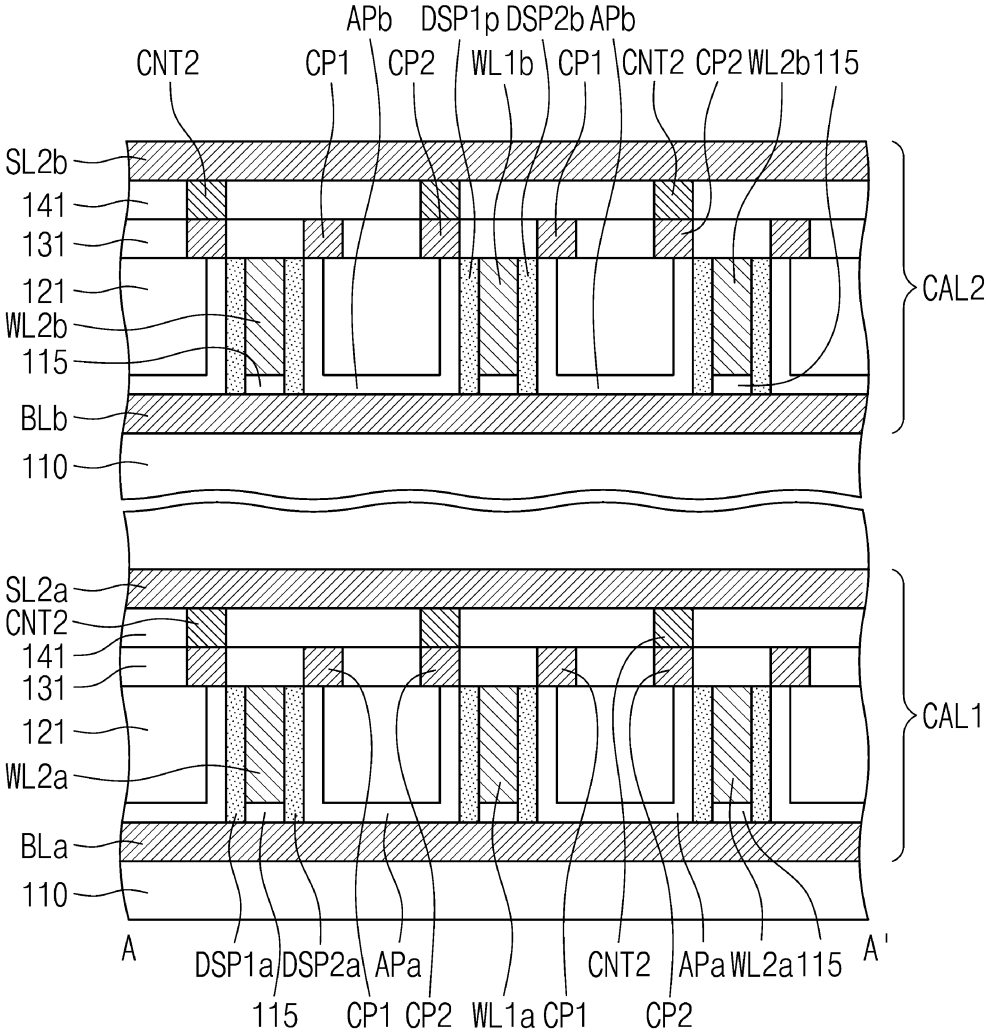

APb
DSP1p
DSP2b
APb
CNT2
CP1
CP2
WL1b
CP1
CNT2
CP2
WL2b
115
SL2b
141
131
121
WL2b
115
BLb
110
CAL2
SL2a
CNT2
141
131
121
WL2a
BLa
110
CAL1
A
DSP1a
DSP2a
APa
CNT2
APa
WL2a
115
A'
115
CP1
CP2
WL1a
CP1
CP2

FIG. 10

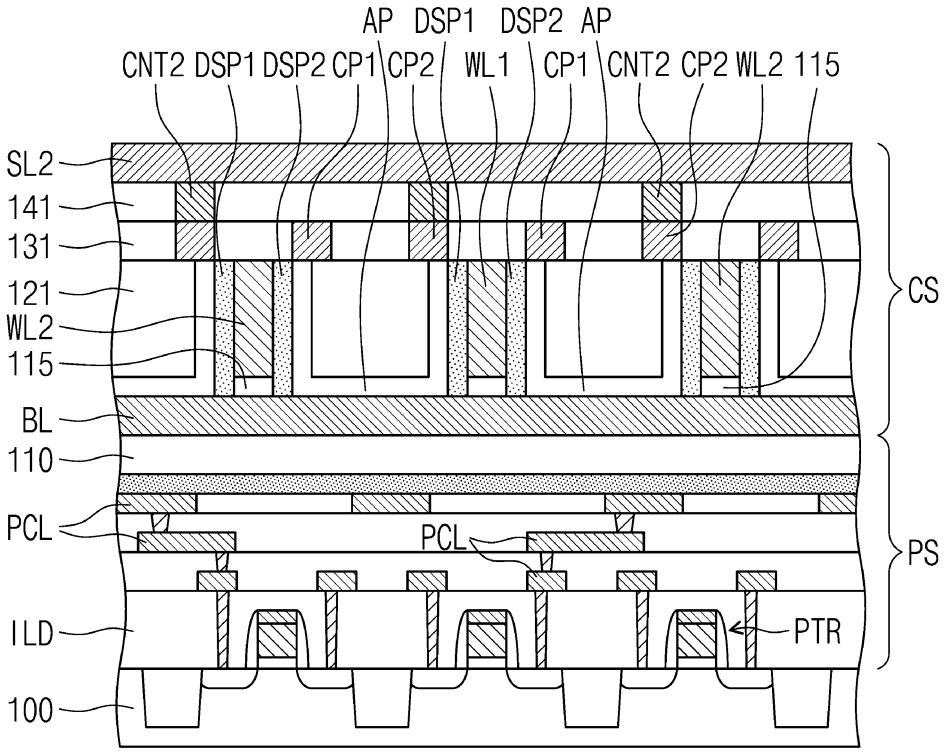

AP
DSP1
DSP2
AP
CNT2
DSP1
DSP2
CP1
CP2
WL1
CP1
CNT2
CP2
WL2
115
SL2
141
131
121
WL2
115
BL
110
PCL
PCL
ILD
100
PTR
CS
PS

FIG. 11

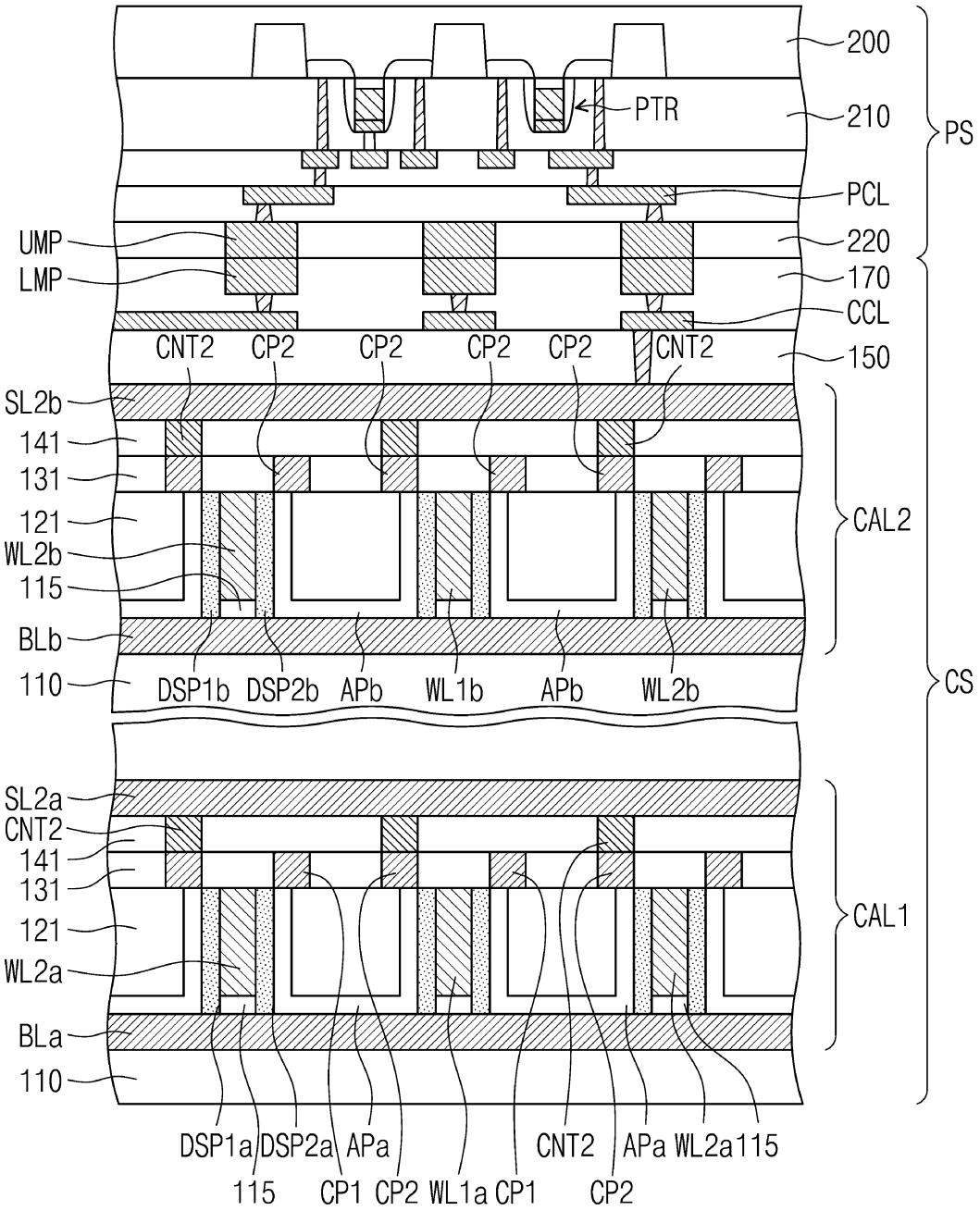

200
PTR
210
PS
PCL
UMP
220
LMP
170
CCL
CNT2
CP2
CP2
CP2
CP2
CNT2
150
SL2b
141
131
121
WL2b
115
CAL2
BLb
110
DSP1b
DSP2b
APb
WL1b
APb
WL2b
CS
SL2a
CNT2
141
131
121
WL2a
CAL1
BLa
110
DSP1a
DSP2a
APa
CNT2
APa
WL2a
115
115
CP1
CP2
WL1a
CP1
CP2

FIG. 12

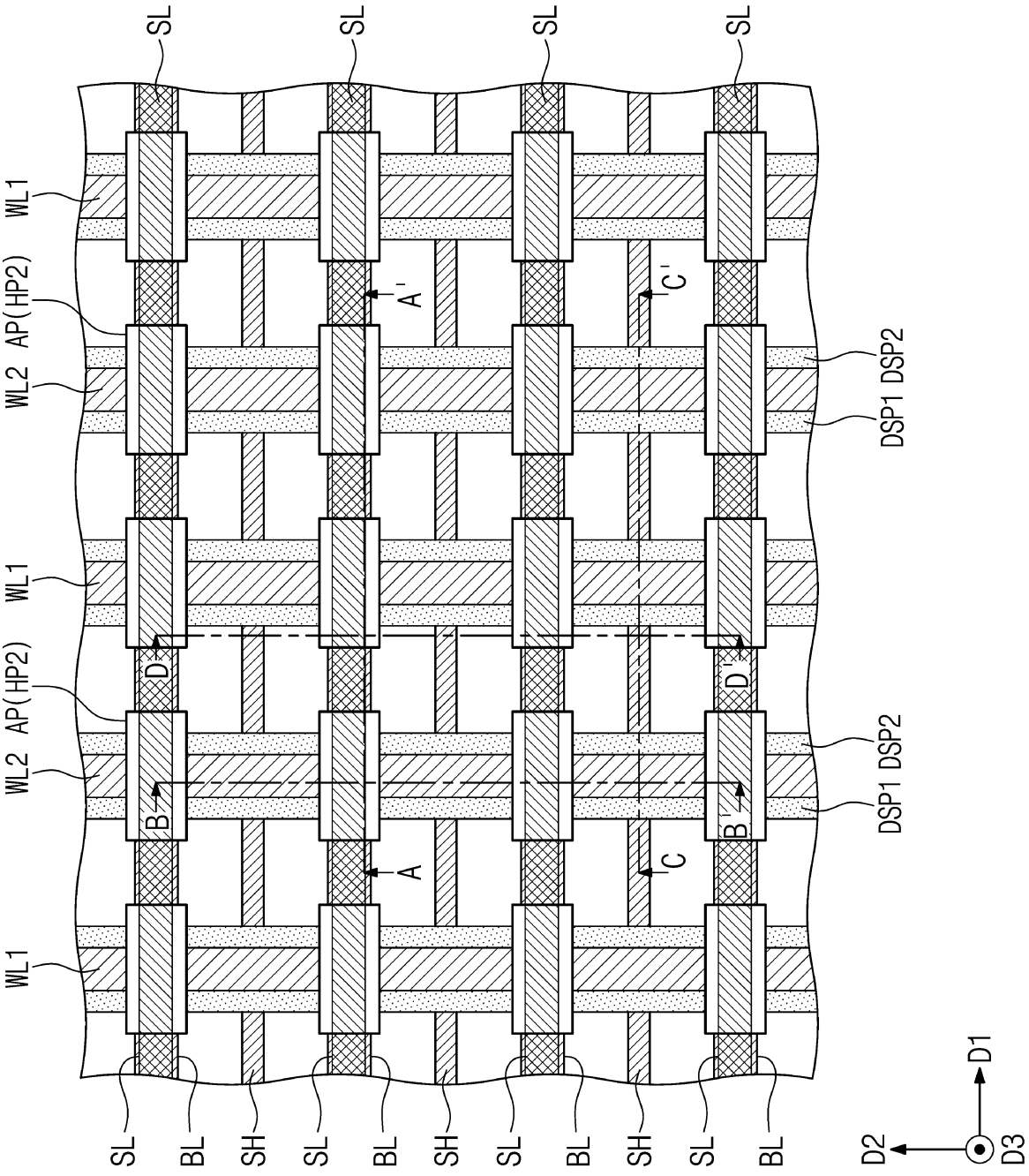


FIG. 13A

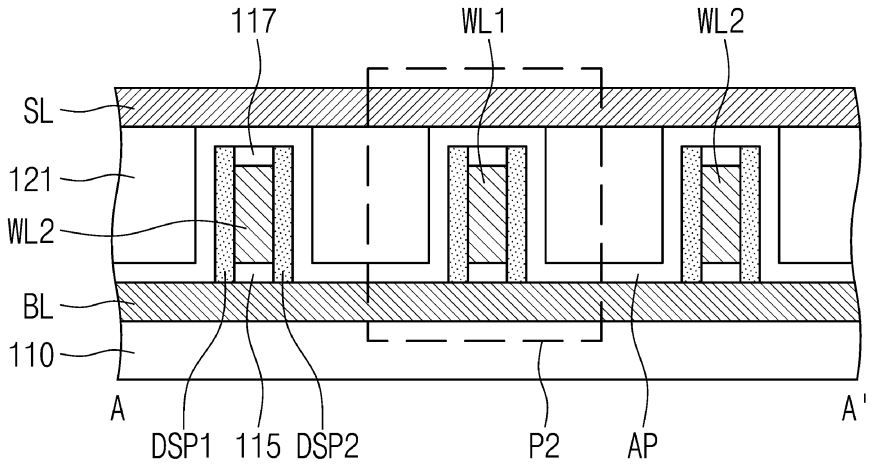


FIG. 13B

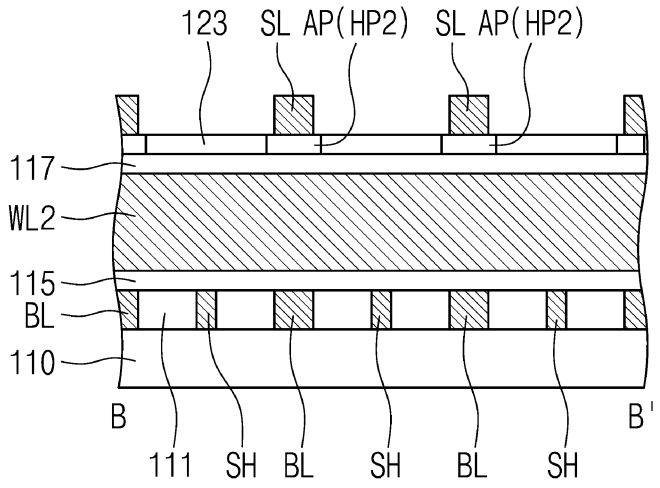


FIG. 14

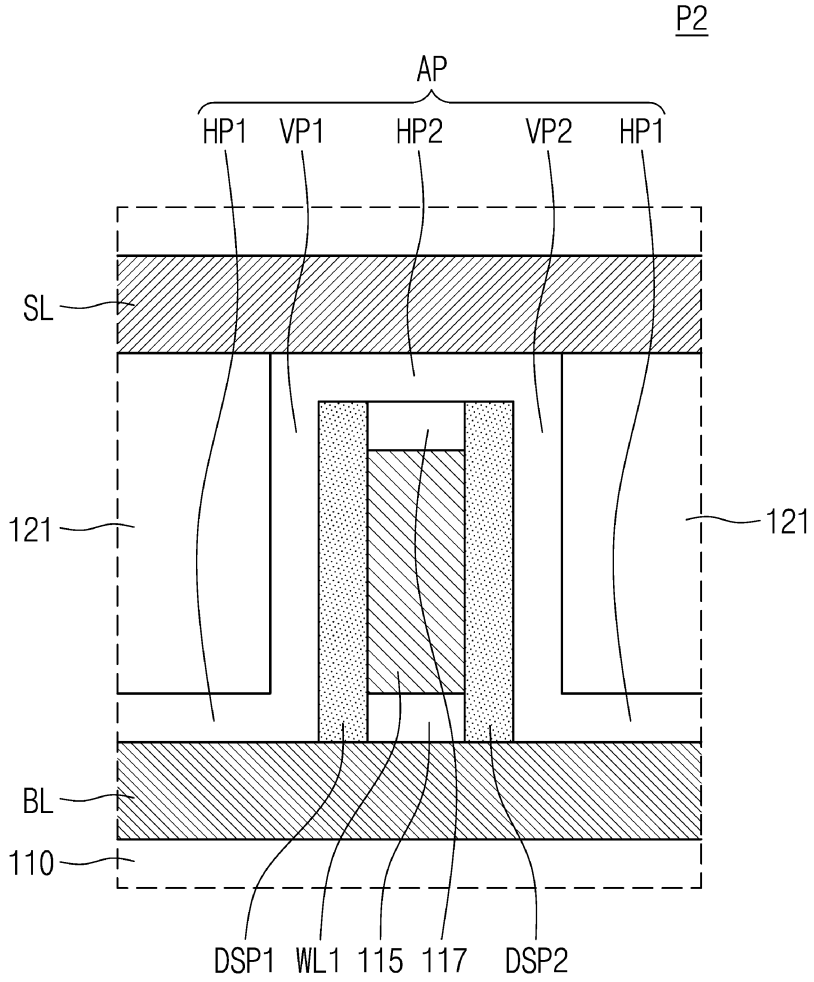

P2
AP
HP1
VP1
HP2
VP2
HP1
SL
121
121
BL
110
DSP1
WL1
115
117
DSP2

FIG. 15

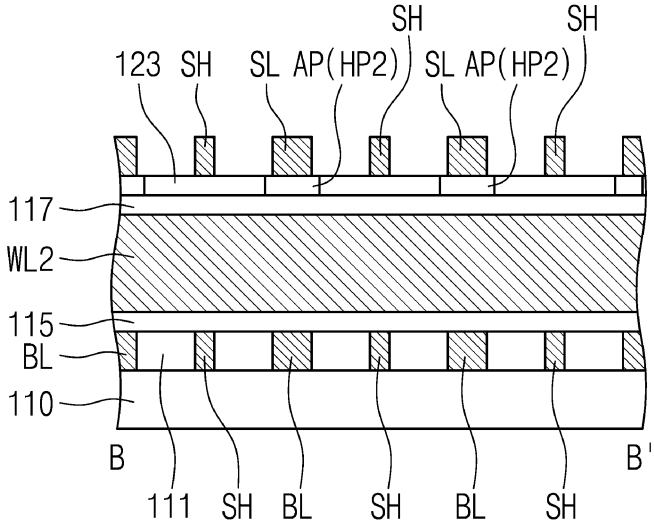

SH
SH
123
SH
SL
AP(HP2)
SL
AP(HP2)
117
WL2
115
BL
110
B
B'
111
SH
BL
SH
BL
SH

FIG. 16A

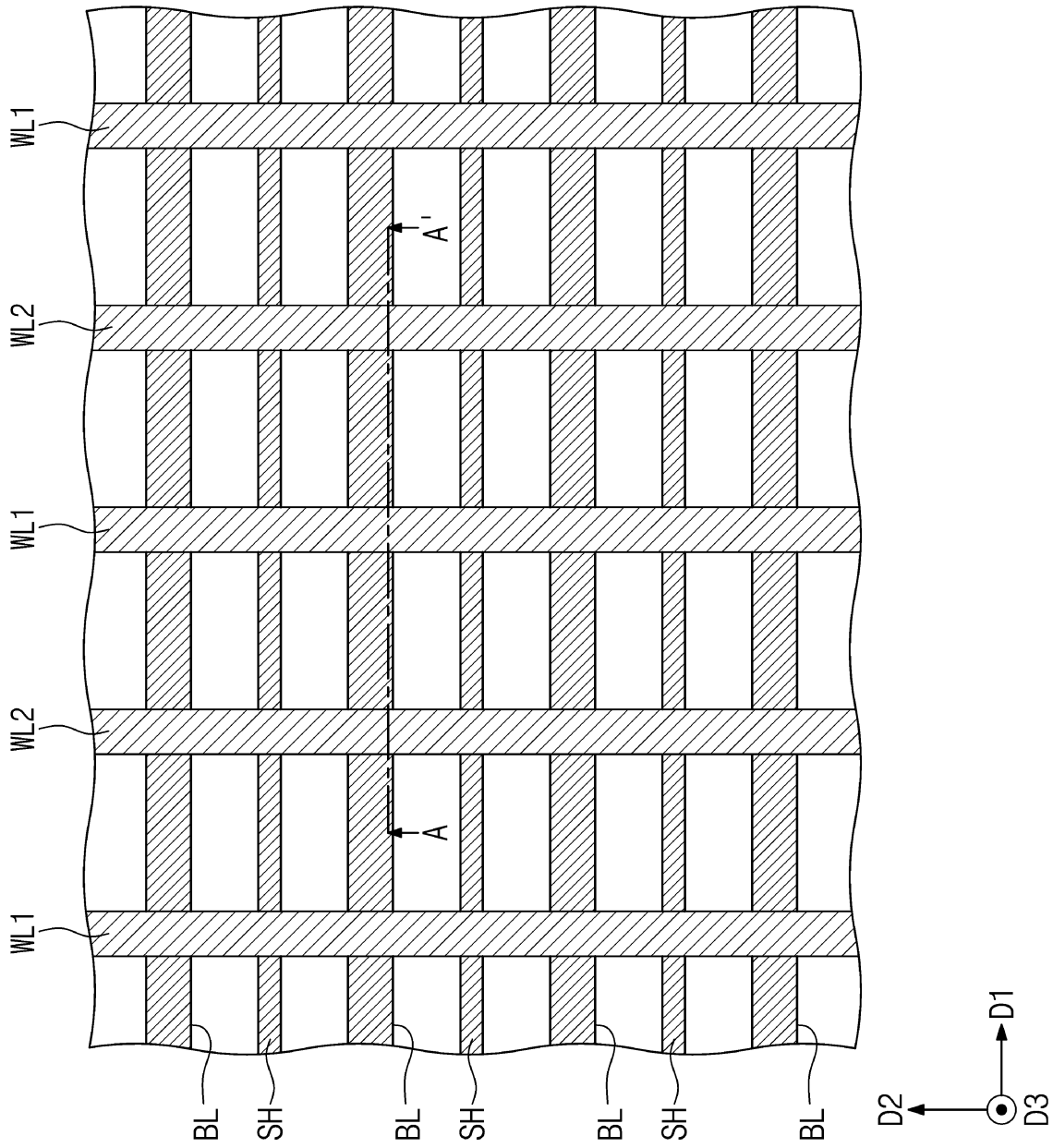


FIG. 16B

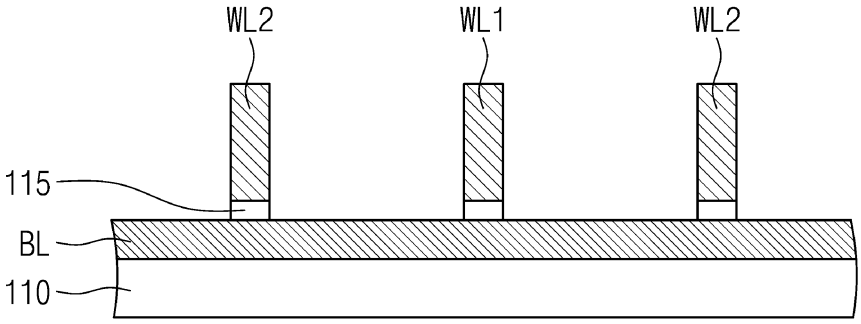


FIG. 17A

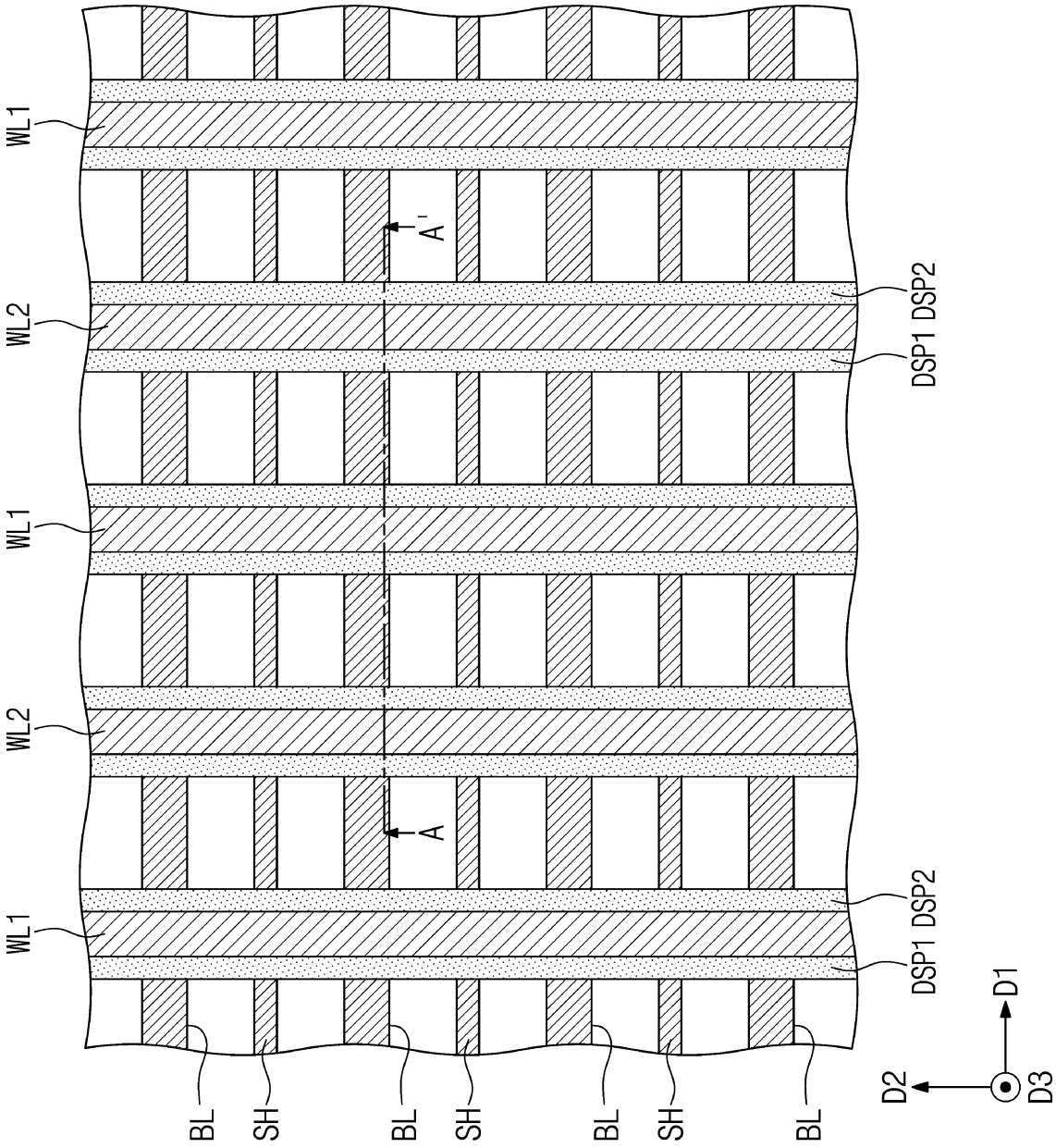

WL1
WL2
WL1
WL2
WL1
A'
A
DSP1 DSP2
DSP1 DSP2
BL
SH
BL
SH
BL
SH
BL
D1
D2
D3

FIG. 17B

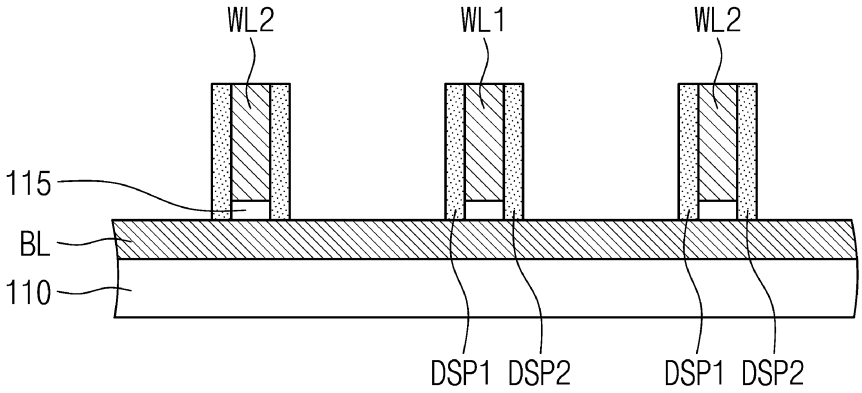


FIG. 18A

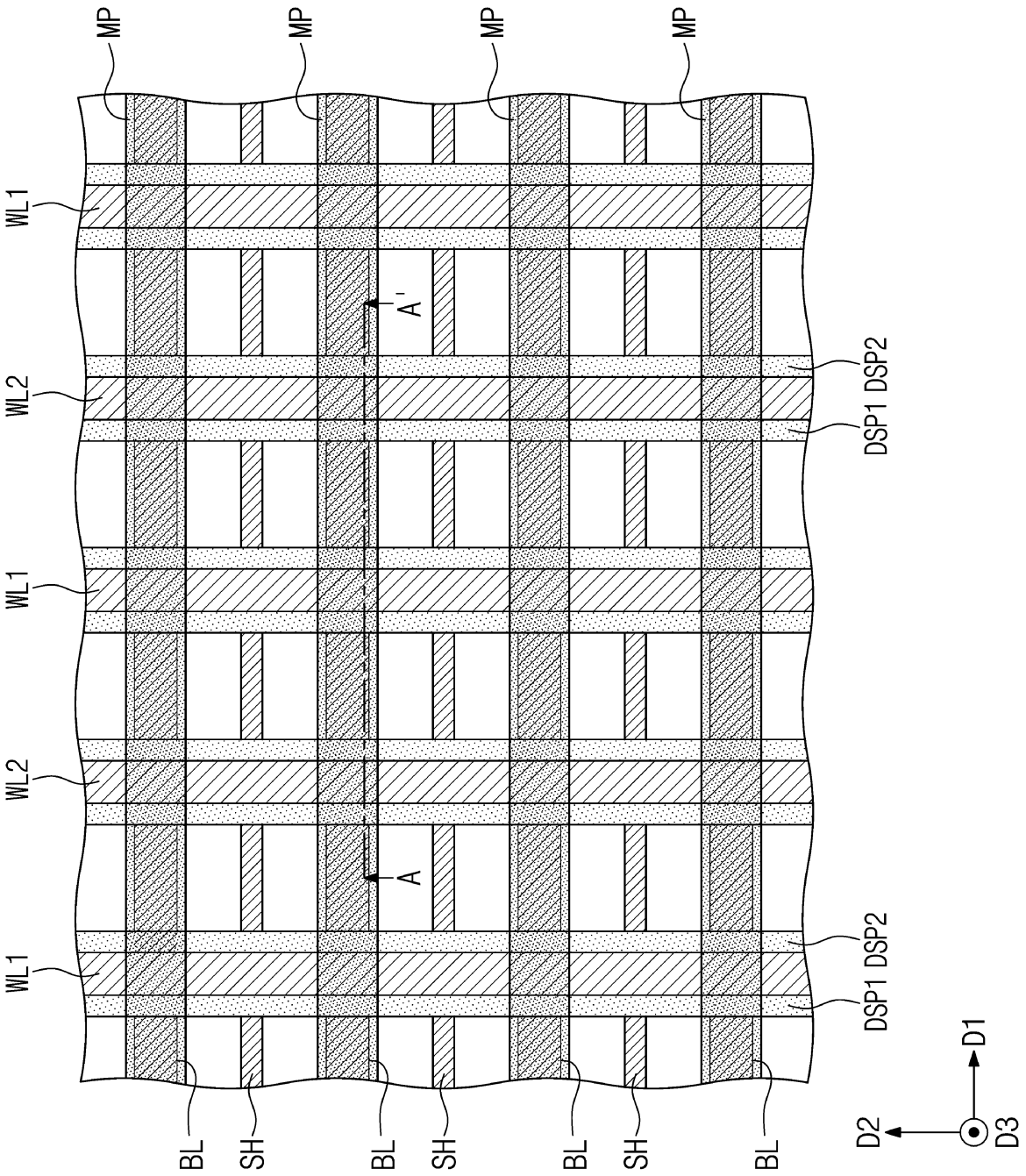

MP
MP
MP
MP
WL1
WL2
WL1
WL2
WL1
A'
A
DSP1 DSP2
DSP1 DSP2
BL
SH
BL
SH
BL
SH
BL
D2
D1
D3

FIG. 18B

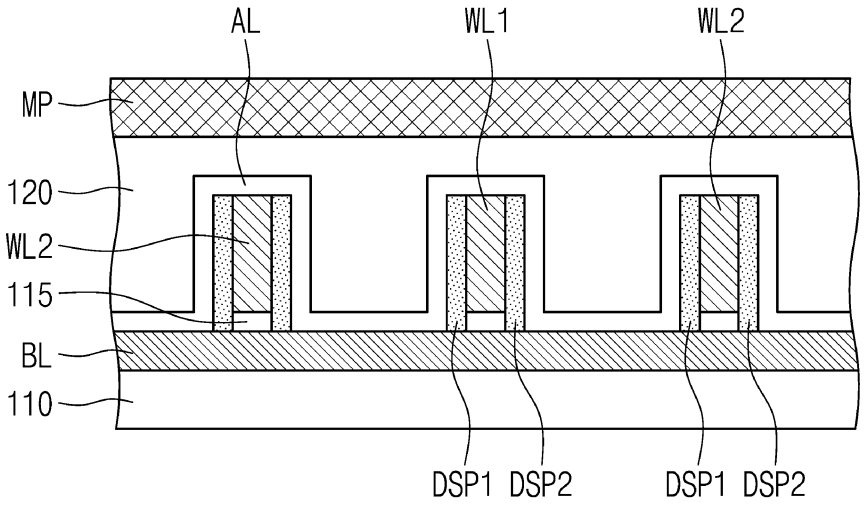


FIG. 19A

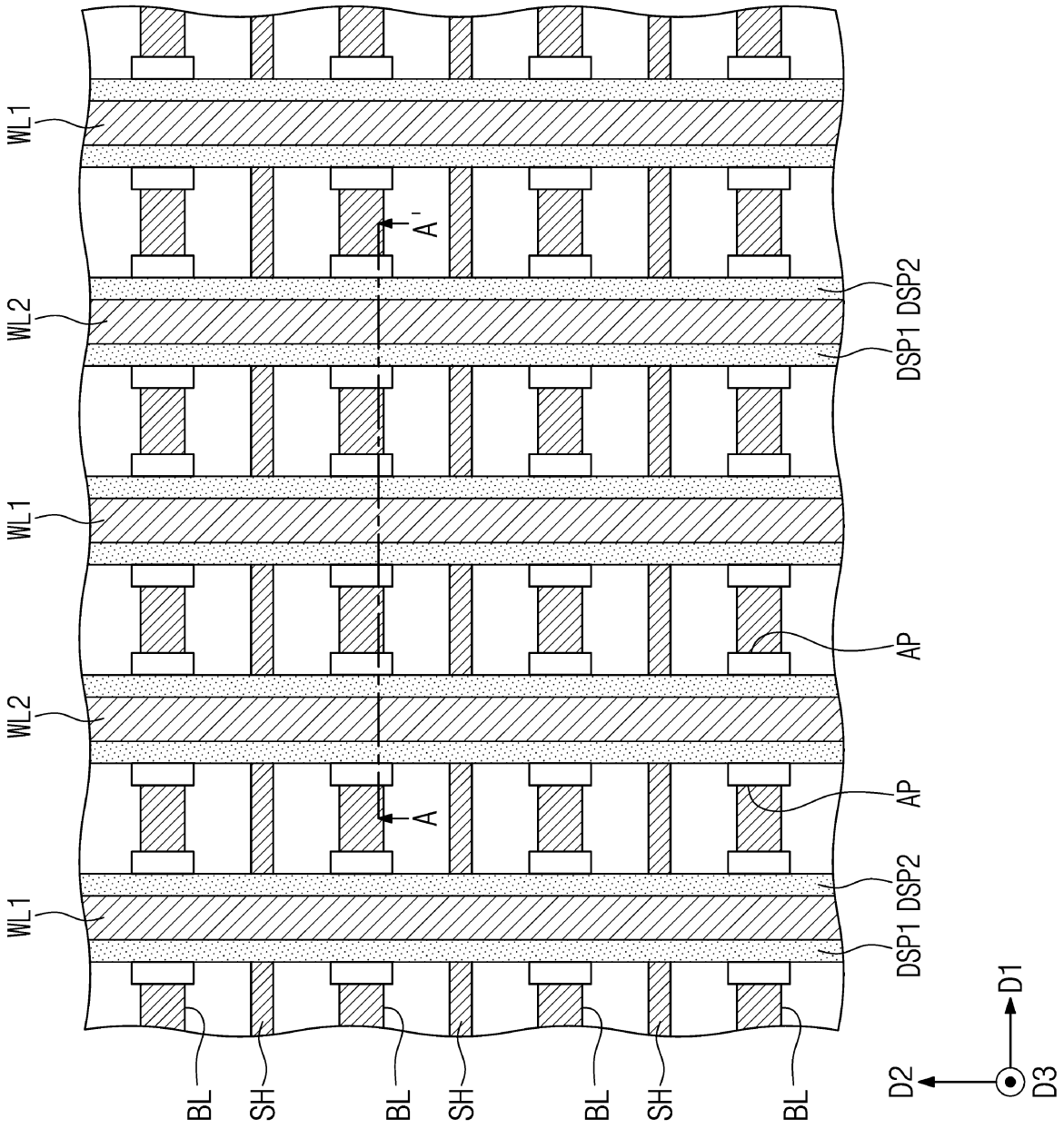

WL1
WL2
WL1
WL2
WL1
A'
A
DSP1 DSP2
DSP1 DSP2
AP
AP
BL
SH
BL
SH
BL
SH
BL
D1
D2
D3

FIG. 19B

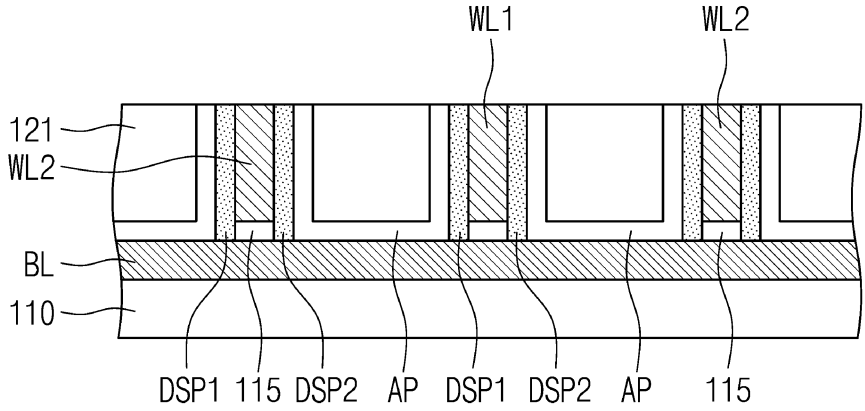


FIG. 20A

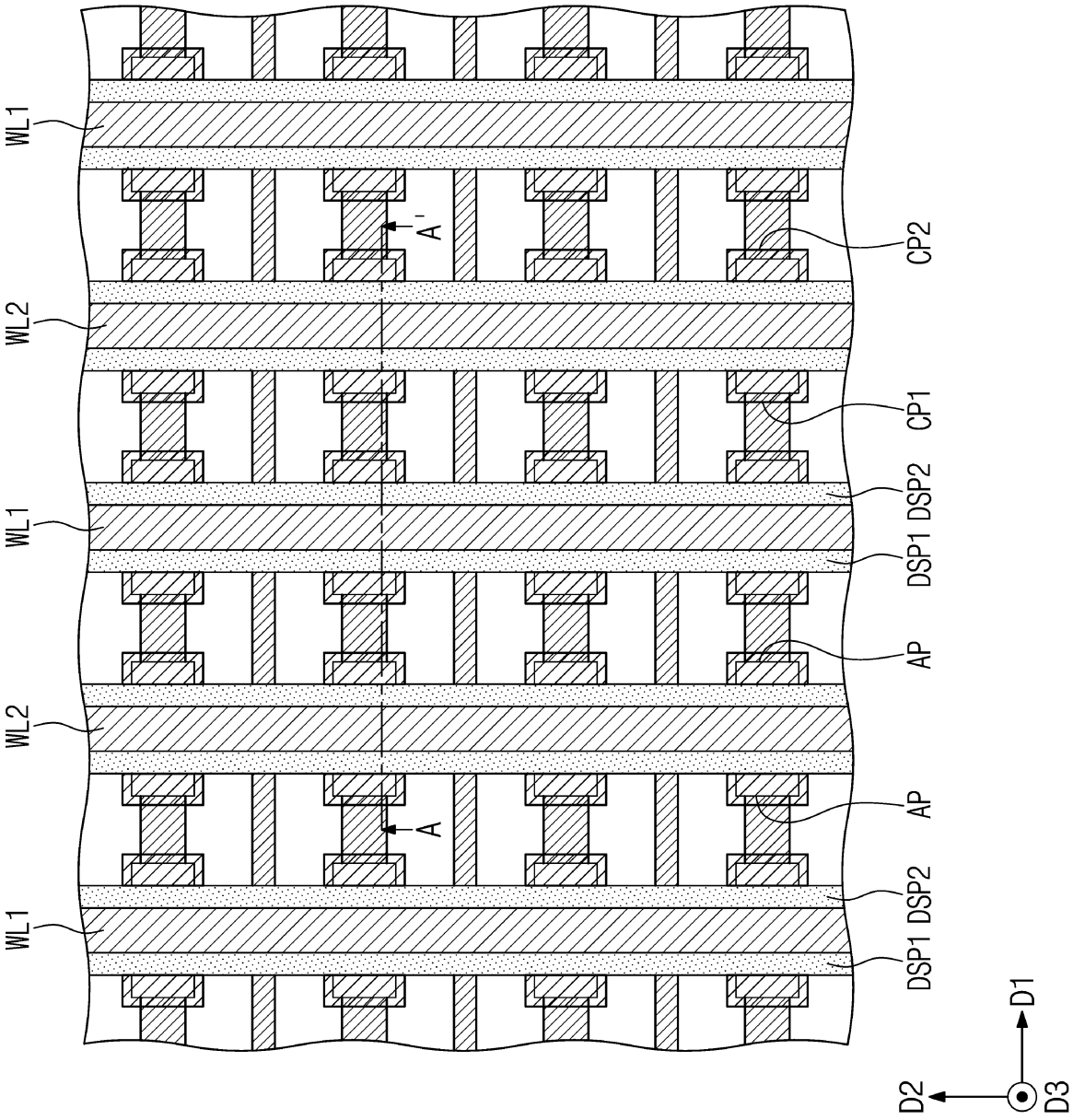


FIG. 20B

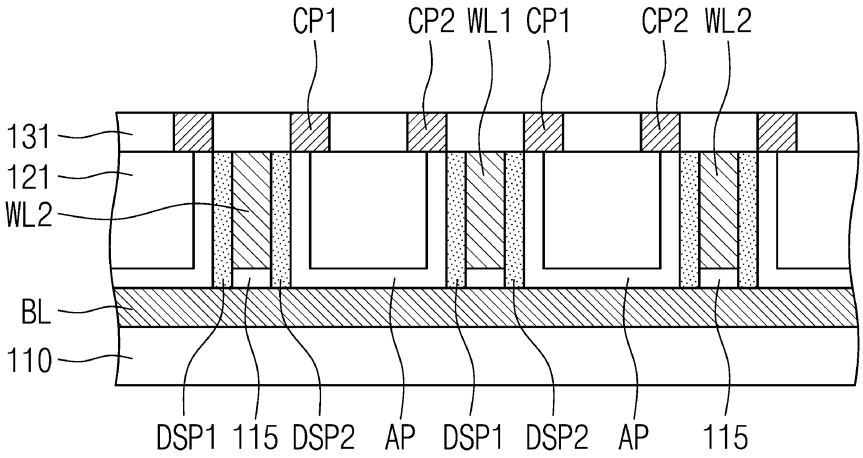

CP1
CP2
WL1
CP1
CP2
WL2
131
121
WL2
BL
110
DSP1
115
DSP2
AP
DSP1
DSP2
AP
115

FIG. 21A

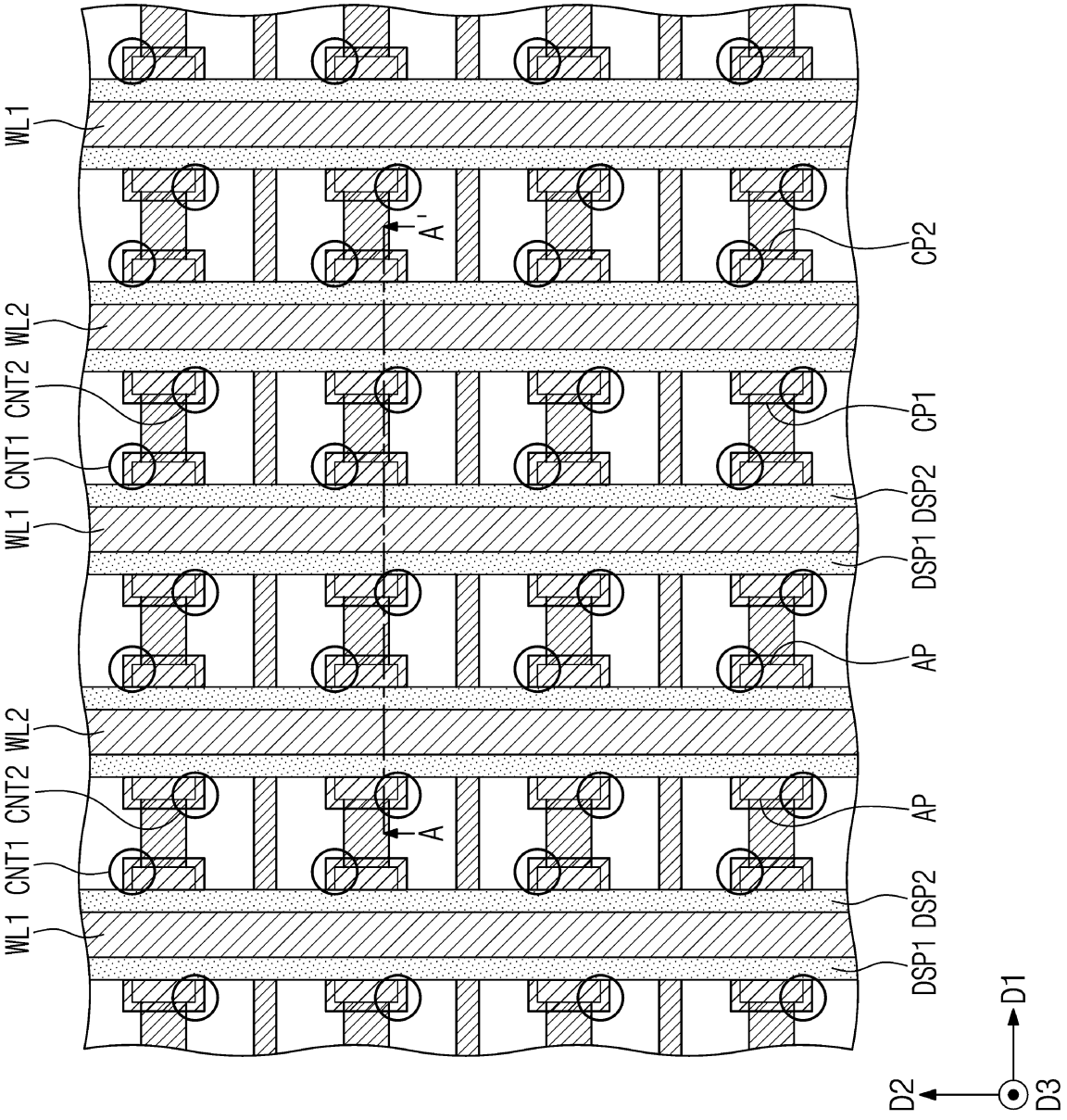

WL1
A'
CP2
WL2
CNT2
CP1
CNT1
DSP2
WL1
DSP1
AP
WL2
CNT2
AP
A
CNT1
DSP2
WL1
DSP1
D1
D2
D3

FIG. 21B

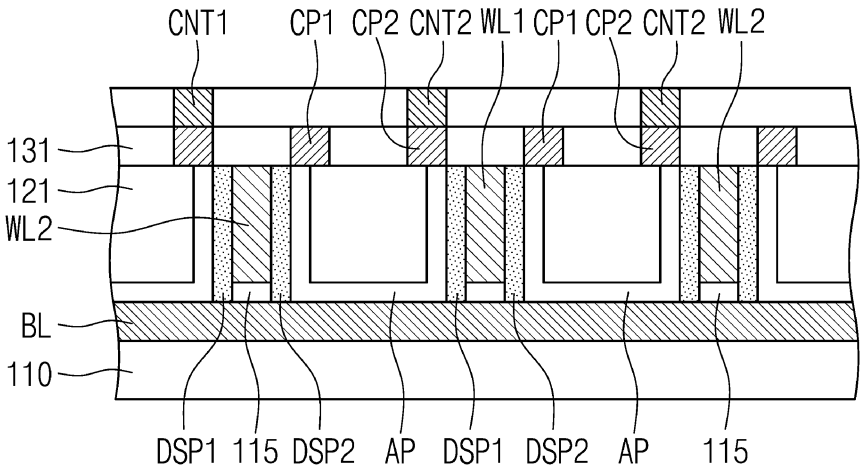

CNT1
CP1
CP2
CNT2
WL1
CP1
CP2
CNT2
WL2
131
121
WL2
BL
110
DSP1
115
DSP2
AP
DSP1
DSP2
AP
115

FIG. 22A

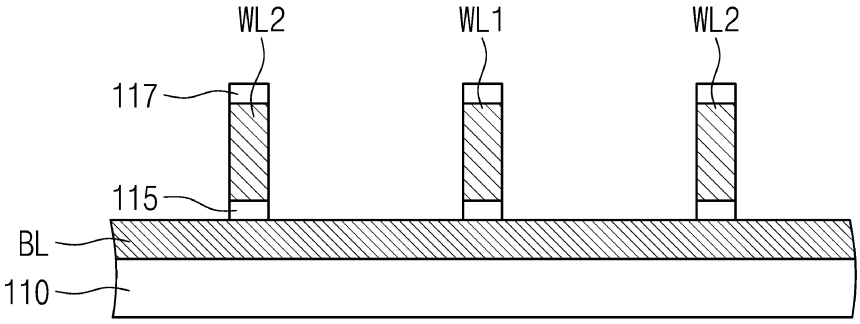


FIG. 22B

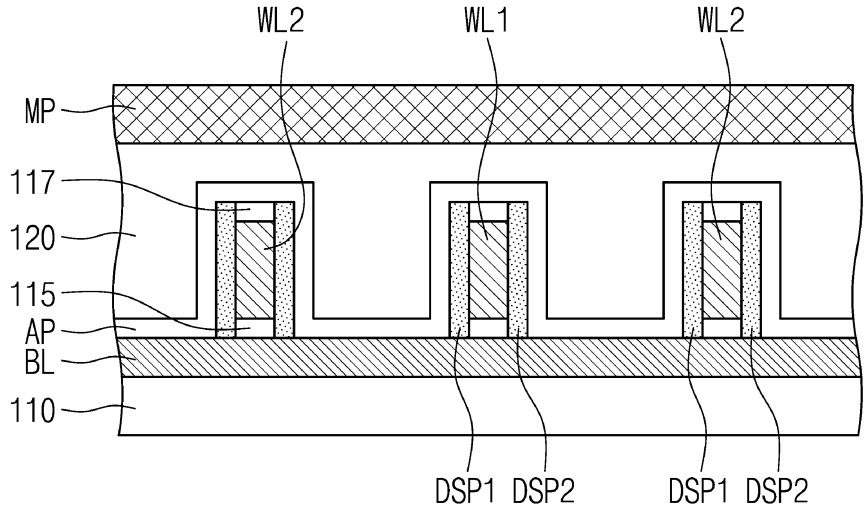


FIG. 22C

