circuit 70.

The latch circuit 80 latches flags FLG1 and FLG2 input from comparators 34 and 35, and outputs a signal OUT2 in accordance with the flags FLG1 and FLG2. As the latch circuit 80, for example, an SR (Set-Reset) flip-flop circuit is used. Details of the arrangement of the latch circuit 80 will be described later with reference to FIG. 9.

The discharge circuit 70 includes an input terminal and an output terminal. A signal OUT2 is input to the input terminal. The output terminal is electrically coupled to the output terminal of an operational amplifier 37. That is, the discharge circuit 70 discharges the level of the gate voltage of the regulation transistor 90 in accordance with the signal OUT2 input from the latch circuit 80. Details of the arrangement of the discharge circuit 70 will be described later with reference to FIG. 9.

As shown in FIG. 9, the latch circuit 80 includes an OR gate 81 and NAND gates 82 to 84.

The OR gate 81 performs the OR operation between the input flags FLG1 and FLG2, and outputs the result as a signal SET2. The NAND gate 82 performs the NAND operation between the input flags FLG1 and FLG2, and outputs the result as a signal RST2. The NAND gate 83 performs the NAND operation between the signal SET2 input from the OR gate 81 and a signal input from the NAND gate 84, and outputs the result as the signal OUT2. The NAND gate 84 performs the

C L A I M S

1. A voltage generation circuit comprising:

a charge pump circuit configured to boost a voltage input to a first node and output a first signal to a second node;

an operational amplifier configured to receive a first reference voltage and a first voltage obtained by dividing a voltage of the second node and output a second signal to a third node;

a first transistor having a gate coupled to the third node, one terminal coupled to a power supply, and the other terminal coupled to the first node;

a logic circuit configured to detect the voltage of the second node and output a third signal; and

a charge-up circuit configured to receive the third signal and charge a voltage of the third node, wherein

the charge-up circuit comprises:

a first PMOS transistor having a gate configured to receive a fourth signal based on the third signal and one terminal coupled to a power supply voltage; and

a second PMOS transistor having one terminal coupled to the other terminal of the first PMOS transistor and the other terminal and a gate coupled to a fourth node.

2. The voltage generation circuit of claim 1, wherein the charge-up circuit further comprises a first NAND gate configured to perform a NAND operation between the third signal and a fifth signal obtained by delaying and

inverting the third signal and output a result as the fourth signal.

3. The voltage generation circuit of claim 1, wherein the logic circuit includes a limiter circuit comprising:

a first comparator configured to compare the first reference voltage with a voltage based on the voltage of the second node and output a first flag; and

a second comparator configured to compare a second reference voltage equal to the first reference voltage with the voltage based on the voltage of the second node and output a second flag.

4. The voltage generation circuit of claim 3, wherein the logic circuit includes a first latch circuit that is an SR flip-flop circuit.

5. The voltage generation circuit of claim 3, wherein the logic circuit includes a first latch circuit comprising:

a first OR gate configured to perform an OR operation between the first flag and the second flag and output a result as a sixth signal;

a second NAND gate configured to perform a NAND operation between the first flag and the second flag and output a result as a seventh signal;

a third NAND gate configured to perform a NAND operation between the seventh signal and the third signal and output a result as an eighth signal; and

a fourth NAND gate configured to perform a NAND

operation between the sixth signal and the eighth signal and output a result as the third signal.

6. The voltage generation circuit of claim 1, further comprising a clock control circuit configured to output a clock signal in accordance with the third signal,

wherein the charge pump circuit controls boost of a voltage of the first node in accordance with the clock signal.

7. The voltage generation circuit of claim 3, further comprising:

a second latch circuit configured to output a ninth signal in accordance with the first flag and the second flag; and

a discharge circuit configured to discharge a voltage of the third node in accordance with the ninth signal.

8. The voltage generation circuit of claim 7, wherein the discharge circuit comprises a first NMOS transistor having a gate configured to receive a 10th signal based on the ninth signal and one terminal coupled to a ground potential.

9. The voltage generation circuit of claim 8, wherein the discharge circuit further comprises a first NOR gate configured to perform a NOR operation between the ninth signal and a 11th signal obtained by delaying and inverting the ninth signal and output a result as the 10th signal.

10. The voltage generation circuit of claim 7, wherein

the second latch circuit comprises:

a second OR gate configured to perform an OR operation between the first flag and the second flag and output a result as a 12th signal;

a fifth NAND gate configured to perform a NAND operation between the first flag and the second flag and output a result as a 13th signal;

a sixth NAND gate configured to perform a NAND operation between the 13th signal and the ninth signal and output a result as a 14th signal; and

a seventh NAND gate configured to perform a NAND operation between the 12th signal and the 14th signal and output a result as the ninth signal.

11. A voltage generation circuit comprising:

a charge pump circuit configured to boost a voltage input to a first node and output a first signal to a second node;

an operational amplifier configured to receive a first reference voltage and a first voltage obtained by dividing a voltage of the second node and output a second signal to a third node;

a first transistor having a gate coupled to the third node, one terminal coupled to a power supply, and the other terminal coupled to the first node;

a logic circuit configured to detect the voltage of the second node, generate a first flag and a second flag, and output a third signal based on the first flag and the

second flag;

a first latch circuit configured to receive the first flag and the second flag and output a fourth signal; and

a discharge circuit configured to receive the fourth signal and discharge a voltage of the third node.

12. The voltage generation circuit of claim 11, wherein the discharge circuit comprises a first NMOS transistor having a gate configured to receive a fifth signal based on the fourth signal and one terminal coupled to a ground potential.

13. The voltage generation circuit of claim 12, wherein the discharge circuit further comprises a first NOR gate configured to perform a NOR operation between the fourth signal and a sixth signal obtained by delaying and inverting the fourth signal and output a result as the fifth signal.

14. The voltage generation circuit of claim 11, wherein the first latch circuit comprises:

a first OR gate configured to perform an OR operation between the first flag and the second flag and output a result as a seventh signal;

a first NAND gate configured to perform a NAND operation between the first flag and the second flag and output a result as an eighth signal;

a second NAND gate configured to perform a NAND operation between the eighth signal and the fourth signal and output a result as a ninth signal; and

a third NAND gate configured to perform a NAND operation between the seventh signal and the ninth signal and output a result as the fourth signal.