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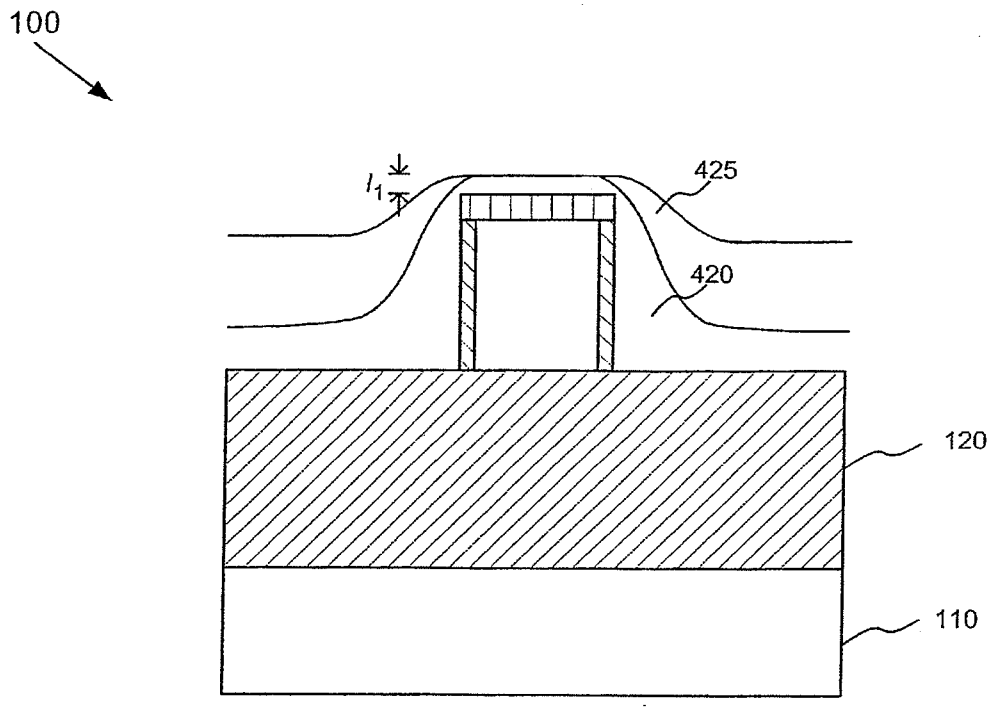
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[Continued on next page]

(54) Title: FINFET WITH DUAL SILICON GATE LAYER FOR CHEMICAL MECHANICAL POLISHING PLANARIZATION



(57) Abstract: A FinFET-type semiconductor device includes a fin structure (210) on which a relatively thin amorphous silicon layer (420) and then an undoped polysilicon layer (425) is formed. The semiconductor device may be planarized using a chemical mechanical polishing (CMP) in which the amorphous silicon layer (420) act as a stop layer to prevent damage to the fin structure.

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