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SYSTEM AND METHOD FOR MANAGING SYSTEM MANAGEMENT INTERRUPTS IN
A MULTIPROCESSOR COMPUTER SYSTEM

ABSTRACT OF THE DISCLOSURE

5 A system and method is disclosed in which, during the execution of an interrupt
handling sequence in one of the processor of a multiprocessor system, a processors write a
reason code to a status register to identify the cause of the interrupt. The BIOS code of the
system writes to an interrupt initiation register to cause each of the processors to enter an
interrupt handling sequence. Each of the processors of the system handling the interrupt on the
10 basis of the content of the status register, resulting in each of the processors synchronously
handling an interrupt for an event that would otherwise result in a local interrupt.

FIG. 2