We Claim:

1. A ~~heating plate for a~~ substrate support assembly used to support a semiconductor substrate in a semiconductor processing apparatus, comprising:

an electrostatic chuck (ESC) including an electrostatic clamping layer having at least one clamping electrode configured to electrostatically clamp a semiconductor substrate on the substrate support assembly;

a heating plate arranged below the electrostatic clamping layer;

a cooling plate attached to a lower side of the heating plate by a thermal barrier layer;

the heating plate comprising:

a first electrically insulating layer;

planar heater zones comprising at least first, second, third and fourth planar heater zones, each comprising one or more heater elements, the planar heater zones laterally distributed across the first electrically insulating layer and operable to tune a spatial temperature profile on the substrate;

power supply lines comprising at least a first electrically conductive power supply line electrically connected to the first and second planar heater zones and a second electrically conductive power supply line electrically connected to the third and fourth planar heater zones;

power return lines comprising at least a first electrically conductive power return line electrically connected to the first and third planar heater zones and a second electrically conductive power return line electrically connected to the second and fourth planar heater zones~~.~~; and

wherein (a) the power supply lines are connected to leads electrically insulated from each other and extended through at least one power supply conduit in the cooling plate and the power return lines are connected to leads electrically insulated from each other and extended through at least one power return conduit in the cooling plate; or (b) the power supply lines and power return lines are connected to terminal connectors embedded in the cooling plate.

2. The ~~heating plate~~ substrate support assembly of claim 1, wherein

(a) the planar heater zones and the power supply lines are in a first plane; the power return lines are in a second plane parallel to the first plane; the first and second planes are separated from one another by the first electrically insulating layer; the power return lines are

electrically connected to the planar heater zones by vias extending vertically in the first electrically insulating layer;

(b) the planar heater zones and the power return lines are in a first plane; the power supply lines are in a second plane parallel to the first plane; the first and second planes are separated from one another by the first electrically insulating layer; the power supply lines are electrically connected to the planar heater zones by vias extending vertically in the first electrically insulating layer; or

(c) the planar heater zones are in a first plane; the power supply lines are in a second plane parallel to the first plane; the power return lines are in a third plane parallel to the first plane; the first and second planes are separated by the first electrically insulating layer; the second and third planes are separated by a second electrically insulating layer; the power supply lines and power return lines are electrically connected to the planar heater zones by vias extending through the electrically insulating layers.

3. The ~~heating plate~~substrate support assembly of claim 1, wherein the planar heater zones are sized such that:

(a) each planar heater zone is not larger than four device dies being manufactured on the semiconductor substrate, or

(b) each planar heater zone is not larger than two device dies being manufactured on the semiconductor substrate, or

(c) each planar heater zone is not larger than one device die being manufactured on the semiconductor substrate, or

(d) the area of each planar heater zone is between 2 and 3 square centimeters, or

(e) the heating plate includes 100 to 400 planar heater zones, or

(f) each planar heater zone is 1 to 15 cm^2, or

(g) each planar heater zone is 16 to 100 cm^2, or

(h) each planar heater zone is scaled with sizes of device dies on the semiconductor substrate and the overall size of the semiconductor substrate.

4. The ~~heating plate~~substrate support assembly of claim 1, wherein the first electrically insulating layer comprises a polymer material, a ceramic material, or a combination thereof.

5. The ~~heating plate~~substrate support assembly of claim 1, wherein the total number of the power supply lines and the power return lines is equal to or less than the total number of the planar heater zones.

6. The ~~heating plate~~substrate support assembly of claim 1, wherein a total area of the planar heater zones is from 50% to 90% of an upper surface of the heating plate.

7. The ~~heating plate~~substrate support assembly of claim 1, wherein the planar heater zones are arranged in a rectangular grid, hexagonal grid or concentric rings; and the planar heater zones are separated from each other by gaps at least 1 millimeter in width and at most 10 millimeters in width.

8. The ~~heating plate~~substrate support assembly of claim 1, wherein a rectifier is serially connected between each heater zone and the power supply line connected thereto, or a rectifier is serially connected between each heater zone and the power return line connected thereto.

9. The ~~heating plate~~ substrate support assembly of claim 8, wherein the rectifier is a semiconductor diode.

~~10. A substrate support assembly comprising:~~

~~an electrostatic chuck (ESC) including an electrostatic clamping layer having at least one clamping electrode configured to electrostatically clamp a semiconductor substrate on the substrate support assembly;~~

~~the heating plate of claim 1 arranged below the electrostatic clamping layer;~~

~~a cooling plate attached to a lower side of the heating plate by a thermal barrier layer.~~

~~11. The substrate support assembly of claim 10, wherein:~~

~~(a) the power supply lines are connected to leads electrically insulated from each other and extended through at least one power supply conduit in the cooling plate and the power~~

~~return lines are connected to leads electrically insulated from each other and extended through at least one power return conduit in the cooling plate; or~~

~~(b) the power supply lines and power return lines are connected to terminal connectors embedded in the cooling plate.~~

~~12~~10. The substrate support assembly of claim ~~10~~ 1, further comprising a control and power circuit operable to selectively supply power at any given time to (a) only the first heater zone, (b) only the second heater zone, (c) only the third heater zone, (d) only the fourth heater zone, (e) only the first and second planar heater zones, (f) only the first and third planar heater zones, (g) only the second and fourth planar heater zones, (h) only the third and fourth planar heater zones, and (i) all of the planar heater zones.

~~13~~11. The substrate support assembly of claim ~~12~~10, further comprising at least one filter or isolator serially connected between the control and power circuit and electric ground.

~~14~~12. The substrate support assembly of claim ~~13~~11, wherein the at least one filter or isolator is a transformer.

~~15.~~13. The substrate support assembly of claim ~~10~~1, further comprising at least one primary heater layer arranged above or below the first electrically insulating layer of the heating plate, wherein the primary heater layer is electrically insulated from the planar heater zones, the power supply lines, and the power return lines of the heating plate; the primary heater layer includes at least one heater which provides mean temperature control of the semiconductor substrate; the planar heater zones provide radial and azimuthal temperature profile control of the semiconductor substrate, during processing thereof.

14. The substrate support assembly of claim 1, wherein the terminal connectors are spring-tipped passthroughs.

15. The substrate support assembly of claim 13, wherein the primary heater layer includes two or more heaters.

16. A heating plate configured to provide radial and azimuthal temperature control of a semiconductor substrate supported on a semiconductor substrate support in a processing chamber, comprising:

a first layer having an array of heater zones operable to tune a spatial temperature profile on the semiconductor substrate, the heater zones powered by two or more power supply lines and two or more power return lines wherein each power supply line is connected to at least two of the heater zones and each power return line is connected to at least two of the heater zones, each heater zone not larger than four device dies being manufactured on the semiconductor substrate, and

a second layer having one or more primary heaters operable to provide mean temperature control of the semiconductor substrate during processing in the processing chamber.

17. A substrate support comprising:

a heating plate configured to provide radial and azimuthal temperature control of a semiconductor substrate supported on a semiconductor substrate support in a processing chamber, comprising:

a first layer having an array of heater zones operable to tune a spatial temperature profile on the semiconductor substrate, the heater zones powered by two or more power supply lines and two or more power return lines wherein each power supply line is connected to at least two of the heater zones and each power return line is connected to at least two of the heater zones, each heater zone not larger than four device dies being manufactured on the semiconductor substrate, and

a second layer having one or more primary heaters operable to provide mean temperature control of the semiconductor substrate during processing in the processing chamber;

a switching device which independently supplies power to each one of the heater zones via one of the power supply lines and one of the power return lines to provide time-averaged power to each of the heater zones by time divisional multiplexing of the switches; and

a temperature controlled and radio frequency (RF) powered base plate beneath the heating plate and high side circuitry housed in local faraday cage under the base plate.

18. A heating plate configured to provide radial and azimuthal temperature control of a

semiconductor substrate supported on a semiconductor substrate support in a processing chamber, comprising:

a first layer having an array of heater zones operable to tune a spatial temperature profile on the semiconductor substrate, the heater zones powered by two or more power supply lines and two or more power return lines wherein each power supply line is connected to at least two of the heater zones and each power return line is connected to at least two of the heater zones, each heater zone not larger than four device dies being manufactured on the semiconductor substrate;

a second layer having one or more primary heaters operable to provide mean temperature control of the semiconductor substrate during processing in the processing chamber;

the heating plate includes a first electrically insulating layer with planar heater zones distributed laterally across the first electrically insulating layer and comprising at least first, second, third and fourth planar heater zones, each planar heater zone having one or more heater elements;

the power supply lines comprise at least a first electrically conductive power supply line electrically connected to the first and second planar heater zones and a second electrically conductive power supply line electrically connected to the third and fourth planar heater zones; and

the power return lines comprise at least a first electrically conductive power return line electrically connected to the first and third planar heater zones and a second electrically conductive power return line electrically connected to the second and fourth planar heater zones.

19. The heating plate of claim 16, wherein the heating plate is incorporated in a substrate support which includes temperature sensors configured to measure temperature at locations on the semiconductor substrate; and

a control and power circuit connected to the array of heater zones and configured to receive the measured parameters from the temperature sensors and adjust power delivered to the heater zones to minimize differences between the measured parameters and set targets.

20. The substrate support of claim 17, further comprising:

an isolator connected to electric ground,

wherein the switching device is connected to the isolator.

21. The substrate support of claim 20, wherein the switching device is located in a plasma etching chamber.

22. The substrate support of claim 20, wherein the isolator is an isolation transformer that isolates the switching device from RF.

23. A heating plate configured to provide radial and azimuthal temperature control of a semiconductor substrate supported on a semiconductor substrate support in a processing chamber, comprising:

a first layer having an array of heater zones operable to tune a spatial temperature profile on the semiconductor substrate, the heater zones powered by two or more power supply lines and two or more power return lines wherein each power supply line is connected to at least two of the heater zones and each power return line is connected to at least two of the heater zones, each heater zone not larger than four device dies being manufactured on the semiconductor substrate;

a second layer having one or more primary heaters operable to provide mean temperature control of the semiconductor substrate during processing in the processing chamber;

the heater zones are supported on a first electrically insulating layer;

the second layer is arranged above or below the first electrically insulating layer; and

the one or more primary heaters are electrically insulated from the array of heater zones, the power supply lines, and the power return lines.

24. The substrate support of claim 17, wherein the switching device is a high side controller that floats at an RF potential, the substrate support further comprising:

an optical coupler connected to the high side controller for digital communication with a low-side controller.

25. The substrate support of claim 17, wherein the switching device connects at least one power return line to a floating reference.

26. The substrate support of claim 17, wherein the switching device is configured to turn on one of the heater zones when at least one power supply line connected to the heater zone is connected to a power supply, and at least one power return line connected to the heater zone is connected to a floating reference.

27. The substrate support of claim 17, wherein the switching device connects all power return lines to a floating reference.

28. The substrate support of claim 17, wherein the switching device is configured to address each heater zone of the array of heater zones at a frequency of at least 1 Hz.

29. A substrate support comprising the heating plate of claim 16, wherein the substrate support includes sensors configured to measure parameters on different locations on the substrate support and power of the heater zones.

30. The substrate support of claim 29, wherein the sensors include at least one of voltage and current sensors.

31. The substrate support of claim 29, wherein the measured parameters include at least temperature measurements.

32. The substrate support of claim 17, wherein the switching device is configured to maintain a connection between all power return lines and a floating reference during a time when one power supply line is powered and regulate power transmitted to heat a heater zone that is turned on.

33. A substrate support, comprising:

a heating plate configured to provide radial and azimuthal temperature control of a semiconductor substrate supported on a semiconductor substrate support in a processing chamber, comprising:

a first layer having an array of heater zones operable to tune a spatial temperature profile on the semiconductor substrate, the heater zones powered by two or more power supply lines and two or more power return lines wherein each power supply line is connected to at least two of the heater zones and each power return line is connected to at least two of the heater zones, each heater zone not larger than four device dies being manufactured on the semiconductor substrate, and

a second layer having one or more primary heaters operable to provide mean temperature control of the semiconductor substrate during processing in the processing chamber; and

an electrostatic clamping (ESC) layer above the heating plate.

34. The substrate support of claim 33, further comprising a radio frequency (RF) powered base plate beneath the heating plate.

35. The heating plate of claim 16, wherein the heater zones comprise at least 100 independently controllable heater zones embedded in ceramic material.

~~16~~36. A method for manufacturing ~~the heating plate of claim 1~~ a heating plate for a substrate support assembly used to support a semiconductor substrate in a semiconductor processing apparatus, the heating plate comprising a first electrically insulating layer; planar heater zones comprising at least first, second, third and fourth planar heater zones, each comprising one or more heater elements, the planar heater zones laterally distributed across the first electrically insulating layer and operable to tune a spatial temperature profile on the substrate; power supply lines comprising at least a first electrically conductive power supply line electrically connected to the first and second planar heater zones and a second electrically conductive power supply line electrically connected to the third and fourth planar heater zones; power return lines comprising at least a first electrically conductive power return line electrically connected to the first and third planar heater zones and a second electrically conductive power return line electrically connected to the second and fourth planar heater zones, the method comprising:

(a) forming holes in ceramic sheets;

(b) ~~screen~~ printing a slurry of conductor powder, or pressing a precut metal foil, or spraying a slurry of conductor powder, on the ceramic sheets to form the planar heater zones, the power supply lines, and power return lines;

(c) filling the holes in the ceramic sheets with a slurry of conductor powder to form power supply and power return vias; and

(d) aligning, pressing and bonding the ceramic sheets to form the heating plate.

~~17~~37. The method of claim 36 ~~for manufacturing the heating plate~~, wherein:

~~(a)~~ the planar heater zones and power supply lines are formed on the upper side of a first ceramic sheet, the power return lines are formed on the lower side of the first ceramic sheet, a second ceramic sheet is placed over the upper surface of the first ceramic sheet and a third ceramic sheet is placed below the first ceramic sheet, and the first, second and third ceramic sheets are pressed together and sintered to form a joint-free heating plate~~; or~~

~~(b) the planar heater zones are formed on the upper side of a first ceramic sheet, the power supply lines are formed on the upper side of a second ceramic sheet placed below the first ceramic sheet, the power return lines are formed on the upper side of a third ceramic sheet placed below the second ceramic sheet, a fourth ceramic sheet is placed over the upper surface of the first ceramic sheet, and the first, second, third and fourth ceramic sheets are pressed together and sintered to form a joint-free heating plate~~.

~~18~~38. A method for manufacturing ~~the heating plate of claim 1~~a heating plate for a substrate support assembly used to support a semiconductor substrate in a semiconductor processing apparatus, the heating plate comprising a first electrically insulating layer; planar heater zones comprising at least first, second, third and fourth planar heater zones, each comprising one or more heater elements, the planar heater zones laterally distributed across the first electrically insulating layer and operable to tune a spatial temperature profile on the substrate; power supply lines comprising at least a first electrically conductive power supply line electrically connected to the first and second planar heater zones and a second electrically conductive power supply line electrically connected to the third and fourth planar heater zones; power return lines comprising at least a first electrically conductive power return line electrically connected to the first and third planar heater zones and a second electrically conductive power return line electrically connected to the second and fourth planar heater zones, the method comprising:

manufacturing a component layer ~~including steps:~~ of the heating plate by:

(a) bonding a metal sheet onto a polymer film;

~~(b) applying a patterned resist film onto the metal sheet wherein openings in the patterned resist film correspond to locations where metal is to be removed;~~

~~(c)~~(b) etching the metal sheet to remove metal exposed through openings of ~~the resist~~ a patterned film, the etching forming an electrically conductive metal pattern of at ~~—~~least one of the planar heater zones, power supply lines and~~/or~~ power return lines; and

~~(d)~~(c) removing the ~~resist~~ film;

manufacturing a via layer ~~including steps:~~ by:

(a) punching or cutting holes in a polymer film; and

(b) forming conductive vias in the holes;

building a laminate by bonding at least one ~~or more~~manufactured component ~~layers~~layer and at least one ~~or more~~manufactured via ~~layers~~layer; and

insulating the laminate by bonding a continuous polymer film onto at least one of upper and~~/or~~ lower surfaces of the laminate.

~~19~~39. A method for manufacturing ~~the heating plate of claim 1~~ a heating plate for a substrate support assembly used to support a semiconductor substrate in a semiconductor processing apparatus, the heating plate comprising a first electrically insulating layer; planar heater zones comprising at least first, second, third and fourth planar heater zones, each comprising one or more heater elements, the planar heater zones laterally distributed across the first electrically insulating layer and operable to tune a spatial temperature profile on the substrate; power supply lines comprising at least a first electrically conductive power supply line electrically connected to the first and second planar heater zones and a second electrically conductive power supply line electrically connected to the third and fourth planar heater zones; power return lines comprising at least a first electrically conductive power return line electrically connected to the first and third planar heater zones and a second electrically conductive power return line electrically connected to the second and fourth planar heater zones, the method comprising:

depositing metal, amorphous conductive inorganic material, or conductive ceramic on the first electrically insulating layer to form at least one of the planar heater zones, power supply lines and~~/or~~ power return lines.

~~20~~40. A method for ~~plasma~~ processing semiconductor substrates in a ~~plasma~~semiconductor

processing ~~chamber~~apparatus containing ~~the substrate support assembly of claim 10~~ a substrate support assembly comprising an electrostatic chuck (ESC) including an electrostatic clamping layer having at least one clamping electrode configured to electrostatically clamp a semiconductor substrate on the substrate support assembly; a heating plate arranged below the electrostatic clamping layer, the heating layer comprising a first electrically insulating layer; planar heater zones comprising at least first, second, third and fourth planar heater zones, each comprising one or more heater elements, the planar heater zones laterally distributed across the first electrically insulating layer and operable to tune a spatial temperature profile on the substrate; power supply lines comprising at least a first electrically conductive power supply line electrically connected to the first and second planar heater zones and a second electrically conductive power supply line electrically connected to the third and fourth planar heater zones; power return lines comprising at least a first electrically conductive power return line electrically connected to the first and third planar heater zones and a second electrically conductive power return line electrically connected to the second and fourth planar heater zones; and a cooling plate attached to a lower side of the heating plate by a thermal barrier layer, the method comprising:

(a) loading a semiconductor substrate into the processing chamber and positioning the semiconductor substrate on the substrate support assembly;

(b) determining a temperature profile ~~that compensates~~ for processing conditions affecting critical dimension (CD) uniformity~~;~~

(c) heating the semiconductor substrate to conform to the temperature profile using the substrate support assembly;

(d) ~~igniting plasma and~~ processing the semiconductor substrate while controlling the temperature profile by independently controlled heating of the planar heater zones;

(e) unloading the semiconductor substrate from the processing chamber and repeating steps (a)-(e) with a different semiconductor substrate.

41. The method of claim 36, wherein the planar heater zones are formed on a first ceramic sheet, the power supply lines are formed on a second ceramic sheet placed below the first ceramic sheet, the power return lines are formed on a third ceramic sheet placed below the second ceramic sheet, a fourth ceramic sheet is placed over the first ceramic sheet, and the first, second, third and fourth ceramic sheets are pressed together and sintered to form a joint-free heating plate.

42. The method of claim 41, wherein the first, second, third, and fourth ceramic sheets are aligned prior to being pressed together and sintered.

43. The method of claim 37, wherein the first, second, and third ceramic sheets are aligned prior to being pressed together and sintered.

44. The method of claim 36, comprising pressing or cutting recesses into the ceramic sheets formed into the heating plate and mounting rectifiers in the recesses.

45. The method of claim 36, comprising connecting a rectifier between each heater zone and the power supply line or power return line connected thereto.

46. A method for manufacturing a heating plate for a substrate support assembly used to support a semiconductor substrate in a semiconductor processing apparatus, the heating plate comprising a first electrically insulating layer; planar heater zones comprising at least first, second, third and fourth planar heater zones, each comprising one or more heater elements, the planar heater zones laterally distributed across the first electrically insulating layer and operable to tune a spatial temperature profile on the substrate; power supply lines comprising at least a first electrically conductive power supply line electrically connected to the first and second planar heater zones and a second electrically conductive power supply line electrically connected to the third and fourth planar heater zones; power return lines comprising at least a first electrically conductive power return line electrically connected to the first and third planar heater zones and a second electrically conductive power return line electrically connected to the second and fourth planar heater zones, the method comprising:

forming a manufactured component layer of the heating plate by:

(a) bonding a sheet onto a polymer film;

(b) applying a second film onto the sheet wherein openings in the second film correspond to locations where metal is to be removed;

(c) etching the sheet to remove portions of the sheet exposed through openings of the second film, the etching forming an electrically conductive pattern of at least one of the planar heater zones, power supply lines and power return lines; and

(d) removing the second film;

forming a manufactured via layer by:

(a) punching or cutting holes in a polymer film; and

(b) forming conductive vias in the holes;

building a laminate by bonding at least one manufactured component layer and at least one manufactured via layer; and

insulating the laminate by bonding a continuous polymer film onto at least one of upper and lower surfaces of the laminate.

47. The method of claim 46, wherein the sheet is a conductive inorganic film.

48. The method of claim 46, wherein the sheet is a conductive ceramic sheet.

49. The method of claim 36, wherein the ceramic sheets are green sheets and the bonding comprises sintering the green sheets.

50. The method of claim 39, wherein the depositing comprises sputtering, PVD, CVD, PECVD, plasma spraying or electroplating.

51. The method of claim 36, wherein the heating plate includes 100 to 400 planar heater zones, each planar heater zone covers 1 to 15 cm^2 or each planar heater zone covers 16 to 100 cm^2.

52. The method of claim 36, wherein a total area of the planar heater zones is from 50 to 90% of the upper surface of the heating plate.

53. The method of claim 36, further comprising arranging a primary heater layer above or below the planar heater zones, the primary heater layer including one or more primary heaters powered by 100 to 10,000 W and each of the planar heater zones powered by less than 20 W.

54. The method of claim 36, further comprising attaching the heating plate to a cooling plate and connecting the power supply and power return lines to terminal connectors.

55. The method of claim 36, wherein the layers are bonded with adhesive.

56. The method of claim 36, further comprising forming a substrate support assembly by attaching the heating plate and an electrostatic chuck to a lower electrode.

~~21. The substrate support assembly of claim 11, wherein the terminal connectors are spring-tipped passthroughs.~~

~~22. The substrate support assembly of claim 15, wherein the primary heater layer includes two or more heaters.~~

~~23~~57. A method of powering heaters in a substrate support assembly on which a semiconductor substrate is supported, the support assembly ~~comprising~~having an array of heaters powered by two or more power supply lines and two or more power return lines wherein each power supply line is connected to a power supply and at least two of the heaters and each power return line is connected to at least two of the heaters, and a switching device which independently connects each one of the heaters to one of the power supply lines and one of the power return lines so as to provide time-averaged power to each of the heaters by time divisional multiplexing of switches of the switching device, -the method comprising:

supplying power to each of the heaters sequentially using a time-domain multiplexing scheme.

~~24~~58. The method of ~~powering heaters in the substrate support assembly of~~ claim ~~23~~57, wherein only one power supply line is connected to a power supply at the same time.

~~25~~59. The method ~~of powering heaters in the substrate support assembly~~ of claim ~~23~~57,

wherein an average power of each of the heaters is directly proportional to an average duration of time that heater is turned on.

~~26~~60. The method of ~~powering heaters in the substrate support assembly of~~ claim ~~23~~57, wherein the array of heaters are arranged in a grid ~~with the~~, the method further comprising:

connecting heaters in row number N ~~connected to~~with a power supply line number N; and

connecting heaters in column M connected to a power return line number M.

~~27~~61. The method of ~~powering heaters in the substrate support assembly of~~ claim ~~23~~57, ~~wherein~~further comprising:

sequentially connecting each of the power supply lines ~~is connected~~ to a power supply ~~sequentially.~~.

~~28~~62. The method of ~~powering heaters in the substrate support assembly of~~ claim ~~23~~57, ~~wherein~~further comprising:

addressing each heater ~~is addressed~~ at a frequency of at least 1 Hz.

~~29~~63. The method of ~~powering heaters in the substrate support assembly of~~ claim ~~23~~57, wherein:

measuring, via sensors ~~measure~~, parameters ~~which are sent~~ of the substrate and the heaters;

sending the measured parameters to a control and power circuit ~~which adjusts~~; and

adjusting power delivered to the heaters ~~so as~~ to minimize differences between the measured parameters and set targets.

64. The method of claim 57, wherein the substrate support includes a control and power circuit, the method further comprising:

sequentially supply power, via the control and power circuit, to at least 16 heaters.

65. The method of claim 57, wherein at least one primary heater layer is arranged above or below a first electrically insulating layer of a heating plate supporting the heaters, wherein the primary heater layer is electrically insulated from the heaters, the power supply lines, and the power return lines; the primary heater layer includes at least one heater which provides mean temperature control of the semiconductor substrate; the heaters provide radial and azimuthal temperature profile control of the semiconductor substrate, the method comprising:

powering the primary planar heater layer to a predetermined temperature; and

plasma processing the semiconductor substrate at the predetermined temperature.

66. The method of claim 57, further comprising:

(a) loading a semiconductor substrate into the processing chamber and positioning the semiconductor substrate on the substrate support assembly;

(b) determining a temperature profile that compensates for processing conditions affecting critical dimension (CD) uniformity;

(c) heating the semiconductor substrate to conform to the temperature profile using the substrate support assembly;

(d) igniting plasma and processing the semiconductor substrate while controlling the temperature profile by independently controlled heating of the heaters; and

(e) unloading the semiconductor substrate from the processing chamber and repeating steps (a)-(e) with a different semiconductor substrate.

67. The method of claim 66, wherein the processing comprises plasma etching the semiconductor substrate.

68. The method of claim 57, further comprising:

supplying one power supply line with power; and

during the supply of power to the one power supply line:

selecting return lines to be activated; and

connecting a plurality of the selected return lines to a floating reference for identical or different time durations to regulate power supplied to heaters connected to the power supply line and the selected return lines.

~~30~~69. The method ~~of powering heaters in the substrate support assembly~~ of claim ~~23~~57, wherein the heaters are sized such that:

(a) each heater is not larger than four device dies being manufactured on the semiconductor substrate, or

(b) each heater is not larger than two device dies being manufactured on the semiconductor substrate, or

(c) each heater is not larger than one device die being manufactured on the semiconductor substrate, or

(d) the area of each heater is between 2 and 3 square centimeters, or

(e) the heater array includes 100 to 400 planar heaters, or

(f) each heater heats a planar heater zone of 1 to 15 cm^2, or

(g) each heater heats a planar heater zone of 16 to 100 cm^2, or

(h) each heater is scaled with sizes of device dies on the semiconductor substrate and the overall size of the semiconductor substrate.

~~31.~~70. The method of ~~powering heaters in the substrate support assembly of~~ claim ~~23~~57, wherein the total number of the power supply lines and the power return lines is equal to or less than the total number of the heaters.

~~32.~~71. The method ~~of powering heaters in the substrate support assembly~~ of claim ~~23~~57, wherein the heaters are arranged in a rectangular grid, hexagonal grid or concentric rings; and the heaters are separated from each other by gaps at least 1 millimeter in width and at most 10 millimeters in width.

~~33.~~72. The method ~~of powering heaters in the substrate support assembly~~ of claim ~~23~~57, wherein a rectifier is serially connected between each heater and the power supply line

connected thereto, or a rectifier is serially connected between each heater and the power return line connected thereto.

~~34. The method of powering heaters in the substrate support assembly of claim 23, wherein a control and power circuit sequentially supplies power to at least 16 heaters.~~

~~35. The method of powering heaters in the substrate support assembly of claim 23, wherein at least one primary heater layer is arranged above or below a first electrically insulating layer of a heating plate supporting the heaters, wherein the primary heater layer is electrically insulated from the heaters, the power supply lines, and the power return lines; the primary heater layer includes at least one heater which provides mean temperature control of the semiconductor substrate; the heaters provide radial and azimuthal temperature profile control of the semiconductor substrate, the method comprising powering the primary planar heater layer to a predetermined temperature and plasma processing the semiconductor substrate.~~

~~36. The method of powering the heaters in substrate support assembly of claim 23, further comprising:~~

~~(a) loading a semiconductor substrate into the processing chamber and positioning the semiconductor substrate on the substrate support assembly;~~

~~(b) determining a temperature profile that compensates for processing conditions affecting critical dimension (CD) uniformity~~

~~(c) heating the semiconductor substrate to conform to the temperature profile using the substrate support assembly;~~

~~(d) igniting plasma and processing the semiconductor substrate while controlling the temperature profile by independently controlled heating of the heaters;~~

~~(e) unloading the semiconductor substrate from the processing chamber and repeating steps (a)-(e) with a different semiconductor substrate.~~

~~37. The method of powering heaters in the substrate support assembly of claim 36, wherein the processing comprises plasma etching the semiconductor substrate.~~

~~38. The method of powering heaters in the substrate support assembly of claim 23, wherein while one power supply line is supplied power, selecting return lines to be activated and sequentially connecting a plurality of the selected return lines to a floating reference for identical or different time durations to regulate power supplied to heaters connected to the power supply line and the selected return lines.~~

~~39~~73. The method ~~of powering heaters in the substrate support assembly~~ of claim ~~23~~57, wherein the heaters are resistive heaters and the maximum power supplied to the resistive heaters is 20 W.

~~40~~74. The method of ~~powering heaters in the substrate support assembly of~~ claim ~~23~~57, ~~wherein~~further comprising: individually tuning a time averaged heating power of each heater ~~is individually tuned~~ by the time-domain multiplexing.

~~41~~75. The method ~~of powering heaters in the substrate support assembly~~ of claim ~~23~~57, wherein the substrate support assembly includes primary heaters powered with 100 to 10,000 W, the primary heaters located below the array of heaters.

~~42. A semiconductor substrate support for supporting a semiconductor substrate in a plasma processing chamber, comprising:~~

~~an array of heaters operable to tune a spatial temperature profile on the semiconductor substrate, the heaters powered by two or more power supply lines and two or more power return lines wherein each power supply line is connected to at least two of the heaters and each power return line is connected to at least two of the heaters, and~~

~~a switching device which independently supplies power to each one of the heaters via one of the power supply lines and one of the power return lines so as to provide time-averaged power to each of the heaters by time divisional multiplexing of the switches.~~

~~43. The semiconductor substrate support of claim 42, further comprising a temperature controlled and radio frequency (RF) powered base plate beneath the array of heaters and high side circuitry housed in local faraday cage under the base plate.~~

~~44. The semiconductor substrate support of claim 42, further comprising a heating plate having a first electrically insulating layer, the array of heaters arranged in planar heater zones comprising at least first, second, third and fourth planar heater zones, each comprising one or more heater elements, the planar heater zones laterally distributed across the first electrically insulating layer, the power supply lines comprising at least a first electrically conductive power supply line electrically connected to the first and second planar heater zones and a second electrically conductive power supply line electrically connected to the third and fourth planar heater zones and the power return lines comprising at least a first electrically conductive power return line electrically connected to the first and third planar heater zones and a second electrically conductive power return line electrically connected to the second and fourth planar heater zones.~~

~~45. The semiconductor substrate support of claim 42, further comprising temperature sensors which measure parameters sent to a control and power circuit which adjusts power delivered to the heaters so as to minimize differences between the measured parameters and set targets.~~

~~46. The semiconductor substrate support of claim 42, wherein the switching device is connected to an isolator which is connected to electric ground.~~

~~47. The semiconductor substrate support of claim 46, wherein the switching device is located in the plasma processing chamber.~~

~~48. The semiconductor substrate support of claim 46, wherein the isolator is an isolation transformer that isolates the switching device from RF.~~

~~49. The semiconductor substrate support of claim 42, further comprising at least one primary heater layer arranged above or below a first electrically insulating layer of a heating plate supporting the heaters, wherein the primary heater layer is electrically insulated from the heaters, the power supply lines, and the power return lines; the primary heater layer includes at least one primary heater which provides mean temperature control of the semiconductor~~

~~substrate, and the array of heaters provide radial and azimuthal temperature profile control of the semiconductor substrate.~~

~~50. The semiconductor substrate support of claim 48, wherein the switching device is a high side controller and the substrate support further comprises an optical coupler connected to the high side controller for digital communication with a low side controller.~~

~~51. The semiconductor substrate support of claim 42, wherein the switching device connects at least one power return line to a floating reference.~~

~~52. The semiconductor substrate support of claim 42, wherein the switching device turns on a heater when at least one power supply line connected to the heater is connected to a power supply, and at least one power return line connected to the heater is connected to a floating reference.~~

~~53. The semiconductor substrate support of claim 42, wherein the switching device connects all power return lines to a floating reference.~~

~~54. The semiconductor substrate support of claim 42, wherein the switching device addresses each heater at a frequency of at least 1 Hz.~~

~~55. The semiconductor substrate support of claim 42, further comprising sensors configured to measure parameters on different locations on the substrate support and power of the heaters.~~

~~56. The semiconductor substrate support of claim 55, wherein the sensors include at least one of voltage and current sensors.~~

~~57. The semiconductor substrate support of claim 55, wherein the measured parameters include at least temperature measurements.~~