CLAIMS:

1. A method of forming a contact platform (160) for a device substrate (102), the method comprising:

providing a semiconductor device structure (50) having an electrically-conductive contact element (110), a passivation layer (130) atop the electrically-conductive contact element (110), and a recess (432) extending through the passivation layer (130) and terminating at the electrically-conductive contact element (110);

at least partially filling the recess (432) with a resilient material (500);

selectively removing a portion of the resilient material (500) to form a resilient pad (140), the resilient pad (140) overlying the electrically-conductive contact element (110) and spaced apart from the passivation layer (130); and

forming an electrically-conductive platform (160) such that the electrically-conductive platform(160) at least partially surrounds the resilient pad (140).

2. The method of claim 1, further comprising removing excess resilient material (501) from the semiconductor device structure, the excess resilient material (501) overlying the passivation layer.

3. The method of claim 2, wherein the step of removing excess material (501) comprises polishing the semiconductor device structure (50) using the passivation layer (130) as a stop layer.

4. The method of claim 1, further comprising forming an electrically-conductive pillar interconnect (180) overlying and electrically coupled to the electrically-conductive platform (160), the electrically-conductive pillar interconnect (180) having an outer perimeter (184), the outer perimeter (184) entirely overlying the resilient pad (140).

5. The method of claim 1, wherein the step of at least partially filling the recess (432) comprises depositing a polyimide material on the semiconductor device structure (50), the polyimide material at least partially overlying the passivation layer (130).

CLAIMS

1. A semiconductor device comprising a device substrate and an interconnect structure, the interconnect structure comprising:

an electrically-conductive pad formed overlying the device substrate;

an electrically-conductive platform formed overlying the electrically-conductive pad and enclosing a cavity, the electrically-conductive platform having a perimeter portion extending away from the electrically-conductive pad and a capping portion atop the perimeter portion; a cushioning material disposed in the cavity; and

an adhesion layer disposed between the electrically-conductive pad and the perimeter portion, and between the cushioning material and the capping portion.

2. The semiconductor device of claim 1, wherein the adhesion layer is further disposed between the cushioning material and the perimeter portion.

3. The semiconductor device of claim 1, wherein the adhesion layer comprises chromium.

4. The semiconductor device of claim 1, wherein the perimeter portion and the capping portion are integrally formed.

5. A semiconductor device comprising a device substrate and an interconnect structure, the interconnect structure comprising:

an electrically-conductive pad formed overlying the device substrate;

an electrically-conductive platform formed overlying the electrically-conductive pad and enclosing a cavity, the electrically-conductive platform having a perimeter portion extending away from the electrically-conductive pad and a capping portion atop the perimeter portion;

a cushioning material disposed in the cavity; and

an electrically-conductive pillar interconnect formed at least partially overlying, and electrically coupled to, the electrically-conductive platform.

6. The semiconductor device of claim 5, wherein the electrically-conductive pillar interconnect has a cross-sectional perimeter, and the cross-sectional perimeter is disposed entirely overlying the cushioning material.

7. The semiconductor device of claim 1, wherein the cushioning material is adapted to receive a force from the electrically-conductive platform, to elastically deform in response to the force, and to return to an undeformed shape after removal of the force.

8. A semiconductor device structure having a device substrate, the semiconductor device structure comprising:

an electrically-conductive contact pad formed overlying the device substrate;

a resilient block disposed on the contact pad, the resilient block adapted to elastically deform in response to a force;

an electrically-conductive platform substantially surrounding the resilient block, the platform coupled to the resilient block and electrically coupled to the contact pad;

an electrically-conductive pillar interconnect disposed above, and electrically coupled to, the platform, the pillar interconnect extending to a termination end; and

a solder bead formed on the termination end.

9. The semiconductor device structure of claim 8, wherein the resilient block comprises a photo-sensitive polyimide.

10. The semiconductor device structure of claim 8, wherein the electrically-conductive contact pad comprises copper.

11. The semiconductor device structure of claim 8, wherein the electrically-conductive platform comprises copper.

12. The semiconductor device structure of claim 8, wherein the resilient block has a rectangular prismatic shape.

13. The semiconductor device structure of claim 12, wherein the resilient block has a thickness within the range of about 600 to 1000 Angstroms.