

BUS ALIGNED QUADRATURE FM DETECTOR

Frequency Modulation (FM) detection, using a so called quadrature detector, is well known. This kind of FM detector typically is a four quadrant multiplier with one input terminal driven by an amplitude limited FM modulated information signal (reference signal), and another input terminal driven with a version of the reference signal which is quadrature (90°) phase shifted relative to the reference signal using a tuned circuit including an RLC network. With a single tuned circuit, the resultant transfer characteristic of the detector, while closely approximating a straight line near the center (carrier) frequency of the modulated signal, departs from a straight line when the frequency of the FM signal deviates appreciably. Because of the wide deviation of a conventional FM broadcast signal ($\pm 75\text{KHz}$), the departure from a straight line introduces harmonic distortion, particularly for louder audio signals.

The slope of the phase versus frequency curve of the tuned circuit is determined by its "Q". Distortion can be reduced by lowering the "Q" but this reduces the output signal level so that a reduced signal-to-noise (S/N) ratio results. This means that the quadrature FM detector requires a linearity versus sensitivity trade-off between total harmonic distortion (THD) and S/N.

Tolerances in the values of the inductance and capacitance of the tuned circuit can result in a phase versus frequency curve that is not centered at the FM carrier frequency. Although the demodulator will still function under such non-ideal conditions, less of the linear portion of the phase curve will be available and the THD will be degraded. This degradation of THD can be compensated for by lowering the "Q" of the tuned circuit. However, as stated above, the result would be to degrade S/N performance. In order to optimize THD while still maintaining a reasonably high "Q" for good S/N, an alignment of the tuned circuit is desirable so that it is accurately tuned to the FM carrier frequency. Current manufacturing processes and apparatus control systems make it desirable that such an alignment be

performed electronically since the operation of currently produced apparatus, e.g., television receivers and the like, is typically bus controlled under the control of a programmed microprocessor and a PROM memory.

5 Briefly, in a quadrature FM detector, phase detection is performed by multiplication of an amplitude limited FM information signal (reference signal) with a version of the reference signal which has been phase shifted by a phase shifting circuit including a tuned LC circuit. In order to assure that the LC
10 circuit is tuned to the carrier frequency, the LC circuit includes a varactor diode which is tuned by a control voltage generated by a DAC under the control of a programmed computer via a data bus. The control voltage is coupled from the DAC to the varactor diode via the same pin of the integrated circuit to which the LC circuit is
15 coupled to the FM detector.

Fig. 1 shows, partially in block diagram form and partially in schematic form, a quadrature FM detector according to aspects of the present invention.

Fig. 2 is a schematic of the product detector of Fig. 1.

20 Fig. 3 is an alternate embodiment of the product detector of Fig. 2.

Referring to Fig. 1, an FM modulated information signal, which in the exemplary embodiment is the 4.5 MHz (U.S.) intercarrier sound signal of a television receiver, is coupled to
25 input terminal pin 14 of integrated circuit (IC) 12. This FM modulated information signal is amplitude limited by limiter 16 and is coupled, via series capacitor 20 (30 picofards) and shunt resistor 22 (10 Kohms), to an input terminal 52 of a four quadrant product detector 18, which in the exemplary embodiment, is a
30 Gilbert cell. A quadrature signal, which is 90 degree phase shifted with respect to the signal coupled to input terminal 52 (reference signal), is coupled to a second input terminal 50 of detector 18 via a phase shift network of series capacitor 24 (7 picofards), RLC tank circuit 26 coupled between IC terminal pin 42 and ground,
35 series capacitor 28 (50 picofards), and shunt resistor 30 (10

Kohms). A bias voltage is also provided to input terminals 52, 50 via respective resistors 22 and 30.

Tank circuit 26 includes an adjustable inductance (L) 32 in parallel with a fixed capacitance (C) 34. LC circuit 32,34 is a purchased unit manufactured by the Sony Company, part No. 1T363, and is provided in a shielded container 36, which is grounded. In the exemplary embodiment, capacitor 34 is 75 picofarads and inductance 32 is 12 microhenries. This unit is tuned to within 1 percent of 5.3 MHz. Resistor 38 is coupled across LC circuit 32,34, and with an exemplary value of 5 Kohms, provides a circuit "Q" of about 8.5.

Varactor diode 40 is coupled in parallel with LC circuit 32,34 in order to accurately adjust the tuned frequency of tank circuit 26 to 4.5 MHz. Diode 40 is adjustable between 13 and 33 picofarads by a control voltage, generated by DAC 44, which is applied to the anode of diode 40 via isolation resistor 47. In the exemplary embodiment, the adjustment range of diode 40 is limited by the range of control voltages available from DAC 44. When LC circuit 32,34 is used with a varactor diode, the value of capacitor 34 is added to the capacitance of varactor diode 40 and the sum of the two capacitances tunes tank 26 to 4.5 MHz.

The control voltage generated by DAC 44 is coupled to varactor 40 via the same pin 42 used to couple tank 26 to the other members of demodulator 10 disposed on IC 12. The control voltage generated by DAC 44 is responsive to control signals received via bus 46, under the control of a microprocessor or microcomputer (not shown). Each DAC discussed herein is associated with a bus decoder for determining which data is addressed to the particular DAC, and for decoding the bus data into plural data lines for application to the DAC ladder. For simplicity of illustration, the bus decoder for the respective DACs discussed herein is not shown. The bus of the exemplary embodiment is I2C but any applicable bus, such as an IM bus, can be used.

In order to prevent the control voltage across varactor diode 40 from being shunted to ground by inductance 32, a DC

blocking capacitor 48 is connected in series with the LC circuit 32,34 at node 39. For the same reason, resistor 38 is also returned to node 39. However, since the resistance of resistor 38 is much larger than the DC resistance of inductance 32, returning resistor 38 to node 39 is optional, and it may be returned to ground. Additionally, DC blocking capacitor 48 also permits the use of an inductive component which is not intended to pass DC current since the additional magnetic flux due to such a current would have to be taken into account in the design of inductance 32. Thus, the designer has greater flexibility in the choice of components.

When tank circuit 26 is tuned to the carrier frequency of the FM signal, it is resistive at the tuned frequency. In this manner, the signal coupled to terminal 50 via capacitor 24, tank circuit 26, capacitor 28 and resistor 30 is 90 degrees shifted from the reference signal coupled to terminal 52 via capacitor 20 and resistor 22, which add some phase shift to the reference signal path.

The detected output information signal at terminal 58 of product detector 18 is a square wave (train of pulses) at the frequency of the FM carrier but with the duty cycle of the square wave being a function of the frequency deviation of the carrier. The demodulated information signal is recovered from the duty cycle variation by an integrator 60 (low pass network) which can be any suitable active or passive network, and is coupled via amplifier 62 to IC sound output terminal 64.

Referring now to Fig. 2, there is shown a detailed schematic of the Gilbert cell product detector 18 based upon the Gilbert cell product detector described on page 177 of "Solid State Radio Engineering" by Herbert K. Krause et al., published by the Wiley Company, Copyright 1980. For the purposes of Fig. 2, resistors 22a,22b and 30a,30b can be considered equivalents of respective resistors 22, 30 of Fig. 1.

Detector 18 is driven in an unbalanced configuration by unbalanced signals at terminals 50,52. Resistor 72 is coupled between Vcc and the collector electrodes of the transistors 66, 68

which are connected together at node 73. The demodulated output signal at terminal 58 is derived across load resistor 72 and corresponds to the currents flowing through resistor 72. Output level DAC 54, under computer control via bus 46, generates an output level control signal, current I_g , which is coupled to node 73 via terminal 56. In the absence of any signal from DAC 54, current I_c of transistor 66, flowing through resistor 72, determines the amplitude of the demodulated pulse output signal. Transistor 66 is a current sink. As current I_g is provided by DAC 54 to node 73, less signal current is drawn through resistor 72 for the same I_c through transistor 66. Consequently, the voltage drop across resistor 72 is decreased, and the lower level of the output signal square wave at terminal 58 will rise towards V_{cc} . Similarly, the lower level of the output signal square wave will decrease (move further away from V_{cc}) as I_g decreases and a larger percentage of I_c flows through resistor 72. This relationship is described by the following equation, where R_L is resistor 72 and V_o is the voltage at terminal 58:

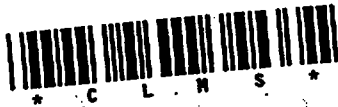
$$V_o = V_{cc} + iR_L \text{ where } i = I_g - I_c \text{ and } |I_c| > |I_g|$$

Thus, the peak level of the output signal square wave at terminal 58 is V_{cc} and the lower level of the output signal square wave is V_{cc} minus V_o . In this manner, the peak-to-peak amplitude of the output signal square wave is adjusted in response to the output current I_g of DAC 54, as determined by the digital data on bus 46.

In an alternate embodiment shown in Fig. 3, the collector-emitter path of a bipolar transistor or the drain-source path of a field effect transistor (FET) is coupled in parallel with load resistor 72. These devices are shown in Fig. 3 as a block member with the numerical designation 76. The control electrode of transistor 76 is coupled to input terminal 56 to receive the control signals from DAC 54. The impedance of parallel circuit 72,76 is adjustable in response to the control signal applied to the control electrode. When the total impedance of the parallel circuit

72,76 is reduced, collector current I_c of transistor 66 will generate a lower voltage across the lower impedance value. Alternately, when the impedance of parallel circuit 72,76 is maximum, i.e., the conduction path of transistor 76 has maximum impedance, the
5 peak-to-peak square wave output voltage generated by the same I_c will be maximum.

Demodulator 10 has a variety of uses, e.g., in FM radios and television receivers including VCRs for demodulating the FM IF sound signal to produce an audio signal, or in VCRs for
10 demodulating the video luminance signal which, in VHS format, is FM recorded onto the tape.



Claims:

1. A demodulator circuit comprising:
first signal means (14,16,20,22) for providing a first
5 signal modulated with information;
second signal means (14,16,24,26,28,30) for providing
a second signal which is phase adjustable with respect to the first
signal by an LC circuit (32,34);
said LC circuit being tunable by a variable impedance
10 (40) responsive to a control voltage to change the phase of the
second signal to a predetermined phase relationship with respect
to said first signal; and
product detector means (18) for providing an output
signal responsive to the phase relationship of said first signal with
15 respect to said second signal, said output signal including
demodulated information.
2. The demodulator circuit of claim 1 wherein:
said LC circuit (32,34) includes a capacitance (34) and
20 an inductance (32) connected in parallel and said variable
impedance is a varactor diode (40) coupled in parallel with said
LC circuit.
3. The demodulator circuit of claim 1 wherein:
25 said product detector means includes a four quadrant
multiplier (18).
4. The demodulator circuit of claim 3 wherein:
said four quadrant multiplier (18) includes a Gilbert
30 cell.
5. The demodulator circuit of claim 3 further
comprising:
a DC blocking capacitor (48) connected in series with
35 said parallel LC circuit.



6. A demodulator circuit comprising:
first signal means (14,16,20,22) for providing a first
signal modulated with information;
control means (44) for generating a control voltage;
5 second signal means (14,16,24,26,28,30) for providing
a second signal which is phase adjustable with respect to said first
signal by an LC circuit (32,34);
said LC circuit (32,34) being tunable by a variable
impedance (40) responsive to said control voltage to change the
10 phase of said second signal to a predetermined phase relationship
with respect to said first signal; and
product detector means (18) for providing an output
signal responsive to the phase relationship of said first signal with
respect to said second signal, said output signal including
15 demodulated information.

7. The demodulator circuit of claim 6 wherein:
said control means (44) generates said control voltage
in response to an electronic programmed means.
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8. The demodulator circuit of claim 6 wherein:
said control means includes a DAC (44).

9. The demodulator circuit of claim 6 wherein:
25 said LC circuit (32,34) is a capacitance and an
inductance (32) wired in a parallel arrangement and the variable
impedance is a varactor diode (40) coupled in parallel with said
LC circuit.

30 10. The demodulator circuit of claim 6 wherein:
the product detector means includes a four quadrant
multiplier (18).

35 11. The demodulator circuit of claim 10 wherein:
said four quadrant multiplier (18) includes a Gilbert
cell.



12. The demodulator circuit of claim 6 wherein:
said second signal is a version of said first signal.

13. A demodulator circuit disposed on an integrated
5 circuit (10), comprising:

first signal means (14,16,20,22) for providing a first
signal modulated with information;

control means (44) disposed on said integrated circuit
for generating a control voltage;

10 second signal means (14,16,24,26,28,30) for providing
a second signal which is phase adjustable with respect to said first
signal by an LC circuit (32,34);

said LC circuit (32,34) being disposed external of said
integrated circuit (10) and coupled to a terminal (42) of said
15 integrated circuit, said LC circuit (32,34) being tunable by an
variable impedance (40) disposed external of said integrated
circuit (10) and coupled to said terminal (42), said variable
impedance (40) being responsive to the control voltage present at
said terminal (42) to change the phase of the second signal to a
20 predetermined phase relationship with respect to said first signal;
and

product detector means (18) for providing an output
signal responsive to the phase relationship of said first signal with
respect to said second signal, said product detector means (18)
25 being disposed on said integrated circuit (10), the output signal
including demodulated information.

14. The demodulator circuit of claim 13 wherein:
said control means (44) generates said control voltage
30 in response to an electronic programmed means.

15. The demodulator circuit of claim 13 wherein:
said control means includes a DAC (44).



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16. The demodulator circuit of claim 13 wherein:
said LC circuit (32,34) is a capacitance (34) and an
inductance (32) coupled in parallel and said variable impedance
includes a varactor diode (40) coupled in parallel with said LC
5 circuit (32,34).

17. The demodulator circuit of claim 13 wherein:
said product detector means includes a four quadrant
multiplier (18).
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18. The demodulator circuit of claim 17 wherein:
said four quadrant multiplier (18) includes a Gilbert
cell.

19. The demodulator circuit of claim 13 wherein:
said second signal is a version of said first signal.
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20. A demodulator circuit comprising:
first signal means (14,16,20,22) for providing a first
20 signal modulated with information;
second signal means (14,16,24,26,28,30) for providing
a second signal which is phase adjustable with respect to the first
signal by an LC circuit comprising an inductance (32) and a
capacitance (34),
25 a DC blocking capacitor (48) connected in series with
the inductance of said LC circuit (32,34), and
product detector means (18) for providing an output
signal responsive to the phase relationship of said first signal with
respect to said second signal, said output signal including
30 demodulated information.

21. The demodulator circuit of claim 20 wherein:
said LC circuit (32,34) is a parallel tuned circuit and
further includes a varactor diode (40) coupled in parallel with
35 said LC circuit and said DC blocking capacitor (48).



22. The demodulator circuit of claim 20 wherein:
said product detector means includes a four quadrant
multiplier (18).

5 23. The demodulator circuit of claim 22 wherein:
said four quadrant multiplier (18) includes a Gilbert
cell.

10 24. The demodulator circuit of claim 20 wherein:
said LC circuit (32,34) is resonant at a frequency of
interest and the impedance of said DC blocking capacitor (48) is
negligible at the frequency of interest.