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PATENT SPECIFICATION

DRAWINGS ATTACHED

L139,352



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Int. Cl.:—H 01 11/14

COMPLETE SPECIFICATION

Process for Making Ohmic Contact to a Semiconductor Substrate

5 We, TEXAS INSTRUMENTS INCORPORATED, a Corporation organised according to the laws of the State of Delaware, United States of America, of 13500 North Central Expressway, Dallas, Texas, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

10 This invention relates generally to semiconductor devices, and more particularly, but not by way of limitation, relates to an improved process for applying expanded metallic contacts to germanium devices having a planar configuration, and to the article of manufacture resulting therefrom.

15 One process heretofore used for making contact to the base region of a planar germanium transistor entails depositing a suitably doped alloy, such as silver-gold-antimony, gold-antimony, or silver-antimony, over the surface of the photo-resist film used to selectively open the base contact windows 20 in the silicon oxide layer. The metal layer is then patterned by suitable photolithographic mask and etch techniques to remove the excess alloy material and leave the alloy only in the contact openings. After the photolithographic masking material has been stripped from the metal film that remains in the openings and from the oxide layer, the metal film and base region are alloyed to produce, upon recrystallization, a heavily 25 doped region to which aluminum or other expanded contact material can be applied.

30 In the above described process, which is generally employed, it will be noted that a vacuum chamber and associated vapor deposition equipment is required to deposit the alloy film, and separate photolithographic

masking and etching equipment is required in addition to that required to deposit and pattern the film which forms the expanded contacts.

45 Another process which is sometimes used to establish good ohmic contact involves evaporating a tin-arsenic alloy onto the oxide layer in which openings have been cut over the base regions and then alloying the tin-arsenic without further processing. The molten tin-arsenic alloy does not penetrate the oxide mask, but does "ball up" and wet the germanium substrate where exposed through the openings in the oxide mask, and 50 leave a heavily doped recrystallization region. The excess tin-arsenic alloy can be removed in acid to leave only the heavily doped recrystallized region formed where the substrate was exposed through the oxide layer. A metallic film is then deposited over the substrate and patterned to form expanded contact tabs which extend through the cuts and make good ohmic contact with the recrystallized regions.

55 Although these prior methods produce suitable semiconductor devices, they are complex procedures which require considerable time and special equipment. This invention is concerned with an improved process for making good ohmic contact with a germanium, silicon, or other semiconductor substrate which can be carried out quickly, simply and economically both with respect to processing time and the equipment required. The process eliminates the need for evaporation equipment and reduces the necessary use of photomask equipment, and several processing steps are eliminated without the addition of any extra steps of significance in the fabrication of a transistor. As a result of the elimination of processing steps, breakage due 60 65 70 75 80

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to handling is reduced. Higher yields have been attained and aluminum expanded contacts can be used without fear that the melting point will be lowered by traces of tin-arsenic which produce difficulties during header mounting, or without fear of increasing the base resistance at bake-out temperatures by reaction with silver-gold-antimony. Further, the invention is adaptable to thin epitaxial collector layer devices because alloying, which tends to reduce the collector-base breakdown voltage by penetrating the base diffusion in a random uncontrolled manner, is avoided.

In accordance with this invention, a metallic film is deposited by a displacement plating process, other than electro-plating, on an exposed surface of the semiconductor substrate e.g. areas exposed by openings cut in an oxide layer previously formed over the substrate surface. The expression "displacement plating process" as used herein refers to a process which is capable of producing a metallic deposit on the surface of a base member by simply immersing the base member in a suitable plating solution without requiring an external electromotive force. It is thereby to be contrasted from electro-plating procedures. The process is chosen such that the surface molecules of the substrate are replaced by metal molecules to form a metallic film in good ohmic contact with the substrate. Such a process may be more specifically termed as a galvanic displacement plating process. By depositing the film only over selected exposed areas of the substrate, the need subsequently to pattern the metallic film deposited by the displacement plating process can be eliminated. A second metallic film, such as aluminum, can then be evaporatively deposited over the entire substrate, including the film areas deposited by displacement plating and patterned to form expanded contacts which are in good ohmic contact with an underlying active region in the substrate through the film deposited by displacement plating.

In accordance with a more specific aspect of the invention, either palladium or platinum is deposited from a dilute, slightly acidic, halide solution as a displacement plating. For example a solution of palladium chloride which has been adjusted to a pH value of approximately 2 with hydrochloric acid, allowed to become saturated at room temperature, diluted to a ratio of 100 to 1 to 300 to 1 and readjusted by the addition of hydrochloric acid to a pH of between 1 and 2 can be used to chemically plate palladium on the exposed surface of a germanium substrate. The reaction is rapid and a metal film of sufficient thickness is attained by immersing the germanium slice in the solution for from 5 to 15 seconds. The palladium is then thoroughly cleaned and baked in a

reducing atmosphere for from one-half to three hours at a temperature of from 400° to 350°C, the period depending upon the temperature, to further decrease the resistance of the contact.

By way of example the invention will be described in greater detail with reference to the accompanying drawings, wherein:

FIGURES 1—3 are schematic cross-sectional views of a transistor in various stages of fabrication which serve to illustrate a process embodying this invention and the resultant product.

Now describing a specific embodiment of the invention in detail, a typical germanium transistor device at an intermediate stage of fabrication is indicated generally by the reference numeral 10 in FIGURE 1. A germanium substrate is comprised of a relatively lightly doped P-type germanium region 12 having a resistivity suitable for the collector region of the transistor, and a more heavily doped P-type region 14 which serves as a low resistivity contact region to which a metallic film will be made ohmic contact. An N-type base region 16 has been diffused into the P-type collector region 12 through a masking frame 18 patterned from deposited silicon oxide to form a collector base junction 20. At the same time, a diffused N-type region 21 is formed around the outer periphery of the masking frame 18, but is of no consequence in the operation of the transistor device. A more heavily doped P-type emitter region 22 is then formed by an alloy process. As illustrated, the excess material from the alloy process has been removed as by etching, although the presence or absence of the excess metal is of no consequence in the present invention. A second silicon oxide film 24 is then deposited over the entire surface of the substrate and is patterned by conventional photolithographic techniques to open base contact windows 26 and 28.

Next, metal films 30 and 32 are selectively deposited by a displacement plating process only on the surface of the base region 16 that is exposed through the openings 26 and 28. This is accomplished by a plating solution comprised of a dilute acidic metal halide solution. For example, a palladium chloride (PdCl_2) solution may be prepared by adjusting the pH value of the solution to approximately 2 with hydrochloric acid and allowing the solution to become saturated at room temperature, then diluting the saturated solution with from 100 parts to 300 parts of water per part of the saturated solution and readjusting the pH of the diluted solution to between 1 and 2 with hydrochloric acid. The substrate is merely dipped into the dilute solution at room temperature and brown metallic palladium films 30 and 32 are deposited on the surface of the germanium substrate that is exposed through the

openings cut in the oxide layer. The grain size of the palladium film is so small that it is cannot be distinguished at 800X magnification. Since the palladium film is formed on the germanium surface due to chemical substitution of palladium for germanium, there is no tendency for the palladium to plate out on the oxide. The substrate is then thoroughly rinsed in deionized water to quench the plating reaction and remove any excess plating solution, and is dried by dipping the substrate successively in pure acetone, then pure trichlorethylene, the remainder of which is evaporated under a dry nitrogen stream.

Next, the substrate is preferably baked in hydrogen, or forming gas, at a temperature substantially below the alloying temperature to decrease the electrical resistance between the palladium films and the base region. It has been found that a baking period of one-half hour at 400°C, or one and one-half to three hours at 370°C is adequate. The reason for the decrease in the resistance of the base contact as a result of baking is not fully understood although it is speculated that either the palladium film tends to sinter slightly, or the arsenic or other doping impurities may tend to concentrate at the surface of the base region to give a more heavily doped surface, either of which would tend to reduce the resistance. An important advantage of the excess is that the baking step may be carried out at the same time, and at the same temperature of course, as the baking steps customarily used to improve the electrical properties of the transistor.

Next, a layer of photo-resist material is formed over the substrate, exposed and developed to open up a window over the emitter region 22. The photo-resist protects the metal films 30 and 32 while the silicon oxide layer 24 is etched to open the window 34 and expose the emitter region 22 as illustrated in FIGURE 2. A metallic film, such as aluminum, is then evaporatively deposited over the substrate, including over the metal films 30 and 32 in the base cuts through the oxide and over the exposed emitter region 22 and is patterned by conventional photolithographic techniques to form expanded base contacts 36 and 38 and an expanded emitter contact 40. A metallic film 42, such as gold-gallium, is also deposited over the opposite side of the substrate to serve as a collector contact.

The palladium does not appear to dope N-type germanium detrimentally at any of the processing temperatures encountered in the manufacture of transistors after the application of the contacts. It is also advantageous that the contacts be baked at 370°C, which is well below the melting point of the aluminum alloy emitter material used in many transistors, in order to prevent any

detrimental reaction between the emitter alloy material and the oxide.

In its broader aspects, the invention is not limited to displacement plating on germanium, but is equally applicable to the selective plating on silicon with appropriate plating solutions. For example, palladium may be plated on silicon using the same solution heretofore described provided a small amount of hydrofluoric acid (HF) is added to the solution to cut through the thin oxide film that always forms on silicon when it is exposed. The quantity of HF required may merely be that required to readjust the pH of the solution after it is diluted.

Further, platinum and most other Group VIII metals, except nickel, iron and cobalt, may be plated on semiconductor material. In addition, silver, gold and some other metals may be plated on semiconductor material in accordance with the present invention, although gold and silver would normally be desirable on silicon rather than on germanium. By the selective displacement plating of a metallic film only upon the substrate and not upon the oxide film, the need for evaporation equipment and photolithographic equipment and solutions is eliminated. A number of process steps are eliminated with only the added step of dipping the substrate for a few seconds into the plating solution, and rinsing and drying the substrate, all of which requires an absolute minimum of equipment and can be accomplished in a relatively short period of time. If desired, the opening 34 over the emitter may be cut at the same time as the openings 26 and 28 over the base and the palladium deposited over the emitter to eliminate another photolithographic step. The baking step is carried out with the hydrogen bake step already required in the manufacture of germanium transistors. Since a number of handling steps are eliminated, the breakage rate is reduced. Further, when the holes in the oxide are badly undercut by the etching solution, the process described has resulted in a much higher yield than when tin-arsenic alloying was used. Aluminum expanded contacts can be used without fear of traces of tin-arsenic lowering the melting point and causing balling during mounting of the wafer on the header, or without fear of an increase in base resistance at bake out temperatures by reaction with silver-gold-antimony. The process is particularly adaptable to the fabrication of semiconductor devices having very thin base layers because any alloying, which is essentially an uncontrolled process insofar as the depth of alloying is concerned, is avoided.

Although preferred embodiments of the invention have been described in detail, it is to be understood that various changes, substitutions and alterations can be made in

the process materials and steps without departing from the scope of the invention as defined by the appended claims.

WHAT WE CLAIM IS:—

5 1. A process for making ohmic contact with a semiconductor substrate having a covering insulating layer thereon with at least one opening providing an exposed surface portion of the substrate, comprising
10 plating by a displacement plating procedure other than electroplating the exposed surface portion only of the substrate through a reaction in which a metallic material is at least initially substituted for the semiconductor
15 material at the exposed surface portion of the substrate to form a thin metallic film over the exposed surface portion of the substrate in ohmic contact with the substrate, with the insulating layer remaining unaffected by the
20 displacement plating so as to be free from any overlying metallic film.

2. A process as set forth in claim 1, wherein the insulating layer covering the semiconductor substrate has a plurality of openings
25 therethrough providing a plurality of exposed surface portions of the substrate, and plating by the displacement plating procedure other than electroplating the plurality of exposed surface portions only of the substrate to form respective thin metallic films
30 over each of the plurality of exposed surface portions of the substrate.

3. A process as set forth in either of claims 1 or 2, wherein the semiconductor substrate is provided with the covering insulating layer by forming an oxide layer over the surface of the semiconductor substrate and selectively removing a portion or portions of the oxide
35 layer to define one or more openings therethrough so as to provide one or more exposed surface portions of the substrate for subsequent plating with metallic material by the displacement plating procedure other than electroplating.
40

4. A process as set forth in any preceding claim, wherein the metallic material is palladium or platinum.

5. A process as set forth in any preceding claim, wherein the semiconductor substrate is
50 germanium or silicon.

6. A process as set forth in any preceding

claim, including the further steps of baking the substrate at an elevated temperature to decrease the electrical resistance between the thin metallic film or films and the substrate, depositing a further metallic film over the insulating layer and the thin metallic film or films, and selectively removing predetermined portions of the further metallic film to leave an expanded contact area or areas in electrical contact with the thin metallic film or films and therefore with the substrate.
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7. A process as set forth in claim 6, wherein the further metallic film is aluminum.
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8. A process as set forth in any preceding claim, wherein the step of plating by the displacement plating procedure other than electroplating is carried out by immersing the substrate with the insulating layer thereon in a dilute acidic solution of a metal halide.
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9. A process as set forth in claim 8, wherein the solution includes a small quantity of hydrofluoric acid.
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10. A process as set forth in claim 6, wherein the baking of the substrate is carried out in a reducing atmosphere at a temperature in the range of 400°C to 350°C for a period of thirty minutes to three hours.
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11. A process as set forth in any preceding claim, wherein the substrate defines the base, emitter and collector regions of a transistor and in which the thin metallic film or films are in ohmic contact with the base region.
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12. A process as set forth in claim 1, substantially as described herein, with reference to the accompanying drawings.

13. A semiconductor substrate treated in accordance with a process as set forth in any preceding claim.
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14. A semiconductor device produced by a process according to any of claims 6, 7 or 10.
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the process materials and steps without departing from the scope of the invention as defined by the appended claims.

WHAT WE CLAIM IS:—

- 5 1. A process for making ohmic contact with a semiconductor substrate having a covering insulating layer thereon with at least one opening providing an exposed surface portion of the substrate, comprising
- 10 plating by a displacement plating procedure other than electroplating the exposed surface portion only of the substrate through a reaction in which a metallic material is at least initially substituted for the semiconductor
- 15 material at the exposed surface portion of the substrate to form a thin metallic film over the exposed surface portion of the substrate in ohmic contact with the substrate, with the insulating layer remaining unaffected by the
- 20 displacement plating so as to be free from any overlying metallic film.
2. A process as set forth in claim 1, wherein the insulating layer covering the semiconductor substrate has a plurality of openings
- 25 therethrough providing a plurality of exposed surface portions of the substrate, and plating by the displacement plating procedure other than electroplating the plurality
- 30 of exposed surface portions only of the substrate to form respective thin metallic films over each of the plurality of exposed surface portions of the substrate.
3. A process as set forth in either of claims
- 35 1 or 2, wherein the semiconductor substrate is provided with the covering insulating layer by forming an oxide layer over the surface of the semiconductor substrate and selectively removing a portion or portions of the oxide
- 40 layer to define one or more openings therethrough so as to provide one or more exposed surface portions of the substrate for subsequent plating with metallic material by the displacement plating procedure other than
- 45 electroplating.
4. A process as set forth in any preceding claim, wherein the metallic material is palladium or platinum.
5. A process as set forth in any preceding
- 50 claim, wherein the semiconductor substrate is germanium or silicon.
6. A process as set forth in any preceding claim, including the further steps of baking the substrate at an elevated temperature
- 55 to decrease the electrical resistance between the thin metallic film or films and the substrate, depositing a further metallic film over the insulating layer and the thin metallic film or films, and selectively removing predetermined portions of the further metallic
- 60 film to leave an expanded contact area or areas in electrical contact with the thin metallic film or films and therefore with the substrate.
7. A process as set forth in claim 6,
- 65 wherein the further metallic film is aluminum.
8. A process as set forth in any preceding claim, wherein the step of plating by the displacement plating procedure other than
- 70 electroplating is carried out by immersing the substrate with the insulating layer thereon in a dilute acidic solution of a metal halide.
9. A process as set forth in claim 8,
- 75 wherein the solution includes a small quantity of hydrofluoric acid.
10. A process as set forth in claim 6,
- 80 wherein the baking of the substrate is carried out in a reducing atmosphere at a temperature in the range of 400°C to 350°C for a period of thirty minutes to three hours.
11. A process as set forth in any preceding claim, wherein the substrate defines the
- 85 base, emitter and collector regions of a transistor and in which the thin metallic film or films are in ohmic contact with the base region.
12. A process as set forth in claim 1, substantially as described herein, with reference to the accompanying drawings.
- 90 13. A semiconductor substrate treated in accordance with a process as set forth in any preceding claim.
14. A semiconductor device produced by a
- 95 process according to any of claims 6, 7 or 10.

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