

SRAM Cell and Methods of Fabrication

[0001] This application claims the benefit of U.S. Provisional Application No. 60/500,426, filed on September 5, 2003, entitled "Novel SRAM Cell and Methods of Fabrication", which application is hereby incorporated herein by reference.

TECHNICAL FIELD

[0002] The present invention relates generally to semiconductor devices, and more particularly to a static random access memory (SRAM) cell and methods of fabrication.

BACKGROUND

[0003] Electronic devices including mobile and portable devices such as cell phones, personal digital assistants (PDA), digital cameras, and combinations thereof, require static random access memory (SRAM) chips with low standby power and low operating power consumption. An SRAM chip may comprise millions of SRAM cells similar to the 6T SRAM cell 100 shown in Figure 1a. Other types of SRAM cells include four transistor (4T) SRAM cells and single transistor (1T) SRAM cells, for example. Shallow trench isolation (STI) structures are commonly used to define the active areas of and to electrically isolate SRAM cells.

[0004] However, undesired recesses known as divots may form directly adjacent transistor active areas in shallow trench isolation structures during the STI manufacturing process. The conventional STI process flow includes pad oxide and silicon nitride (SiN) deposition, active area masking, nitride/oxide etching, silicon (Si) trench etching, liner oxidation, chemical vapor deposition (CVD) oxide filling, chemical mechanical polishing (CMP), and nitride and pad oxide removal. Well known issues in conventional STI processes include divot formation (*i.e.*, oxide

recess, or FOX recesses) along STI edges. The divot at the edge of the STI is formed due to the wet dip of the pad oxide and/or sacrificial oxide by a hydrofluoric acid (HF) solution.

[0005] Figure 1b is an overhead view of the 6T SRAM cell 100 of Figure 1a, showing transistor gate stacks 102 crossing over divots 104 formed along the boundary 106 between active areas 108 and shallow trench isolation (STI) regions 110.

[0006] Figure 1c is a cross-sectional view of the N2 transistor in the 6T SRAM cell 100 corresponding to the reference line X in Figure 1b. Figure 1c shows the gate dielectric 112 and gate electrode 114 deposited with a conformity greater than about 75%. If we do not use the word conformably deposited over divots 104. STI corners 116 in the active region 108 of the N2 transistor experience undesired current leakage. Because the gate dielectric 112 does not completely fill the divots 104, the divots 104 also comprise a portion of the gate electrode 114. The undesired extension of the gate dielectric 112 and gate electrode 114 along the sidewalls of the STI corners 116 may be a source of current leakage. Particularly, the non-planar shape of the gate dielectric 112 and gate electrode 114 at the STI corners 116 produces a concentrated electromagnetic field, thus causing STI corner current leakage. Additionally, the gate dielectric 112 experiences material stress over steps 118 in the divots 104, which may have an undesired effect on transistor power consumption.

SUMMARY OF THE INVENTION

[0007] These and other problems are generally solved or circumvented, and technical advantages are generally achieved, by illustrative embodiments of the present invention, which provide an SRAM cell and methods of fabrication.

[0008] In one aspect, the invention provides for a semiconductor device comprising a substrate. An active region in the substrate comprises a semiconductor material, and an isolation region in the substrate adjacent the active region comprises an insulating material. The active region and isolation region form a surface having a step therein and a dielectric material is formed over the step, the dielectric material having a dielectric constant greater than about 8.

[0009] In another aspect, the invention provides for a memory cell comprising an active region having at least one transistor formed therein. The memory cell also comprises an isolation region adjacent the active region, and a boundary region having a first step. The boundary region is intermediate the active region and the isolation region. The memory cell further comprises a gate dielectric extended over the first step, the gate dielectric comprising a material with a dielectric constant above about 8.

[0010] In yet another aspect, the invention provides for a memory cell comprising a transistor in an active region, the active region comprising a material selected from the group consisting of silicon, germanium, carbon, and combinations thereof. The memory cell also comprises an isolation region adjacent the active region, the isolation region comprising a material selected from the group consisting of silicon nitride, silicon oxide, silicon oxynitride, and combinations thereof. The isolation region further comprises an isolation structure selected from the group consisting of shallow trench isolation structure, mesa isolation structure, local

oxidation of silicon isolation structure, and a combination thereof. The memory cell further comprises a first step, a second step, and a third step. The first step is intermediate the active region and the isolation region, the first step having a first step height of about 400 angstroms. The second step is formed in the active region, the second step having a step height less than about 5000 angstroms. The third step is formed in the isolation region, the third step having a step height less than about 500 angstroms. The memory cell further comprises a gate dielectric overlying the first step, the second step, and the third step. The gate dielectric comprises a material with a relative permittivity above about 8, and the material overlying the first, second and third steps has a conformity above about 75%.

[0011] In yet another aspect, the invention provides for a method of forming an SRAM cell. The method comprises the step of forming an isolation trench in a substrate. The isolation region defines an active region. The method also comprises the step of over-filling the isolation trench with a dielectric material and removing some of the dielectric material, the removing step forming a divot in the remaining dielectric material. The method further comprises forming a transistor in the active region. The transistor includes a gate dielectric that extends over and at least partially fills the divot, the gate dielectric having a relative permittivity greater than about 8. The method still further comprises the steps of forming a gate electrode over the gate dielectric and forming a silicide in the gate electrode.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawing, in which:

[0013] Figure 1a is a schematic view of a six transistor static random access memory (6T SRAM) cell;

[0014] Figure 1b is a layout view of the 6T SRAM cell of Figure 1a, showing only selected layers;

[0015] Figure 1c is a cross-sectional view of a transistor from the 6T SRAM cell of Figure 1b;

[0016] Figures 2a-2e are cross-sectional views illustrating a method of manufacturing the present invention in accordance with a first illustrative embodiment; and

[0017] Figures 3a-3f are cross-sectional views of a step in illustrative embodiments of the present invention.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0018] The making and using of the presently illustrative embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

[0019] Figures 2a–2e are cross-sections illustrating a method of manufacturing in accordance with a first illustrative embodiment of the present invention. The method includes the semiconductor substrate 200 shown in Figure 2a. The semiconductor substrate 200 includes shallow trench isolation (STI) structures 202 in bulk p-type silicon 203, directly adjacent the active region 204. The STI structures 202 have divots 206 directly adjacent corners 208 of the active region 204. The divots 206 have steps 205 with a bottom surface 207 of silicon dioxide and a top surface 209 of a silicon material. For clarity, the divots 206 are shown in an exaggerated scale.

[0020] After the formation of the STI structure 202, the substrate surface 210 is cleaned by nitridation using nitrogen gas (N_2). However, other methods of cleaning the substrate surface 210 in preparation for the high k thin layer deposition include the use of other nitrogen gases including nitrous oxide (N_2O), nitric oxide (NO), and ammonia (NH_3), for example.

[0021] A high k layer of hafnium oxide (HfO_2) 212 with a dielectric constant greater than about 8, is deposited with a conformity greater than about 75% by atomic layer chemical vapor deposition (ALCVD) over the substrate surface 210, as shown in Figure 2b. Details regarding the ALCVD process may be found in a paper by Conley et al. entitled “Preliminary Investigation of Hafnium Oxide Deposited via ALCVD,” Proc. IRW Final Report, pp.11-15, 2001, which is

incorporated herein by reference. In addition to deposition by ALCVD, other illustrative embodiments include high k thin film deposition processes such as metal organic chemical vapor deposition (MOCVD), sub atmosphere chemical vapor deposition (SACVD), and rapid thermal chemical vapor deposition (RTCVD). Still other illustrative embodiments include remote plasma enhanced chemical vapor deposition (RPECVD), low pressure chemical vapor deposition (LPCVD), high density plasma chemical vapor deposition (HDP CVD), and various physical vapor deposition (PVD) processes including evaporation and sputtering.

[0022] It should be noted that materials having a relative permittivity or dielectric constant (k) greater than the dielectric constant of silicon dioxide ($k = 3.9$) are commonly referred to as high k dielectric materials. However, high k dielectric materials in illustrative embodiments of the present invention preferably have a dielectric constant greater than about 8.

[0023] During the ALCVD deposition described above, the HfO_2 gate dielectric material is deposited over the substrate surface with a conformity greater than about 75%. The conformity of the gate dielectric is usually tuned through deposition pressure, temperature and gas flow, for example. Variations in these and other process conditions may vary the conformity of the gate dielectric.

[0024] A layer of polysilicon 214 is deposited over the hafnium oxide 212. Illustrative embodiments of the present invention include forming any material suitable for gate electrode formation over the high k layer 212. Gate electrode materials in other illustrative embodiments include platinum (Pt), tantalum nitride (TaN), titanium nitride (TiN), aluminum, and tungsten for example.

[0025] A selective etch removes portions of the high k gate dielectric layer 212 and the overlying gate electrode 214 layer. Figure 2d is a layout view the first illustrative embodiment

after the selective etch step. Figure 2e shows a cross-section of Figure 2d along line 2e-2e. The hafnium oxide layer 212 and gate electrode layer 214 form a gate stack 216 over the transistor channel 218. Subsequent manufacturing steps, including ion implantation, for example, form a transistor 215. Further metallization steps form a 6T SRAM cell on an SRAM chip.

[0026] The 6T SRAM cell of the first illustrative embodiment has six transistors, all of which have a high k gate dielectric. However, in other illustrative embodiments, only portions of the transistors in the 6T SRAM cell have high k gate dielectrics. For example, high k gate dielectric materials may be limited to the p-type transistors in the 6T SRAM cell, or limited to the n-type transistors in the 6T SRAM cell.

[0027] The transistor 215 in the SRAM cell of the first illustrative embodiment is preferably a metal oxide semiconductor field effect transistors (MOSFETs). Alternatively, the transistor 215 may be another type of transistor such as a strained channel transistor, for example. The strained channel transistor may comprise silicon, carbon, germanium, and combinations thereof, for example.

[0028] The substrate 203 of the first illustrative embodiment includes a bulk silicon substrate. Substrates in other illustrative embodiments of the present invention further include silicon on insulator (SOI) substrates, strained silicon on insulator (SSOI) substrates and strained silicon over relaxed silicon germanium substrates. The relaxed silicon germanium may include a graded silicon germanium layer, for example.

[0029] The dielectric material in the shallow trench isolation structures 202 in the transistor 215 is silicon dioxide (SiO_2). In other illustrative embodiments of the present invention, materials used in the isolation structures of SRAM cells include silicon nitride (Si_3N_4), silicon oxynitride (SiON), boron nitride (BN), and silicon (Si), for example. In some illustrative

embodiments of the present invention, the high k gate dielectric material is also a part of the transistor isolation structure, such as in a local oxidation of silicon isolation structure. In other embodiments, the high k material is the pad oxide and used as a liner in shallow trench isolation structures. In still other embodiments, the isolation material is formed in the recesses of mesa isolation structures.

[0030] Steps 205, highlighted by dotted lines in Figure 2e, are in the divots 206 of the STI structures 202. The steps 205 are formed in an etching process related to the STI manufacturing process. In other illustrative embodiments of the present invention, steps in the substrate may be formed by a selective etch. The selective etch may further comprise a masking step, however, the invention is not so limited. The selective etch may be isotropic or anisotropic. If the selective etch is an anisotropic etch, it may be any type of dry etch. If the selective etch is an isotropic etch, it may be a chemical dry etch or a wet etch. A selective wet etch used to form a step in an illustrative embodiment of the present invention may comprise an etchant with a etch rate (ER) that etches faster on selected regions, *e.g.*, isolation regions. The etchant may comprise hydrofluoric acid (HF), phosphoric acid (H₃PO₄), or combinations thereof, for example. Other embodiments of the present invention require a backside clean step after the wet etch step. However, the backside clean step is not required for the manufacturing of all embodiments.

[0031] The steps 205 in the divots 206 have a bottom surface of silicon dioxide and a top surface of silicon. The illustrative embodiments shown in Figures 3a-3f and described below use various types of steps with various top surfaces, bottom surfaces, and overlying high k gate dielectric layers.

[0032] The illustrative embodiment in Figure 3a shows a step 220 formed, for example, at an STI boundary of an SOI transistor with mesa isolation. The step 220 has a vertical distance

D_{v1} of between about 5 to about 500 angstroms. The top surface 222 of the step is silicon 224 and the bottom surface 226 of the step 220 is silicon oxide 228. A layer of hafnium oxide (HfO_2) 230 formed over the step has a step coverage greater than about 75%.

[0033] The illustrative embodiment in Figure 3b shows a step 232, for example, in an STI divot of a 6T SRAM cell transistor. The step 232 includes the boundary 234 of an insulating material 242 and a semiconductor material 238. The top surface 236 of the step 232 is silicon 238. The top surface 236 is vertically separated (D_{v2}) from the bottom surface 240 by about 200 angstroms. The bottom surface 240 of the step 232 is silicon oxide 242. The high k layer of hafnium oxide 244 is more than 75% conformal to the step 232.

[0034] Figure 3c shows a step 248, for example, in a 1T SRAM cell transistor. The top surface 250 of the step 248 is silicon oxide 252 and the bottom surface 254 of the step 248 is silicon 256. The step height D_{v3} is about between 5 to 100 angstroms. Hafnium oxide 258 formed over the step 248, is more than 75% conformal to the step 248.

[0035] In Figure 3d, the boundary 262 between the active region 264 and the shallow trench isolation (STI) region 266, of an SRAM cell transistor for example, has a step 268. The bottom surface 270 of the step is the surface of the active region 264 comprising a compound of silicon, carbon and germanium. The top surface 274 of the step 268 is the top surface of the STI region 266 comprising silicon dioxide. The step height D_{v4} is about 400 angstroms. A high k gate dielectric layer of hafnium oxide 280 formed over the step 268 has step coverage greater than about 75%.

[0036] In figure 3e, a gate dielectric material of hafnium oxynitride 282 is formed over a step 284 with a conformity greater than about 75% and in an isolation region 286 of a 6T SRAM cell. The top surface 288 and the bottom surface 290 of the step 284 is silicon oxide 286. The

top surface 288 has a vertical distance D_{v5} of about 400 angstroms from the bottom surface 290. The step 284 in Figure 3e has top 288 and bottom 290 surfaces comprising the same dielectric material, however, in other embodiments having a step in an isolation region, the top and bottom steps may comprise different dielectric materials.

[0037] A portion of a 6T SRAM cell transistor shown in Figure 3f has a step 294 in an active region 296. The step 294 has a top surface 298 and bottom surface 300 of the same material. The top surface 298 and bottom surface 300 of the step 294 are active region surfaces comprising silicon 296. The top surface 298 has a vertical distance D_{v6} of about 5000 angstroms from the bottom surface 300. A high k gate dielectric layer of hafnium silicate 302 formed over the step 294 by atomic layer deposition (ALD) has a dielectric constant greater than about 8. In other illustrative embodiments having steps with top and bottom surfaces in an active region, the top and bottom steps are different materials.

[0038] The illustrative embodiments described above have several advantages. The high k dielectric material ($k > 8$) enables better control of the STI corner current leakage in SRAM cell transistors, providing lower standby current and lower power consumption. By providing a gate dielectric with a dielectric constant greater than 8, a thicker gate dielectric may be used in SRAM cell transistors while maintaining the required capacitance between the gate electrode and the underlying transistor channel. A thick layer of high k material minimizes the tunneling current and the out-diffusion of ion implanted dopants from the gate.

[0039] Steps in illustrative embodiments of the present invention have various step heights. Steps that have a vertical distance less than about 400 angstroms, have a top surface of insulating material and a bottom surface of semiconductor material. Other illustrative embodiments of the present invention include steps with a top surface of semiconductor material and a bottom

surface of insulating material. In such embodiments, the step height is preferably less than about 200 angstroms. Steps with a vertical distance less than 500 angstroms preferably have a top and a bottom surface of dielectric material. Steps with a top and a bottom surface of semiconductor material have a vertical distance less than about 5000 angstroms.

[0040] Illustrative embodiments include high k gate dielectric materials that preferably comprise hafnium and zirconium, including zirconium oxide, hafnium oxynitride, and hafnium silicate, for example. Other illustrative embodiments include aluminum oxide, and lanthanum oxide, for example. Illustrative embodiments include the use of combinations of the above mentioned gate dielectric materials, including multi-layered heterogeneous gate dielectrics and gate dielectric alloys comprising zirconium, hafnium, oxygen, nitrogen, lanthanum, and aluminum, for example. Illustrative embodiments of the present invention also include multi-layer gate dielectrics comprising high k dielectric layers and dielectric layers having a dielectric constant lower than about 8.

[0041] Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. As another example, it will be readily understood by those skilled in the art that an SRAM cell may be varied while remaining within the scope of the present invention. Furthermore, the structure and method of manufacturing a high k dielectric material with a permittivity higher than about 8 may be embodied in any semiconductor device and is not limited to steps in a 6T SRAM cell.

[0042] Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means,

methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:
a substrate;
an active region in the substrate, the active region comprising a semiconductor material;
an isolation region in the substrate, adjacent the active region and comprising an insulating material, the active region and isolation region forming a surface having a step therein;
and
a dielectric material formed over the step, the dielectric material having a dielectric constant greater than about 8.
2. The semiconductor device of claim 1 wherein the dielectric material is formed over the step with a conformity of greater than about 75%.
3. The semiconductor device of claim 1 wherein the step is intermediate the active region and the isolation region.
4. The semiconductor device of claim 1 wherein a top surface of the step is the active region and a bottom surface of the step is the isolation region.
5. The semiconductor device of claim 4 wherein the top surface and the bottom surface have a vertical separation in the range of about 5 angstroms to about 500 angstroms.
6. The semiconductor device of claim 4 wherein the top surface and the bottom surface have a vertical separation less than about 600 angstroms.

7. The semiconductor device of claim 1 wherein a top surface of the step is the insulating region and a bottom surface of the step is the active region.
8. The semiconductor device of claim 7 wherein the top surface and the bottom surface have a vertical separation in the range of about 5 to about 600 angstroms.
9. The semiconductor device of claim 1 wherein a top surface of the step and a bottom surface of the step are in the active region.
10. The semiconductor device of claim 1 wherein the active region comprises a material selected from the group consisting essentially of silicon (Si), germanium (Ge), carbon (C), and combinations thereof.
11. The semiconductor device of claim 9 wherein the top surface and the bottom surface have a vertical separation in the range of about 5 to about 5000 angstroms.
12. The semiconductor device of claim 1 wherein a top surface and a bottom surface are in the isolation region.
13. The semiconductor device of claim 12 wherein the top surface of the step and the bottom surface of the step have a vertical separation in the range of about 5 to about 600 angstroms.
14. The semiconductor device of claim 1 wherein the isolation region comprises a material selected from the group consisting essentially of silicon oxide, silicon nitride, silicon oxynitride, boron nitride, and combinations thereof.

15. The semiconductor device of claim 1 wherein the isolation region comprises a shallow trench isolation structure.
16. The semiconductor device of claim 1 wherein the dielectric material is selected from the group consisting of aluminum oxide, hafnium oxide, zirconium oxide, lanthanum oxide, hafnium oxynitride, hafnium silicate, and combinations thereof.
17. The semiconductor device of claim 1 wherein the substrate is selected from the group consisting of silicon on insulator substrate, strained silicon on insulator substrate, relaxed silicon germanium substrate, and combinations thereof.
18. The semiconductor device of claim 1 wherein the dielectric material overlies a portion of the active region to form a transistor gate dielectric.

19. A memory cell comprising:
- an active region having at least one transistor formed therein;
 - an isolation region adjacent the active region;
 - a boundary region having a first step, the boundary region intermediate the active region and the isolation region; and
 - a gate dielectric extending over the first step, the gate dielectric comprising a material with a dielectric constant above about 8.
20. The memory cell of claim 18 wherein the memory cell comprises an SRAM cell.
21. The memory cell of claim 20 wherein the first step has a step height less than about 600 angstroms.
22. The memory cell of claim 20 wherein the active region comprises a material selected from the group consisting of silicon, germanium, carbon, and combinations thereof.
23. The memory cell of claim 20 wherein the isolation region comprises a material selected from the group consisting of silicon nitride, silicon oxide, silicon oxynitride, and combinations thereof.
24. The memory cell of claim 20 wherein the isolation region comprises an isolation structure selected from the group consisting of shallow trench isolation structure, mesa isolation structure, local oxidation of silicon structure, and combinations thereof.

25. The memory cell of claim 20 wherein the active region further comprises a second step, the second step height having a height less than about 5000 angstroms, and the gate dielectric formed over the second step with a conformity above about 75%.
26. The memory cell of claim 20 wherein the isolation region comprises a second step, the second step having a height less than about 600 angstroms, and the gate dielectric formed over the second step with a conformity above about 75%.
27. The memory cell of claim 20 wherein the gate dielectric covers the first step with a conformity above about 75%.

28. A memory cell comprising:

a first n-type transistor having a source connected to a first bit line, having a drain connected to a first node, and having a gate connected to a word line;

a second n-type transistor having a source connected to a second bit line, having a drain connected to a second node, and having a gate connected to the word line;

a third n-type transistor having a source connected to a grounded wire, having a drain connected to the first node, and having a gate connected to the second node;

a fourth n-type transistor having a source connected to the grounded wire, having a drain connected to the second node, and having a gate connected to the first node;

a first p-type transistor having a source connected to a voltage supply, having a gate connected to the second node, and having a drain connected to the first node;

a second p-type transistor having a source connected to the voltage supply, having a gate connected to the first node, and having a drain connected to the second node; and

wherein at least one of the transistors has a gate dielectric overlying a step in a divot interposed between an active region of the transistor and an isolation region adjacent the transistor active region, the gate dielectric comprising a material with a dielectric constant greater than about 8, the gate dielectric conforming to the step with a conformity above about 75%.

29. A method of forming an SRAM cell, comprising the steps of:
- forming an isolation region in a substrate, the isolation region surrounding an active region;
 - over-filling the isolation region with a dielectric material;
 - removing some of the dielectric material, the removing step forming a divot in the remaining dielectric material, the divot comprising a first step, the first step having a first top surface and a first bottom surface;
 - forming a transistor in the active region, the transistor including a gate dielectric that extends over and at least partially fills the divot, the gate dielectric having a relative permittivity greater than about 8;
 - forming a gate electrode over the gate dielectric; and
 - forming a silicide in the gate electrode.
30. The method of claim 29 wherein the silicide is selected from the group consisting of cobalt silicide, nickel silicide, platinum silicide, titanium silicide, erbium silicide, and combinations thereof.
31. The method of claim 29 wherein the dielectric material is selected from the group consisting of aluminum oxide, hafnium oxide, zirconium oxide, lanthanum oxide, hafnium oxynitride, hafnium silicate, and combinations thereof.
32. The method of claim 29, further comprising the step of forming the gate dielectric over a second step in the isolation region.

33. The method of claim 32 wherein a second top surface and a second bottom surface of the second step comprise materials selected from the group consisting of silicon, silicon oxide, silicon nitride, silicon oxynitride, and combinations thereof.
34. The method of claim 33 wherein the vertical separation between the top surface and the bottom surface is less than about 600 angstroms.
35. The method of claim 29, further comprising the step of forming the gate dielectric over a second step in the active region.
36. The method of claim 35 wherein the second step comprises a second top surface and a second bottom surface, the second top surface and the second bottom surface comprising materials selected from the group consisting of silicon, carbon, germanium, and combinations thereof.
37. The method of claim 36 wherein the top surface and the bottom surface have a vertical separation of less than about 600 angstroms.
38. The method of claim 29 wherein the top surface and the bottom surface have a vertical separation of less than about 600 angstroms.
39. The method of claim 29 wherein the top surface and the bottom surface have a vertical separation of less than about 400 angstroms.
40. The method of claim 29 wherein the isolation region confines the active region.

41. The method of claim 29 wherein the isolation region comprises a material selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride, and combinations thereof.
42. The method of claim 29 wherein the isolation region has an isolation structure selected from the group consisting of shallow trench isolation structure, mesa isolation structure, local oxidation of silicon (LOCOS) isolation structure, and combinations thereof.
43. The method of claim 29 wherein the gate dielectric is formed by a deposition process selected from a list consisting of atomic layer deposition, physical vapor deposition, chemical vapor deposition, and combinations thereof.
44. The method of claim 43 wherein the method of chemical vapor deposition is selected from a group consisting of metalorganic chemical vapor deposition, pulsed injection MOCVD, rapid thermal chemical vapor deposition, remote plasma enhanced chemical vapor deposition, low pressure chemical vapor deposition, high density plasma chemical vapor deposition, and combinations thereof.
45. The method of claim 29 wherein the gate dielectric has a conformity to an underlying surface of greater than about 75%.
46. The method of claim 29 wherein the steps are formed by selective etch.
47. The method of claim 46 wherein the selective etch is selected from the group consisting of isotropic etch and anisotropic etch.
48. The method of claim 47 wherein the selective etch is an isotropic wet etch.

49. The method of claim 48 wherein the selective isotropic wet etch includes an etchant with a faster etch rate on selected regions.
50. The method of claim 49 wherein the etchant contains hydrofluoric acid or phosphoric acid.
51. The method of claim 49 wherein the selected regions are isolation regions.
52. The method of claim 47 wherein the selective etch is an isotropic chemical dry etch.
53. The method of claim 47 wherein the selective etch is an anisotropic dry etch.
54. The method of claim 46 wherein the selective etch further comprises a masking step.
55. The method of claim 29 wherein the substrate further comprises a material selected from the group consisting of silicon (Si), germanium (Ge), carbon (C), and combinations thereof.
56. The method of claim 29 wherein the substrate is selected from the group consisting of silicon-on-insulator substrate, strained silicon-on-insulator substrate, strained silicon on relaxed silicon germanium (SiGe) substrate, and combinations thereof.