

DEVICE, DESIGN AND METHOD FOR A SLOT IN A CONDUCTIVE AREA

Background of Invention

1) Field of the Invention

This invention relates in general to semiconductor devices, methods for designing semiconductor devices, masks and mask designs, and more particularly, to semiconductor designs, methods and devices with slots in active areas.

2) Description of the Prior Art

Semiconductor integrated circuits and printed circuit electronic packages are generally structures comprised of several layers of conducting, insulating and other materials that are structured in the horizontal dimension by fabrication processes that transfer patterns defined in physical designs or layouts. A layout consists of a set of planar geometric shapes in several layers. These physical designs or layouts are typically represented as computer data consisting of two dimensional shapes in a hierarchical data structure that exploit the repetitive structure usually found in such circuits and packages. The design or layout files are then converted into pattern generator files that are used to produce patterns called masks.

In some cases, the action of the fabrication process is affected by the design patterns being transferred to the physical materials. For example, the local pattern

1 density of the design, i.e., the fraction of area over which material is deposited (or
2 removed) can affect the shapes and dimensions of features, with the "locality extent"
3 dependent on the specific fabrication process. A special process that may be affected by
4 local pattern density is chemical-mechanical (so called "chemech") polishing (CMP). CMP
5 is used to planarize semiconductor substrates. Planarization is becoming more and more
6 important as the numbers of layers used to form a semiconductor device increases.
7 Nonplanar substrates show many problems including difficulties in patterning a photoresist
8 layer, formation of a void within a film during film deposition, and incomplete removal of
9 a layer during an etch process leaving residual portions of the layer.

10 However, CMP has the disadvantage of showing so called "dishing"
11 when polishing areas of wide metal. Especially in case copper is used this effect will result
12 in nonplanar surfaces of the substrate, leading to the difficulties mentioned above.

13 FIG. 1 shows two situations where dishing occurs. Within smaller wires
14 (A) dishing can be neglected to a certain degree, whereas for wide wires (B) it shows big
15 impact on the metal's resistance and on the manufacturability.

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17 The importance of overcoming the various deficiencies noted above is
18 evidenced by the extensive technological development directed to the subject, as
19 documented by the relevant patent and technical literature. The closest and apparently
20 more relevant technical developments in the patent literature can be gleaned by considering
21 US 5,602,423(Jain) that shows a metal line inlaid with slots or pillars.

22 US 6,403,389b1(Chang et al.) shows a method for forming slots in
23 conductors to prevent dishing during chemical-mechanical polish.

24 US 6,495,907b1(Jain et al.) shows a conductor reticulation and process.

25 US 5,671,152(Lavin et al.) shows a method for generating negative fill
26 shapes for metal lines.

27 US 6,319,818b1(Stamper) shows a method to add holes to metal lines
28 to improve CMP planarization.

1 US 6,094,812(English et al.) shows a method to split up metal lines.

2 US 5,923,563(Lavin et al.) shows a method to add fill shapes.

3 US 2002/0199162A1(Ramaswamy et al.) 12/15/2002 discloses a

4 method for a fill pattern.

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6 US 6,396,158B1(Travis) shows a method for designing dummy feature
7 in a mask layout.

8 US 6,081,272(Morimoto et al.) shows a method of sizing and position
9 dummy structures.

10 Andrew B. Kahng et al., "Filling and Slotting: Analysis and
11 Algorithms", ISPD 98 Monterey CA USA, pp. 95-102.

12 However, these designs, methods and device can be improved upon.

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Summary of the Invention

It is an object of embodiments of present invention to provide a method for fabricating a device layout or design that has slots.

It is an object of embodiments of present invention to provide a structure and method for fabricating a mask that has slots.

It is an object of embodiments of present invention to provide a structure and method for fabricating a semiconductor device that has slots in conductive areas.

It is an object of embodiments of the present invention to provide a method to design masks for integrated circuits having slots.

It is therefore an object of embodiments of the present invention to provide an effective method to design semiconductor integrated circuits or electronic packages that solves the dishing problem associated with the CMP process.

It is another object of the invention to provide such a method for designing slots in conductive areas without increasing the data complexity significantly.

The embodiments of the present invention provides a method for determining the placement of slots representations in a layout of an integrated circuit design; the layout comprised of a plurality of conductive layer representations; the conductive layer representation comprised of conductive region representations; at least one the conductive region representation has a via contact representation between adjacent active layers;

the method comprising the steps of:

setting a reference for the placement of the slot representations with respect to the layout;

1 setting the minimum dimensions of the conductive region
2 representations in which the slot representations are placed;
3 setting the dimensions of the slot representations;
4 setting the spacing between slot representations in conductive layer
5 representations;
6 setting the clearance between the slot representations on adjacent
7 conductive layer representations;
8 setting the stagger spacing between rows of adjacent slot
9 representations in conductive layer representations;
10 setting the minimum distance from the edge of the slot representations
11 to the edge of the conductive region representations;
12 setting the minimum distance between the contact via representation
13 and the slot representation.
14 A preferred embodiment of the method comprises the steps of :
15 providing a layout comprised of a plurality of active layers;
16 the active layers comprised of active regions;
17 at least one the active regions has a via contact feature between adjacent
18 active layers;
19 determining the placement of square slots in the layout by the
20 following:
21 (reference) setting a reference for the placement of the square slots
22 feature with respect to the layout;
23 (MS1) setting the minimum dimensions of the active regions in which
24 the square slots features are inserted in to a minimum length of about 12 μm and a
25 minimum width of about 12 μm ;
26 (MS2) setting the dimensions of the square slot features are about 2 μm
27 by about 2 μm ;

1 (MS3) setting the minimum spacing between the square slots features
2 on the same active region to about 4 μm ;

3 (MS4) setting the minimum clearance between the square slots features
4 on adjacent active layers to about 1 μm ;

5 (MS5) setting the stagger spacing between rows of adjacent square slot
6 features in the same active area to about 0 μm ;

7 (MS 6) (edge exclusion) setting the minimum distance from the edge
8 of the square slot features to the edge of the active region to about 1 μm ;

9 (MS 7) setting the minimum distance between the contact via feature
10 and the square slot feature to about 1 μm .

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12 Another example embodiment is a semiconductor device comprising:
13 a plurality metal layers over a substrate; the metal layers comprised of metal areas; via
14 contacts between the metal layers; square slots in the metal areas; the square slots are
15 substantially square;

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17 the square slots positioned as follows:

18 the square slots placed with respect to a reference point;

19 the square slots positioned only in metal areas with dimensions greater
20 than a minimum metal area dimensions;

21 a spacing between the square slots on a single metal area;

22 a stagger spacing between rows of adjacent square slots in the same
23 metal layer;

24 a clearance between the square slots on adjacent metal layers;

25 a minimum distance from the edge of the square slots to the edge of the
26 metal areas;

27 a minimum distance between the contact via and the square slots.

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1 Additional preferred embodiments are set forth in the claims. This
2 summary does not limit the interpretation of the claims.

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4 Additional objects and advantages of the invention will be set forth in
5 the description that follows, and in part will be obvious from the description, or may be
6 learned by practice of the invention. The objects and advantages of the invention may be
7 realized and obtained by means of instrumentalities and combinations particularly pointed
8 out in the append claims.

Brief Description of the Drawings

The features and advantages of a semiconductor device according to the present invention and further details of a process of fabricating such a semiconductor device in accordance with the present invention will be more clearly understood from the following description taken in conjunction with the accompanying drawings in which like reference numerals designate similar or corresponding elements, regions and portions and in which:

Figure 1 shows a cross sectional view of the dishing problem according to the prior art.

Figure 2 is a flow chart for a method for a layout for positioning square slots in conductive area according to a preferred embodiment.

Figure 3A shows a metal layer and a generated slot prior to a “not” operation.

Figure 3B shows the metal pattern and slot after a “not operation “. The metal layer is represented by a metal GDS layer; and the slots have the same GDS layer, but a different data type according to a preferred embodiment.

Figure 4A shows a top down view of a layout or of a chip having slots in conductive areas according to embodiments of the invention.

Figure 4B shows a top down view of a layout or of a chip having slots in conductive areas and shows dashed slots 457 that are not included.

Figure 4C shows a table of preferred slot sizes as a function of spacing between the odd and even layers (Y) and slot spacing $*(2Y+X)$ according to a preferred embodiment of the invention.

Figure 4D shows the spacing X and Y in relationship to the square slots as shown in Figure 4C.

Figure 5A shows a top plan view of a two layers of a layout or actual conductive areas and slots according to a example embodiment.

1 Figure 5B shows a top plan view of a three layers of a layout or actual
2 conductive areas and slots according to a example embodiment.

3 Figure 6A shows a top plan view of a two layers of a layout or device
4 according to a example embodiment.

5 Figures 6B, 6C, 6D and 6E are cross sectional views take along axis 6B
6 in Figure 6A of a device according to a example embodiment.

7 Figure 7A is a top plan view of a layout that shows an unstaggered
8 arrangement of slots according to a example embodiment.

9 Figure 7B is a top plan view of a layout that shows a staggered
10 arrangement of slots.

11 Figure 8 is a top plan view of a 2 layers of a layout or metal area
12 showing the arrangement of slot according to a example embodiment.

13 Figures 9A, 9B and 9C are cross sectional views of a layout or device
14 having different material filling the slots. Figures 9A, 9B and 9C represent a view taken
15 along axis 6B in figure 6A.

16 Figure 10 is a diagram of a computer system upon which an
17 embodiment of the invention can be implemented.

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Detailed Description of the Preferred Embodiments

I. Overview

In the following discussion, certain conventions and definitions will be used to simplify the description and facilitate understanding of the embodiments. For example, much of the description will describe the placement of symmetric shaped (e.g., square) slots in conductive areas, however, it is to be understood that in some embodiments of the invention, the placement occurs mathematically on computer models and layouts of IC devices rather than on a physical metal line.

Embodiments of the present invention are devices, designs and method of determining the placement of square slots in “wide” active regions (e.g., metal lines). Embodiments including square slots inside selected wide metal lines, by adhering to a set of guidelines /rules/steps. There guidelines are described below.

The method of designing slots in active regions reduces the complexity of slot placement, and improves design turnaround time. The slots can improve the planarization of metal areas (e.g., lines) and insulators by reducing depressions (e.g., dishing) in the metal areas.

Figure 2 shows a flow chart outlining preferred steps of an embodiment for placing square slots in metal areas.

II. Terminology

layout – design of device, such as integrated circuit

slot – space in a conductive area. The slot can be filled with dielectric material or conductive material or let a void.

slot region – material filling a slot.

slot feature – representation of a slot in a design of a device or mask design for the device

square slot – a substantially square slot

1 active layers – representation of conductive layers of a device. Can represent metal layers,
2 such as M1, M2, etc to top metal layers in a device. Metal layers can be copper dual
3 damascene layers.
4 active regions – representations of conductive regions of a device. For example, can
5 represent metal lines, metal pads, capacitor plates, resistors, etc.
6 interconnect layers or conductive layer or metal layers- are conductors used in connecting
7 circuit elements of an integrated circuit.

8 **III. Slot placement and method for design**

9 An embodiment of the invention is an method that produces a layout
10 design for an integrated circuit or one of more active layers (e.g., metal layers) for the
11 integrated circuit with symmetric shaped slots in wide active layers. Preferred
12 embodiments provide for square slots in wide dual damascene lines. The slots reduce the
13 dishing in the active area (e.g., Cu lines) during chemical-mechanical polishing (CMP).

14 **A. layout is comprised of a plurality of active layers**

15 A layout or representation of a IC design of one or more layers of an IC
16 design is produced. The layout can be a computer data representation including active
17 layer (e.g., metal layers or metal Levels (e.g., M1, M2). The active layers are
18 representations that correspond to designed circuitry for a semiconductor device. The
19 active layer can include portions of conductive lines (e.g., metal lines), capacitors,
20 resistors, and power supplies.

21 The embodiments are especially applicable to 0.13 μ m and 0.9 μ m
22 groundrule technology. (e.g., minimum line-width geometries of 0.13-micron or 90
23 Nanometer)).

24 The embodiments can be used to place slots in dummy features or any
25 “inactive metal areas” (e.g., dummy areas, test structures, etc). However it is possible to
26 use the embodiments to place slots in resistors, capacitors, and inductors, although it may
27 not be advantageous to do so.

1 The embodiments could also be used to place slots be used in metal
2 area in packaging and printed circuit boards and other technologies with wide metal lines
3 or areas.

4 Preferably the layout is in format of an electronic graphic database file
5 of layout shapes, such as a GDSII data stream. The layout may be a standard layout
6 database file exchange format such as GDS, GDSII, DXF, CIF, IGES, a flat file, or even a
7 proprietary database file format. However, any data file format that defines the geometry
8 of a layout could be used.

9 As shown in figure 3A, the input GDSII data will contain drawn active
10 areas (e.g., metal lines or patterns representations) with or without drawn slots in any
11 GDSII number and data type.

12 Embodiments (e.g., a program) will generate slots (e.g., squares or
13 symmetric shapes) which will be used to "NOT" out slots in that metal layer. Figure 3B
14 shows an example of the line and slot after the "NOT" operation. This slotted metal will
15 then be the final metal used as output GDSSII file. The metal layer and slot can have the
16 same metal GDS layer: but different data types. For example, the metal layer can be Metal
17 GDS layer: data type "0". The slot can be the same GDS layer; data type "8".

18 The shape of the slot is preferably symmetric (along one or two axis)

19 **B. active layers are comprised of active regions**

20 The active layers can represent conductive layers or levels (e.g., M2)
21 such as metal layers or levels. The active layers are comprised of active regions. Active
22 regions can represent conductive lines (such as metal lines), pads, and devices such as
23 capacitor plates, resistors. In a preferred embodiment, the active layer represents a metal
24 layer.

25 **C. a via contact feature between adjacent active layers**

26 At least one the active regions has a via contact feature between
27 adjacent active layers. The via contact feature represents via contacts between metal levels.

1 The via contact features can represent interconnects, such as damascene or dual damascene
2 interconnects. The via contact feature represents via contacts between metal levels. The via
3 contact features can represent interconnect, such as dual damascene interconnects. The via
4 contact features can represent to bottom via contact portion of dual damascene
5 interconnect.

6 ***D. Flow chart***

7 The placement of square slots in the layout can be determined by
8 applying the placement rules. A flowchart of an embodiment is shown in figure 2. A slot
9 will not be place where all the rules can not be met.

10 ***E. setting a reference***

11 A reference (point) is set for the placement of the square slots features
12 with respect to the layout. For example, as shown in figure 4A, the reference point 401 is
13 shown in the bottom left corner of the layout 400. Figure 4A shows a top down view of a
14 representation of a layer (e.g., level). Figure 4A shows metal areas and slots in the metal
15 areas.

16 The outline 400 can represent the outside edge of a chip. The metal
17 areas and chip are not drawn to scale.

18
19 As shown in figure 4A, the square slots are orientated in relation to the
20 reference point 401 which is, for example, in this case at the bottom left of the chip corner.
21 For example, Figure 4A shows the slots 404 406 orientated so that the minimum clearance
22 distances (EE) are to the bottom and left sides of the active region (e.g., metal area) 402.
23 Likewise, Figure 4A shows the slots 442 444 orientated so that the minimum clearance
24 distances (EE) are to the bottom and left sides of the metal area 440. For example, the
25 slots have the minimum edge exclusion (EE) (of 1 μm) on the bottom and left sides of the
26 metal areas. The minimum edge exclusion (EE) is the minimum distance from the slot to
27 the edge of the metal area. (See further explanation below).

1 As shown in figure 4A, the slots are spaced 410 412 452 at least the
2 minimum edge exclusion (EE) distance from the edges of the active areas 402 440 on the
3 top and right sides of the active areas 402 440.

4 Figure 4B is similar to Figure 4A, but Figure 4B shows the dotted line
5 slots 457 that are examples of slots that are not drawn because they fall outside the metal,
6 do not meet the rules and will not be placed

7 **F. (MS1) slots inserted in wide metal lines**

8 The symmetrical or square slots are preferably included in active
9 regions (e.g., metal lines) which are larger than minimum dimensions (See figure 2, step
10 201). Preferably the (square) slots are included in active regions larger than about 12 μm
11 by 12 μm or 144 μm^2 . That is the slots are placed in active regions with a length greater
12 than about 12 μm and a width greater than about 12 μm . Note that most metal patterns are
13 rectangular shaped because it is easier to design layouts. However, the invention is
14 suitable were metal patterns that have other shapes. The determining the minimum active
15 region dimensions in accordance with effects of dishing on the metal lines due to chemical
16 mechanical polishing. The inventors have found that the choice of the 12 μm by 12 μm
17 minimum dimension significantly reduces dishing problems by chemical-mechanical
18 polishing (CMP) and reduces data processing load in slot design. The slots are preferably
19 included in substantially all of the in active regions on a chip (or layout of a chip) (e.g.,
20 metal lines) which are larger than minimum dimensions

21 For example, as shown in figure 4A, slots 404 406 are placed in active
22 region (e.g., metal area) 402 which has a length and width greater than the minimum
23 dimensions.

24 The slots are preferably shaped to minimize the effects on current flow
25 and resistance in the conductive areas. In contrast, to rectangles that have a high resistance
26 to current flow along the longer side. The most preferred slot shape is square.

1 In addition, in embodiments where square shaped slots are discussed,
2 other shaped slots are feasible and the embodiments are not limited to square slots. For
3 example, slots with symmetric shapes, especially in the direction of current flow are
4 feasible. Acceptable shapes include, substantially square slots, circular slots, polygons
5 such as hexagons, pentagons, etc. Preferred shapes are symmetrically around a point, have
6 equal length sides (or arcs) (e.g., square, hexagon, octagon) and have an even number of
7 sides.

8 Square shaped slots have advantages that they can be easily generated
9 and arrayed and make the file size smaller. Square slots can be arranged so they are also
10 independent of current direction. (as opposed to rectangular slots that block current more in
11 the direction against the longer side). Square slots reduce the number of design rules. For
12 example, slot density need not be checked because it is uniformly distributed in the wide
13 metal area. However, the design rules are needed to be changed when converting from
14 rectangular slots to square slots.

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16 **G. (MS2) setting the dimensions of the slot features**

17 The slots are preferably substantially square. The dimensions of the
18 square slot features are set at a length between 0.5 μm and 4 μm and most preferably about
19 2 μm and a width between 0.5 μm and 4 μm and most preferably about by about 2 μm .

20 Figure 4C shows a table of preferred slot sizes as a function of spacing
21 between the odd and even layers (Y) and slot spacing $\ast(2Y+X)$. Figure 4D shows the
22 spacing X and Y in relationship to the square slots.

23 The depth of the square slots is preferably the thickness of the active
24 regions or metal area which surrounds the slot.

25 Referring to figure 4, the length and width 454 456 of square slot 442 is
26 preferably about 2 μm .

1 The inventors chose this square slot dimension in combination with the
2 other guidelines (physical and design) based on the electrical structures obtained.

3 The slots are preferably a shape that has a symmetry such that
4 minimizes the affect current flow. For example, the slots preferably have square shapes,
5 circular shapes, or symmetric polygons, etc. For example, rectangles with the length
6 significantly longer than the width are preferred between of the effect on current flow.

7 **H. (MS3) setting the minimum/max spacing between the slots**
8 **features**

9 Referring to figure 2, step 203, the (minimum/max) spacing between
10 the square slots features on the same active region (e.g., metal area) is preferably between
11 1.5 μm to 8 μm and more preferably about 4 μm . See Figure 3C for a table of preferred
12 values.

13 Referring to figure 4A, the spacing (SS – Slot spacing) between the
14 square slots features 404 406 on the same active region (e.g., metal area) 402 is about 4
15 μm .

16 **I. (MS4) setting the clearance between the square slots**
17 **features on adjacent active layers to about 1 μm ;**

18 Referring to figure 2, step 204, the (minimum/max) clearance between
19 the square slots features on adjacent active layers is set to from about 0.5 μm to 2 μm and
20 more preferably about 1 μm .

21 Figure 5A shows a top down view of at least two active layers (e.g.,
22 metal lines) 502 that can represent odd or even (metal) adjacent layers over a substrate. For
23 example, M1 is adjacent to M2 layer. The odd layer(s) have square slot features 506 508
24 that are spaced apart by the slot spacing SS of about 4 μm . The even active layers have
25 slot 510. There can be one or more odd or even layers.

The slots 506 508 on an even layer are spaced from the Slots 510 in the odd layers by the clearance SC (slot clearance) of about from about 0.5 μm to 2 μm to more preferably about 1 μm . See figure 4C for a table of preferred values (e.g., Y).

Figure 5B further illustrate this clearance rule between slots on adjacent layers. Figure 5B shows metal areas (or representations of metal areas) in three metal layers 530 540 550, such as the first three metal layers (e.g., M1, M2 and M3; or ML, ML+1, ML+2) above the substrate.

Active region 530 has slots 532 534. The slots 532 534 have a slot clearance (SC) 538 539 of about 1 μm from the slot 546 (536 is the projection of slot 546 on area 530) on the adjacent or neighboring (e.g., metal) active layer. For example the slot clearances 538 and 539 are at least 1 μm .

Active region 540 has slot 546. The slots 532 534 have a slot clearance (SC) 548 549 of at about 1 μm from the slot 534 532 (544 542 is the projection of slots 534 532 and 554 552 on area 530) on the adjacent or neighboring layer. For example the slot clearances 548 and 549 are at least 1 μm .

Active region 550 has slots 552 554. The slots 552 554 have a slot clearance 553 551 of at about 1 μm from the slot 546 (556 is the projection of slot 546 on area 550) on the adjacent or neighboring layer. For example the slot clearances 551 553 are at about 1 μm .

J. (MS5) setting the stagger spacing between rows of adjacent square slot features

The stagger spacing between rows of adjacent square slot features in the same active area is between 0 and 4 μm and most preferably about 0 μm . See figure 2, step 205.

As shown in figure 7A, for example, the rows and columns of square slots 704 are not staggered (e.g., stagger spacing = 0) in the active area (e.g., metal area)

1 702. The setting of the stagger spacing to about 0 μm results in a simplification of the
2 method and program.

3 In contrast to the embodiment in figure 7A, referring the 7B, the rows of
4 slots 754 are staggered in the active area 752.

5 **K. (MS 6) (edge exclusion) setting the minimum distance from**
6 **the edge of the square slot features to the edge of the active**
7 **regions**

8 The minimum distance from the edge of the square slot features to the
9 edge of the active region is about 0.5 to 1.5 μm and more preferably about 1 μm . Also See
10 figure 2, step 206.

11 For example, referring back to figure 4, the slots 404 406 have the
12 minimum edge exclusion (EE) (of 1 μm) on the bottom and left sides of the active region
13 402 (metal area). The minimum edge exclusion (EE) is the minimum distance from the
14 slot to the edge of the metal area.

15 As shown in figure 4, the slots 404 406 442 444 are spaced 410 412 444
16 452 with at least the minimum edge exclusion distance from the edges of the active areas
17 402 440 on the top and right sides.

18 **L. (MS 7) setting the minimum distance between the contact via**
19 **feature and the square slot feature**

20 The minimum distance between the contact via feature and the square
21 slot feature is about 1 μm . Also, see figure 2, step 207.

22 For example, as shown in figs 6A and 6B, a first metal area 1 is formed
23 in a first dielectric layer 612. Square slots SL1 616 618 are placed in ML1 614 (e.g.,
24 metal layer or level 1, or active area 1).

1 A second metal area ML2 644 is formed over the metal area ML1 and
2 in second dielectric layer 650. Square slots SL2 640 642 are placed in metal area ML2 644
3 (e.g., metal layer or level 2, or active region-2).

4 The minimum distance 620 between the contact via feature CL2 and
5 the square slot feature SL1 618 is between about 0.5 and 2.0 and more preferably about 1
6 μm .

7 Referring to Figs 6A and 6B, the distance 628 between slots (SL2) 642
8 640 is about 8 μm because a slot could not be positioned under the via contact CL2. This
9 would violate the (MS7) rule. See figure 2, step 207.

10

11 ***M. example of the square slot placement***

12 Figure 8 shows another example of the square slot placement of the
13 embodiment.

14 Figure 8 is a top down representation of active region (e.g., metal area)
15 802 having slots 804. Slot elements 804 are projection of slots from an adjacent or
16 neighboring layer either immediately above or below the layer of the active region 802.

17 In this example, the slots 803 804 are arranged with respect to reference
18 point 801. Reference point 801 is in the bottom left hand corner of the layout (e.g., layout
19 of chip or IC). But, for reference point 801 could be in other locations. For example, the
20 reference point 801 could be the bottom left corner of a chip die.

21 The slots 803 have at least a minimum edge clearance distance 816 828.

22 Other examples include, the distances 824 826 are about 12.1 μm .

23 Distance 801 is at least 1 μm . Slot spacing distance 822 is about 4 μm . the slots 803 804
24 have are substantially square with lengths and widths of about 2 μm .

N. *the placement of square slots features is performed by an algorithm*

The placement of the square slots can be performed by a program or an algorithm on a computer.

O. *Other embodiments*

In an embodiment, the placement of the square slots features comprises adding square slot representations to a GDS format file that is used to fabricate a mask used in fabricating the semiconductor integrated circuit. The GDS format can be used to create a mask writer specific mask file that is used by an e-beam tool to make a mask.

In an embodiment, least one of the active regions or metal area has a dual damascene shape (e.g., See figure 6B, 644)

In an embodiment, the active regions represent metal lines; pads, and via contacts.

In an embodiment, a semiconductor device can be formed using the method of placing slots.

In an embodiment, masks can be formed using the method to add slots to a layout. For example, a GSD file can be modified to add slots. This modified GSD file can be used to design and fabricate at least a mask used to make the designed device.

IV. *Device and Process for forming a slot in a metal line*

Referring to figures 6A and 6B, slots SL1 and SL2 are placed in metal areas (ML1 and ML2).

Figures 6B, 6C, 6D and 6E are taken along axis 6B in Figure 6A. Figure 6B shows a cross sectional view of Slots (SL2) 640 642 in second metal area (ML2) 644. The metal layers preferably arranged in a vertical overlying relationship. Figure 6B shows via contact CL2 connecting metal level 2 (ML2) (644) to metal level 1 (ML1) (614). In preferred embodiments, metal areas (ML1 and ML2) 614 644 are comprised of

1 copper alloys. In preferred embodiments, metal areas ML1 and ML2 are formed by dual
2 damascene processes. For example, second metal (ML2) is the top trench portion of a dual
3 damascene interconnect and via contact (CL2) is the lower trench contact portion of the
4 dual damascene interconnect.

5 Referring to figure 6C, a metal area one (ML1) 614 is formed in a first
6 dielectric layer 612 (DL1) over a semiconductor structure 601. The semiconductor
7 structure can comprise a semiconductor substrate or a substrate with insulating and
8 conductive layers there over. The first dielectric layer (DL1) 612 can represent any level
9 dielectric layer over the structure 601.

10 A first metal area ML1 614 is formed over the first dielectric layer
11 (DL1) 612. Preferably, the first metal area ML1 is formed using a damascene process.
12 Preferably the first metal area is comprised of a copper alloy. The slots SL1 and SL2 640
13 642 in the first metal area help prevent dishing during the polish process of the damascene
14 process.

15 Referring to Figure 6D, a second dielectric layer (DL2) 650 is formed
16 over the first dielectric layer DL1.

17 The second dielectric layer (DL2) is patterned to form a second metal
18 area opening 621. Preferably the second metal area opening 621 is formed using a dual
19 damascene photolithography process. Those skilled in art will recognize that there are
20 many possible photo processes to form the opening 620.

21 Also, the square slots (SL2) 640 642 are defined in the photo process.
22 The square slots are positioned as described above.

23 Referring to figure 6E, a second metal layer ML2 644 is formed over
24 the surface filling the second metal area opening 620. Preferably the second metal layer
25 ML2 is comprised of a copper alloy.

26 Next, the second metal layer ML2 644 is polished back to form the
27 structure shown in figures 6A and 6B. The embodiments square slots reduce the dishing

1 problem in the wide metal area because the dielectric slots SL2 polish slower than the
2 metal area ML2.

3 **A. *figs 9A – 9C process for forming slots regions comprised of***
4 ***other materials.***

5 In an embodiment, the slots are filled with metal or dielectric material.
6 The slots can be filled with material other than the dielectric material of the ILD layer. The
7 slots could be filled with air or a vacuum. A slot regions comprised of metal layer could
8 improve the current capacity of the metal area or metal line.

9 Figs 9A, 9B, and 9C show cross sectional views similar to those in figs
10 6B to 6E. Figs 9A to 9C show a device and process where the slots are filled with a
11 material other than the dielectric layer (e.g., 950- figure 9C).

12 Figure 9A shows a first dielectric layer 912 with metal area 914.
13 Second dielectric layer 950 is formed over the first dielectric layer 912 and first metal area
14 914.

15 An opening 921 (e.g., via opening) is formed in the second dielectric
16 layer 950.

17 Figure 9B shows square slot regions 942 and 940 formed over the
18 second dielectric layer 950. A layer can be formed over the second dielectric layer and
19 patterned to form slot regions 940 and 942.

20 Symmetrical or Square slot regions 942 and 940 can be comprised of
21 conductive or dielectric materials. For example, square slot regions 942 940 could be
22 formed a metal with a different composition than the subsequently formed second metal
23 area 944. For example, the metal area 944 could be comprised of copper and the slot
24 regions 942 940 could be comprised of Al or W. The square slot regions could be
25 comprised of a metal material that has a low CMP rate than the material of the
26 subsequently formed second area 944 (see figure 9c). Also, the slot regions 942 940 could
27 be comprised of a dielectric such as an oxide, FTEOS or low-k material ($K < 3.9$).

Figure 9C shows a second metal area 944 formed with square slots and square slot regions 940 942. A via contact CL2 contacts the first metal layer 914. The second metal area 944 could be formed using a damascene process where the slot regions 940 942 reduce dishing of the metal 944.

Additional metal layers with square slots can be formed over the structure shown in figure 9C.

B. Computer system

Figure 10 shows a diagram of a non-limiting example embodiment of a computer that can be used in an embodiment of the invention. Referring to figure 10, the computer system 500 shown comprises a CPU (Central Processing Unit) 510, a terminal with a monitor 520 connected to the CPU 510 for receiving data from the CPU 510 and an input device (e.g., keyboard) 530 connected to the CPU 510 for sending data respectively to the CPU 510. A RAM (Random Access Memory) 540 and a DASD 550 associated with the CPU are shown connected for bidirectional communication of data to and from CPU. The slot placing application can run on the computer system or more than one computer system possibly connected by a network. This is an example of a system and network the application can be implemented on.

C. pre-existing initial slot in layout

The active layers can further include initial slots that can be added by designers. These slots are generated before the square slots of the embodiment are added. The "initial slots" are treated or classified as non-active areas or metal spacing and the method(s) described above or in fig 2 are used to place the square slots. This enables designer to add their own slots and still use the program.

D. disadvantages of non-square rectangular slots

In damascene interconnect processes and especially in copper dual damascene process, the copper dishing problem is changing the sheet resistance of the

1 metal lines. Due to Chemical Mechanical Polishing (CMP) for copper lines metal line will
2 be thinned down for wide lines. The inventors have found to reduce the dishing effect,
3 slots are required for wide metal lines.

4 Typically, foundry customers are asked to draw their own rectangular
5 metal slots. However, the orientation of rectangular metal slots needs to follow the current
6 direction. This causes the designers difficult to put in slots in metal lines.

7 Furthermore, during tapeout, dielectric slots in metal line design rules
8 checks are difficult to implement. It also reduces the cycle time for tapeout. For example,
9 in case of (non-square) rectangular slot, its orientation to direction of current flow is
10 impossible to check. Then, it is hard to differentiate metal slot and metal space, then
11 maximum space can not be checked due to software limitation.

12 The embodiments of the invention overcome these and other problems.

1

2 **V. Computer Programs/methods**

3

4 Below is an example of a program to generate and place slots according
 5 to an embodiment. This program is based on Mentor Graphics Calibre TM HDRC
 6 Version v8.8_6.1 Release (or later). Explanatory comments are in italics and set off by
 7 “/”.

8

9 **// Get the areas where slot MUST NOT be generated.**

10 noslots = (Fusebot OR Fusetop) OR (IND_MK OR MS_EXCL)

11 *// Fusebot, Fusetop, IND_MK and MS_Excl are areas where metal slots are undesirable.*

12

13 **//Create generic array (odd) of 2x2um rectangles spaced 4um away inside of chip's**
 14 **Border**

15 slot_odd = RECTANGLES 2 2 4 4 INSIDE OF LAYER Border

16

17 **//Shift the generic “odd” rectangles by 3 um in X axis as even rectangles**

18 slot_even = SHIFT slot_odd BY 3 0

19

20 **// Get contact and via areas to exclude metal slots**21 k_cont = SIZE Contact BY 0.1 *//Size contact up by 0.1*22 k_Via1 = SIZE Via1 BY 0.1 *//Size via1 up by 0.1*23 k_Via2 = SIZE Via2 BY 0.1 *//Size via2 up by 0.1*24 k_Via3 = SIZE Via3 BY 0.1 *//Size via3 up by 0.1*25 k_Via4 = SIZE Via4 BY 0.1 *//Size via4 up by 0.1*26 k_TVia = SIZE TopVia BY 0.1 *//Size Topvia up by 0.1*

27

28 **// Generate odd slots in Metal1(ODD Layer Metal)**

29 widem1a = SIZE Metal1 BY 6.0 UNDEROVER

//Size away metal

30 <=12um

31 widem1 = Metal1 AND widem1a *//Get metal >12um*32 m1slotarea1 = SIZE widem1 BY -1 *//Keep slot 1um away from edge*33 m1slotarea2 = m1slotarea1 NOT (noslots OR (k_cont OR k_Via1)) *//Get final area*
 34 *where slots can be generated.*35 m1slot = slot_odd INSIDE m1slotarea2 *//Use only odd rectangles inside of*
 36 *m1slotarea2*37 Metal1_op = Metal1_opc NOT m1slot *//use m1slot as cookie cutter to cut*
 38 *out slots in Metal1*

39

40

```

1  // Generate odd slots in Metal2(EVEN Layer Metal)
2  widem2a = SIZE Metal2 BY 6.0 UNDEROVER           //Size away metal <=12um
3  widem2 = Metal2 AND widem2a                       //Get metal >12um
4  m2slotarea1 = SIZE widem2 BY -1                   //Keep slot 1um away from edge
5  m2slotarea2 = m2slotarea1 NOT ( noslots OR ( k_Via1 OR k_Via2 ) ) //Get final area
6  where slots can be generated.
7  m2slot = slot_even INSIDE m2slotarea2             //Use only Even rectangles inside of
8  m2slotarea2
9  Metal2_op = Metal2_opc NOT m2slot                 //use m2slot as cookie cutter to cut
10 out slots in Metal2
11
12
13 // Same as metal1, uses ODD rectangles
14 widem3a = SIZE Metal3 BY 6.0 UNDEROVER
15 widem3 = Metal3 AND widem3a
16 m3slotarea1 = SIZE widem3 BY -1
17 m3slotarea2 = m3slotarea1 NOT ( noslots OR ( k_Via2 OR k_Via3 ) )
18 m3slot = slot_odd INSIDE m3slotarea2
19 Metal3_op = Metal3_opc NOT m3slot
20
21 // Same as metal2, uses EVEN rectangles
22 widem4a = SIZE Metal4 BY 6.0 UNDEROVER
23 widem4 = Metal4 AND widem4a
24 m4slotarea1 = SIZE widem4 BY -1
25 m4slotarea2 = m4slotarea1 NOT ( noslots OR ( k_Via3 OR k_Via4 ) )
26 m4slot = slot_even INSIDE m4slotarea2
27 Metal4_op = Metal4_opc NOT m4slot
28
29
30 // Same as metal1, uses ODD rectangles
31 widem5a = SIZE Metal5 BY 6.0 UNDEROVER
32 widem5 = Metal5 AND widem5a
33 m5slotarea1 = SIZE widem5 BY -1
34 m5slotarea2 = m5slotarea1 NOT ( noslots OR ( k_Via4 OR k_TVia ) )
35 m5slot = slot_odd INSIDE m5slotarea2
36 Metal5_op = Metal5_opc NOT m5slot
37
38
39 // Same as metal2, uses EVEN rectangles
40 widemt = SIZE MT BY 6.0 UNDEROVER                // 6th (TOP) metal
41 widemt = MT AND widemt
42 mtslotarea1 = SIZE widemt BY -1
43 mtslotarea2 = mtslotarea1 NOT ( noslots OR k_TVia )
44 mtslot = slot_even INSIDE mtslotarea2
45 MT_op = MT NOT mtslot
46

```

1 A preferred embodiment of the invention comprises a computer system
2 for determining a determining the placement of substantially square slots representations in
3 a layout; the layout comprised of a plurality of representations of conductive layers; the
4 conductive layer representations comprised of conductive region representations;

5 at least one the conductive region representations has a via contact
6 representation between adjacent active layers; the system comprising :

7 a means for determining the placement of square slots representations
8 in the layout by the following:

9 a means for setting a reference for the placement of the square slot
10 representations with respect to the layout;

11 a means for setting the minimum dimensions of the conductive region
12 representations in which the square slot representations are inserted in;

13 a means for setting the dimensions of the square slot representations ;

14 a means for setting the spacing between the square slot representations
15 in the conductive layer representations;

16 a means for setting the clearance between the square slot representations
17 on adjacent conductive layer representations;

18 a means for setting the stagger spacing between rows of adjacent square
19 slot representations in the layer representations;

20 a means for setting the minimum distance from the edge of the square
21 slot representation to the edge of the conductive region representation;

22 a means for setting the minimum distance between the contact via
23 representation and the square slot representation.

24 The listing of the program above shows examples of the “means for”
25 described above.

26
27 Note that most metal patterns are rectangular shaped because it is easier
28 to design layouts. However , the invention is suitable were metal lines have other shapes.

1 In addition, in embodiments where square shaped slots are discussed,
2 other shaped slots are feasible and the embodiments are not limited to square slots. For
3 example, slots with symmetric shapes, especially in the direction of current flow are
4 feasible.

5 In forming a mask using the embodiments of the invention, the active
6 areas and non-active areas are defined by areas of different transmittance. (e.g., opaque or
7 transparent areas, such as positive or negative masks).

8
9 In the above description numerous specific details are set forth such as
10 dimensions, in order to provide a more thorough understanding of the present invention. It
11 will be obvious, however, to one skilled in the art that the present invention may be
12 practiced without these details. In other instances, well known process have not been
13 described in detail in order to not unnecessarily obscure the present invention.

14 Unless explicitly stated otherwise, each numerical value and range
15 should be interpreted as being approximate as if the word “about” or “approximately”
16 preceded the value of the value or range.

17 While the invention has been particularly shown and described with
18 reference to the preferred embodiments thereof, it will be understood by those skilled in
19 the art that various changes in form and details may be made without departing from the
20 spirit and scope of the invention. It is intended to cover various modifications and similar
21 arrangements and procedures, and the scope of the appended claims therefore should be
22 accorded the broadest interpretation so as to encompass all such modifications and similar
23 arrangements and procedures.

1

2

3 What is claimed is:

4 1. A method for determining the placement of slots representations in a layout;

5 said layout comprised of a plurality of conductive layer representations;

6 said conductive layer representation comprised of conductive region

7 representations;

8 at least one said conductive region representation has a via contact representation

9 between adjacent active layers;

10 the method comprising the steps of:

11

12 setting a reference for the placement of said slot representations with

13 respect to said layout;

14 setting the minimum dimensions of said conductive region

15 representations in which said slot representations are placed;

16 setting the dimensions of said slot representations;

17 setting the spacing between slot representations in conductive layer

18 representations;

19 setting the clearance between the slot representations on adjacent

20 conductive layer representations;

21 setting the stagger spacing between rows of adjacent slot

22 representations in conductive layer representations;

23 setting the minimum distance from the edge of said slot representations

24 to the edge of said conductive region representations;

25 setting the minimum distance between said contact via representation

26 and said slot representation.

27

28 2. The method of claim 1 wherein said slots have a substantially square shape.

1 3. The method of claim 1 wherein said slots have a shape selected from the group
2 consisting of: substantially square, substantially circular, substantially hexagon,
3 and substantially octagon.

4 4. The method of claim 1 wherein said conductive layer representations represent
5 conductive layers in a semiconductor device.

6 5. The method of claim 1 which further includes:

7 said slots have a shape selected from the group consisting of:
8 substantially square, substantially circular, substantially hexagon, and substantially
9 octagon;

10 said reference for the placement of said slot representations is a corner
11 of said layout;

12 setting the minimum dimensions of said conductive region
13 representations in which said slot representations are inserted in, to a length greater about
14 12 μm and a width greater than about 12 μm ;

15 setting the dimensions of said slot representations to about 2 μm by
16 about 2 μm or about 4 square μm ;

17 setting the spacing between the slot representations on the same
18 conductive layer representation to about 4 μm ;

19 setting the clearance between the slot representations on adjacent
20 conductive layers representations to about 1 μm ;

21 setting the stagger spacing between rows of adjacent slot
22 representations in a single conductive region representation to about 0 μm ;

23 setting the minimum distance from the edge of said slot representation
24 to the edge of said conductive region representation to about 1 μm ;

25 setting the minimum distance between said contact via representation
26 and said slot representation to about 1 μm .

27

- 1 6. The method of claim 1 which further includes outputting the placement of said slots
2 representations.
3
- 4 7. The semiconductor device formed using the method of claim 1.
- 5 8. The mask formed using the method of claim 1.
- 6 9. The computer data generated using the method of claim 1.
7
- 8 10. A method for determining the placement of substantially square slots features in a
9 layout of an integrated circuit design;
10 said layout comprised of a plurality of active layers;
11 said active layers comprised of active regions;
12 at least one said active regions has a via contact feature between adjacent active
13 layers;
14 the method comprising the steps of :
15 setting a reference for the placement of said square slots feature with
16 respect to said layout;
17 setting the minimum dimensions of said active regions in which said
18 square slots features are placed;
19 setting the dimensions of said square slot features;
20 setting the spacing between the square slots features on the same active
21 region;
22 setting the clearance between the square slots features on adjacent active
23 layers ;
24 setting the stagger spacing between rows of adjacent square slots
25 features in said active layers;
26 setting the minimum distance from the edge of said square slot features
27 to the edge of said active region;

1 setting the minimum distance between said contact via feature and said
2 square slot feature.

3
4 11. The method of claim 10 wherein said layout comprises initial slots that are added
5 before the determining the placement of the square slots;

6 the method further comprises: classifying the initial slots as non-active
7 areas.

8 12. The method of claim 10 wherein said active layers represent conductive layers in a
9 semiconductor device.

10 13. The method of claim 10 which further includes

11 said reference for the placement of said slots is the bottom left corner of
12 said layout;

13 setting the minimum dimensions of said active regions in which said
14 square slots features are inserted in to a minimum length of about 12 μm and a minimum
15 width of about 12 μm ;

16 setting the dimensions of said square slot features to about 2 μm by
17 about 2 μm ;

18 setting the spacing between the square slots features on the same active
19 region to about 4 μm ;

20 setting the clearance between the square slots features on adjacent active
21 layers to about 1 μm ;

22 setting the stagger spacing between rows of adjacent square slots in the
23 same metal area to about 0 μm ;

24 setting the minimum distance from the edge of said square slot features
25 to the edge of said active region to about 1 μm ;

26 setting the minimum distance between said contact via feature and said
27 square slot feature to about 1 μm .

28

- 1 14. The method of claim 10 which further includes outputting the placement of said square
2 slots features.
- 3 15. The semiconductor device formed using the method of claim 10.
- 4 16. The mask formed using the method of claim 10.
- 5 17. The computer data generated using the method of claim 10.
- 6 18. The computer implemented method performing the method of claim 10.
- 7
- 8 19. A computer implemented method for determining the placement of substantially
9 square slots features in a layout of an integrated circuit design;
10 providing a layout comprised of a plurality of active layers;
11 said active layers comprised of active regions;
12 at least one said active regions has a via contact feature between adjacent active
13 layers;
- 14 the method comprising the steps of :
- 15 setting a reference for the placement of said square slot features with
16 respect to said layout;
- 17 setting the minimum dimensions of said active regions in which said
18 square slot features are inserted in to a minimum length of about 12 μm and a minimum
19 width of about 12 μm ;
- 20 setting the dimensions of said square slot features are about 2 μm by
21 about 2 μm ;
- 22 setting the spacing between the square slot features on a single active
23 region to about 4 μm ;
- 24 setting the clearance between the square slot features on adjacent active
25 layers to about 1 μm ;
- 26 setting the stagger spacing between rows of adjacent square slot features
27 in the same active area to about 0 μm ;

- 1 setting the minimum distance from the edge of said square slot features
2 to the edge of said active region to about 1 μm ;
- 3 setting the minimum distance between said contact via feature and said
4 square slot feature to about 1 μm .
- 5
- 6 20. The method of claim 19 said reference for the placement of said square slot features is
7 a corner of said layout.
- 8 21. The method of claim 19 wherein said square slot features are substantially square.
- 9 22. The method of claim 19 wherein said square slots features represent square shapes
10 with lengths and widths of between about 0.5 and 4 μm .
- 11 23. The method of claim 19 wherein said active areas are defined using 0.13 μm and
12 0.09 μm ground rules.
- 13 24. The method of claim 19 wherein said layout is represented by a GSD format file; said
14 layout is comprised of layers; said layers are comprised of active layers and square
15 slot layers;
- 16 said layers are represented by a GDS layer number; said active layers
17 are represented by a GDS layer number and first data type number;
- 18 said square slot layers represented by a GDS layer number and second
19 data type number;
- 20 the active layers and square slot layers in the same layer have the same
21 GDS layer number but different data types number.
- 22 25. The method of claim 19 wherein the placement of the square slots features comprises:
23 generating said square slot representations; and using a logical "NOT" operation to
24 not out slots in said active layer in a data file that is used to fabricate a mask.
- 25 26. The method of claim 19 wherein at least one of said active regions has a dual
26 damascene shape.
- 27 27. The method of claim 19 wherein said active regions represent metal lines; pads, and
28 via contacts.

- 1 28. The semiconductor device formed using the method of claim 19.
- 2 29. The mask formed using the method of claim 19.
- 3 30. The computer data generated using the method of claim 19.
- 4
- 5 31. A semiconductor device comprising:
- 6 a plurality metal layers over a substrate; said metal layers comprised of
- 7 metal areas;
- 8 via contacts between said metal layers;
- 9 square slots in said metal areas;
- 10 said square slots are substantially square;
- 11
- 12 said square slots positioned as follows:
- 13 said square slots placed with respect to a reference point;
- 14 said square slots positioned only in metal areas with dimensions greater
- 15 than a minimum metal area dimensions;
- 16 a spacing between said square slots on a single metal area;
- 17 a stagger spacing between rows of adjacent square slots in the same
- 18 metal layer;
- 19 a clearance between said square slots on adjacent metal layers;
- 20 a minimum distance from the edge of said square slots to the edge of
- 21 said metal areas;
- 22 a minimum distance between said contact via and said square slots.
- 23
- 24 32. The semiconductor device of claim 31 that further comprises :
- 25 said reference is a corner of said layout; said layout having a
- 26 rectangular shape;
- 27 said minimum metal area dimensions are a minimum length of about 12
- 28 μm and a minimum width of about 12 μm ;

1 said square slot dimension is about 2 μm by about 2 μm ;
2 the spacing between said square slots on the same metal layer is about 4
3 μm ;
4 the clearance between said square slots on adjacent metal layers is
5 about 1 μm ;
6 said square slots having a stagger spacing between rows of adjacent
7 square slots in the same metal layer to about 0 μm ;
8 the minimum distance from the edge of said square slots to the edge of
9 said metal areas is about 1 μm ;
10 the minimum distance between said contact via and said square slots is
11 about 1 μm .

12
13
14 33. The semiconductor device of claim 31 wherein said square slots are comprised of
15 dielectric material or conductive material.

16 34. The semiconductor device of claim 31 wherein said square slots have a dimension of
17 between about 1.9 and 2.1 μm .

18
19 35. The semiconductor device of claim 31 wherein said metal areas are comprised of
20 copper alloy and have a dual damascene shape.

21
22 36. One or more processor readable storage devices having processor readable code
23 embodied on said process readable storage devices, said processor readable code
24 for programming one or more processors to perform a method of determining a
25 determining the placement of substantially square slots representations in a layout;
26 said layout comprised of a plurality of representations of conductive layers;
27 said conductive layer representations comprised of conductive region
28 representations;

1 at least one said conductive region representations has a via contact representation
2 between adjacent active layers;
3 the method comprising the steps of:
4 setting a reference for the placement of said square slot representations
5 with respect to said layout;
6 setting the minimum dimensions of said conductive region
7 representations in which said square slot representations are placed;
8 setting the dimensions of said square slot representations ;
9 setting the spacing between the square slot representations in a single
10 conductive layer representation;
11 setting the clearance between the square slot representations on adjacent
12 conductive layer representations;
13 setting the stagger spacing between rows of adjacent square slot
14 representations in a single conductive region representation;
15 setting the minimum distance from the edge of said square slot
16 representation to the edge of said conductive region representation;
17 setting the minimum distance between said contact via representation
18 and said square slot representation.
19 37. The storage device of claim 36 which further includes
20 said reference for the placement of said square slot representations is a
21 corner of said layout;
22 setting the minimum dimensions of said conductive region
23 representations in which said square slot representations are inserted in to a minimum
24 length of about 12 μm and a minimum width of about 12 μm ;
25 setting the dimensions of said square slot representations to about 2 μm
26 by about 2 μm ;
27 setting the spacing between the square slot representations on the same
28 conductive region representation to about 4 μm ;

1 setting the clearance between the square slot representations on adjacent
2 conductive layers representations to about 1 μm ;
3 setting the stagger spacing between rows of adjacent square slot
4 representations in said conductive layer representations to about 0 μm ;
5 setting the minimum distance from the edge of said square slot
6 representation to the edge of said conductive region representations to about 1 μm ;
7 setting the minimum distance between said contact via representation
8 and said square slot representation to about 1 μm .

9
10 38. The storage device of claim 36 which further includes outputting the placement of said
11 square slots representations.

12
13 39. A computer system for determining a determining the placement of substantially
14 square slots representations in a layout; said layout comprised of a plurality of
15 representations of conductive layers; said conductive layer representations
16 comprised of conductive region representations; at least one said conductive
17 region representations has a via contact representation between adjacent active
18 layers; the system comprising :

19
20 a means for determining the placement of square slots representations
21 in said layout by the following:

22 a means for setting a reference for the placement of said square slot
23 representations with respect to said layout;

24 a means for setting the minimum dimensions of said conductive region
25 representations in which said square slot representations are inserted in;

26 a means for setting the dimensions of said square slot representations ;

27 a means for setting the spacing between the square slot representations
28 in said conductive layer representations;

1 a means for setting the clearance between the square slot representations
2 on adjacent conductive layer representations;

3 a means for setting the stagger spacing between rows of adjacent square
4 slot representations in said layer representations;

5 a means for setting the minimum distance from the edge of said square
6 slot representation to the edge of said conductive region representation;

7 a means for setting the minimum distance between said contact via
8 representation and said square slot representation.

9
10 40. The computer system of claim 39 wherein:

11 said means for determining the placement of square slots
12 representations in said layout further includes:

13 said reference for the placement of said square slot representations is a
14 corner of said layout;

15 said means for setting the minimum dimensions of said conductive
16 region representations in which said square slot representations are inserted in to a length
17 greater than about 12 μm and a width greater than about 12 μm ;

18 said means for setting the dimensions of said square slot representations
19 to about 2 μm by about 2 μm ;

20 said means for setting the spacing between the square slot
21 representations on the conductive layer representations to about 4 μm ;

22 said means for setting the clearance between the square slot
23 representations on adjacent conductive layers representations to about 1 μm ;

24 said means for setting the stagger spacing between rows of adjacent
25 square slot representations in a single conductive region representation to about 0 μm ;

26 said means for setting the minimum distance from the edge of said
27 square slot representation to the edge of said conductive region representation to about 1
28 μm ;

- 1 said means for setting the minimum distance between said contact via
2 representation and said square slot representation to about 1 μm .
3
4 41. The system of claim 39 which further includes a means for outputting the placement of
5 said square slots representations.
6