

Abstract of the Disclosure (Fig. 1)

MASTER SLICE INTEGRATED CIRCUIT DEVICE

A master slice integrated circuit device comprises an internal cell array ($C_{m,n} - C_{m+5, n+2}$) and an external cell array ($20_m - 20_{m+3}$) formed outwardly from the internal cell array, a main power circuit region (30) formed on the external cell array, a plurality of power lines (1_m) in electrical continuity with the main power circuit region and formed on the internal array region, and a plurality of signal lines for electrically interconnecting prescribed contact members of the internal and external cells. Each power line is connected with the main power circuit region via an intermediate circuit region (40) comprising a fixed position branch-off portion (42) originating at a position on the main power circuit region and extending substantially in the direction of an associated one of the power lines and an intersecting connection allowance portion (44) of prescribed length attached to the fixed position branch-off portion.