

ABSTRACT

A semiconductor package, includes: a base chip having a front surface and a back surface opposite to the front surface, the base chip including bump pads, wafer test pads, and package test pads, disposed on the front surface; connection structures disposed on the front surface
5 of the base chip and connected to the bump pads; and semiconductor chips stacked on the back surface of the base chip, wherein each of the wafer test pads is smaller than the package test pads.

FIG. 1