



DRAM DATA STORAGE AND MOVEMENT FOR NETWORK PROCESSORS

ABSTRACT

The ability of network processors to move data to and from dynamic random access memory (DRAM) chips used in computer systems is enhanced in several respects. In one aspect of the invention, two double data rate DRAMS are used in parallel to double the bandwidth for increased throughput of data. The movement of data is further improved by setting 4 banks of full "read" and 4 banks full of "write" by the network processor for every repetition of the DRAM time clock. A scheme for randomized "read" and "write" access by the network processor is disclosed. This scheme is particularly applicable to networks such as Ethernet that utilize variable frame sizes.

FIG. 1