What is claimed is:

1. A method of manufacture of an integrated circuit packaging system comprising:

forming a dielectric core having an embedded pad, another embedded pad, a surface trace between the embedded pad and the another embedded pad, and having core sidewalls, the core sidewalls extending between a core top side of the dielectric core and a pad top surface of the embedded pad, and a portion of the core sidewalls exposed from the embedded pad;

forming a top solder resist layer on the dielectric core, a pad top surface of the embedded pad below the top solder resist layer, the top solder resist layer exposing a mounting region continuously exposing both the embedded pad and the another embedded pad, and the surface trace exposed from the dielectric core within the mounting region;

forming a device interconnect on the embedded pad, the device interconnect in contact with the core sidewalls; and

mounting an integrated circuit device having an interconnect pillar, the interconnect pillar attached to the device interconnect for mounting the integrated circuit device to the dielectric core.

2. The method as claimed in claim 1 wherein forming the top solder resist layer includes forming the pad top surface below a core top surface of the dielectric core.

3. The method as claimed in claim 1 wherein forming a surface trace on the dielectric core includes forming the surface trace below the top solder resist layer.

4. The method as claimed in claim 1 wherein forming a surface trace on the dielectric core includes forming the surface trace below the core top surface.

5. The method as claimed in claim 1 wherein forming the dielectric core include forming a system pad on a core bottom side of the dielectric core.

6. A method of manufacture of an integrated circuit packaging system comprising:

forming a dielectric core having an embedded pad , another embedded pad, core sidewalls, and a surface trace between the embedded pad and the another embedded pad, the core sidewalls extending between a core top side of the dielectric core and a pad top surface of the embedded pad and a portion of the core sidewalls exposed from the embedded pad;

forming a top solder resist layer on the dielectric core, a pad top surface of the embedded pad below the top solder resist layer, the top solder resist layer exposing a mounting region exposing both the embedded pad and the another embedded pad, and the surface trace exposed from the dielectric core within the mounting region;

attaching a device interconnect on the embedded pad , the device interconnect in contact with the core sidewalls; and

mounting an integrated circuit device having an interconnect pillar, the interconnect pillar attached to the device interconnect for mounting the integrated circuit device to the dielectric core.

7. The method as claimed in claim 6 wherein forming the dielectric core includes forming the embedded pad coplanar with a core top side of the dielectric core.

8. The method as claimed in claim 6 wherein forming the dielectric core includes forming the embedded pad coplanar with the surface trace.

9. The method as claimed in claim 6 wherein forming the dielectric core includes forming the surface trace between the embedded pad and another of the embedded pad on a core top surface of the dielectric core.

10. The method as claimed in claim 6 further comprising mounting an external interconnect on a core bottom side of the dielectric core.

11. An integrated circuit packaging system comprising:

a dielectric core having an embedded pad , another embedded pad, a surface trace between the embedded pad and the another embedded pad, and core sidewalls, the core sidewalls extending between a core top side of the dielectric core and a pad top surface of the embedded pad and a portion of the core sidewalls exposed from the embedded pad;

a top solder resist layer on the dielectric core, a pad top surface of the embedded pad below the top solder resist layer, the top solder resist layer exposing a mounting region exposing both the embedded pad and the another embedded pad, and the surface trace exposed from the dielectric core within the mounting region;

a device interconnect attached to the embedded pad, the device interconnect in contact with the core sidewalls; and

an integrated circuit device having an interconnect pillar, the interconnect pillar attached to the device interconnect for mounting the integrated circuit device to the dielectric core.

12. The system as claimed in claim 11 wherein the pad top surface of the embedded pad is below a core top surface of the dielectric core.

13. The system as claimed in claim 11 wherein the surface trace is below the top solder resist layer.

14. The system as claimed in claim 11 wherein the surface trace is below the core top surface.

15. The system as claimed in claim 11 further comprising:

a bottom solder resist layer on the dielectric core; and

a system pad on the dielectric core and exposed from the bottom solder resist layer.

16. The system as claimed in claim 11 wherein the surface trace is formed on the dielectric core.

17. The system as claimed in claim 16 wherein the embedded pad is coplanar to a core top side of the dielectric core.

18. The system as claimed in claim 16 wherein the embedded pad is coplanar with the surface trace.

19. The system as claimed in claim 16 wherein the surface trace is between the embedded pad and another of the embedded pad on a core top surface of the dielectric core.

20. The system as claimed in claim 16 further comprising an external interconnect on a core bottom side of the dielectric core.