

ABSTRACT

A METHOD TO FORM SHALLOW TRENCH ISOLATIONS

A method of forming shallow trench isolations is achieved. STI structures so formed do not exhibit isolation oxide thinning due to dishing and erosion problems during the oxide CMP process. A silicon substrate is provided. A first dielectric layer is formed overlying the silicon substrate. A silicon nitride layer is deposited. The silicon nitride layer, the first dielectric layer, and the silicon substrate are etched to form trenches for planned shallow trench isolations. A second dielectric layer is deposited overlying the silicon nitride layer and the trenches. The second dielectric layer is etched to form sidewall spacers inside the trenches. A silicon layer is selectively grown overlying the silicon substrate only where the silicon substrate is exposed in the trenches, and wherein the step of growing is stopped before the silicon layer exceeds the top surface of the silicon nitride layer. A third dielectric layer is deposited overlying the silicon nitride layer, the sidewall spacers, and the silicon layer. The third dielectric layer is polished down to the top surface of the silicon nitride layer to complete the shallow trench isolations where the silicon nitride layer acts as a polishing stop, and the integrated circuit device is completed.

(FIGURE 2 IS SUGGESTED FOR PUBLICATION)