

METHOD AND APPARATUS FOR PERFORMING OPERATIVE TESTING ON AN INTEGRATED CIRCUIT

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Abstract of the Disclosure

A method of detecting defective CMOS devices by quiescent current (IDDQ) behavior using a monitor circuit resident in the expendable areas of a die and/or wafer. One embodiment of the present invention incorporates a monitor unit (10) into the scribe grid of a wafer, where pads (2, 3, 4) are built in the corners of the die (5) and connected to the monitor unit (10) via metal connects in the wafer. The monitor unit (10) determines defective die based on IDDQ as expressed by decay of voltage (V_{dd}) in time, where V_{dd} is supplied to a die by way of a switch (20) in the monitor unit (10). Alternate
15 embodiments incorporate various configurations and incorporate functional and other tests into a wafer level test system. Other embodiments provide the monitor unit on the die, allowing for later testing and user confirmation.

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FIG. 2 accompanies this abstract.

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