

ROM CELL CIRCUIT FOR FINFET DEVICES

ABSTRACT

The present disclosure provides a read only memory (ROM) cell array. The ROM cell array includes a plurality of fin active regions oriented in a first direction and formed on a semiconductor substrate; a plurality of gates formed on the plurality of fin active regions and oriented in a second direction perpendicular to the first direction; and a plurality of ROM cells formed by the plurality of fin active regions and the plurality of gates, the plurality of ROM cells being coded such that each cell of a first subset of ROM cells has a source electrically connected to a Vss line, and each cell of a second subset of ROM cells has a source electrically isolated. Each cell of the first subset of ROM cells includes a drain contact having a first contact area and a source contact having a second contact area at least 30% greater than the first contact area.

Figure 2