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ABSTRACT

A NOVEL METHOD OF FABRICATING VARIABLE LENGTH VERTICAL TRANSISTORS

A process for fabricating vertical CMOS devices, featuring variable channel lengths, has been developed. Channel region openings are defined in composite insulator stacks, with the channel length of specific devices determined by the thickness of the composite insulator stack. Selective removal of specific components of the composite insulator stack, in a specific region, allows the depth of the channel openings to be varied. A subsequent epitaxial silicon growth procedure fills the variable depth channel openings, providing the variable length, channel regions for the vertical CMOS devices.

FIGURE 14