

INPUT BUFFER CIRCUIT HAVING SLEEP MODE AND BUS HOLD FUNCTION

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Abstract of the Disclosure

The present invention includes an input buffer circuit (10) having sleep mode and bus hold capability. An input section (11) of the buffer circuit is operated from an operating voltage which is lower than a supply voltage of the buffer circuit thereby minimizing the static power dissipation. Sleep mode circuitry (15, 36, 38) is included for effectively disconnecting an input signal from the rest of the buffer circuit thereby minimizing dynamic power dissipation. Bus hold circuitry (40) is included for holding the logic state appearing at an output of the input buffer circuit when the input signal is removed thereby further reducing the static power dissipation.

FIG. 1 accompanies this abstract.