

DESCRIPTION

WAFER APPEARANCE INSPECTION DEVICE AND METHOD

5 TECHNICAL FIELD

[0001] The present invention relates to the wafer visual inspection apparatus and method for comparing a captured inspection image of a repeated visual pattern of a device chip formed on a wafer with a reference image to inspect the device chip.

10 BACKGROUND ART

[0002] A semiconductor device is, after many semiconductor device circuits (i.e., a repeated visual pattern of device chips) have been formed on a single semiconductor wafer, divided into chip components. Such a chip component is packaged, and is shipped as an individual electronic component or is incorporated into an electric product.

15 [0003] Before the semiconductor device is divided into the chip components, the repeated visual pattern of the device chips formed on the wafer is inspected by comparison between a captured inspection image and a reference image (e.g., Patent Document 1) or is electrically inspected using a probe (e.g., Patent Document 2).

[0004] The device chips formed in a matrix on the wafer in the repeated pattern include
20 “complete chips” diced into products and “incomplete chips” which cannot be developed as products due to a lack of part of the pattern. Quality determination (so-called inspection) is performed for the complete chips by comparison between an image of a chip appearance and a reference image, and on the other hand, is not performed for the incomplete chips for the purpose of shortening a processing time (e.g., Patent Document 3).

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CITATION LIST

PATENT DOCUMENT

[0005] PATENT DOCUMENT 1: Japanese Unexamined Patent Publication No. 2007-155610

5 PATENT DOCUMENT 2: Japanese Unexamined Patent Publication No. H2-290036

PATENT DOCUMENT 3: Japanese Unexamined Patent Publication No. H4-276642

10 SUMMARY OF THE INVENTION

TECHNICAL PROBLEM

[0006] However, since visual inspection is performed for the complete chip while not performed for the incomplete chip, the wafer is delivered to a subsequent step even if there are a scratch, a foreign substance, etc. on the incomplete chip.

15 [0007] For this reason, if probe inspection is performed later, the scratch, the foreign substance, etc. on the incomplete chip contact a probe. This might lead to some problems such as probe damage and wafer cracking/chipping.

[0008] According to a typical visual inspection technique, part of a captured inspection image of an incomplete chip includes a chipped portion. Such a portion is determined as
20 abnormal upon comparison with a reference image, leading to detection of a false defect. Such false defect detection leads to an increase in a processing time.

[0009] For this reason, the present invention has been made in view of the above-described problems, and an object of the present invention is to provide the wafer visual inspection apparatus and method capable of performing inspection according to a complete chip even for
25 an incomplete chip formed over an inspection region and a non-inspection region on a wafer

if the incomplete chip is in the inspection region of the wafer, obtaining a desired inspection result for the entirety of the inspection region of the wafer, and preventing an increase in a processing time.

5 SOLUTION TO THE PROBLEM

[0010] For solving the above-described problems, one aspect of the present invention is the wafer visual inspection apparatus for capturing an image of an inspection target location of a repeated visual pattern of a device chip formed on a wafer to inspect the device chip by comparison with a reference image, which includes

- 10 a wafer holding unit configured to hold the wafer,
- an image capturing unit configured to capture an image including the inspection target location,
- a relative movement unit configured to move the wafer holding unit and the image capturing unit relative to each other,
- 15 a reference image registration unit configured to register the reference image,
- a chip layout registration unit configured to register a chip layout for defining an inspection region and a non-inspection region of the wafer with respect to the reference posture and position of the wafer,
- an image processing unit configured to process the image captured by the image capturing unit.
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The image processing unit includes

- a dynamic mask processing unit configured to replace the brightness value of at least one, which is a pixel corresponding to the non-inspection region, of pixels forming a captured image of an inspection target location of an incomplete chip formed over
- 25 the inspection region and the non-inspection region, with the brightness value of the

reference image based on positional information on the wafer for which the image has been captured and the chip layout, thereby generating an inspection image, and

a comparison inspection unit configured to compare the inspection image generated by the dynamic mask processing unit with the reference image, thereby inspecting the inspection target location.

[0011]

Another aspect of the present invention is

the wafer visual inspection method for capturing an image of an inspection target location of a repeated visual pattern of a device chip formed on a wafer to inspect the device chip by comparison with a reference image, which includes

registering the reference image in advance;

registering, in advance, a chip layout for defining an inspection region and a non-inspection region of the wafer with respect to the reference posture and position of the wafer, capturing an image including the inspection target location while moving the wafer

and an image capturing section relative to each other, and

processing the image.

The processing the image includes

replacing the brightness value of at least one, which is a pixel corresponding to the non-inspection region, of pixels forming a captured image of an incomplete chip formed over the inspection region and the non-inspection region, with the brightness value of the reference image based on positional information on the wafer for which the image has been captured and the chip layout, thereby generating an inspection image, and

comparing the inspection image with the reference image, thereby inspecting the inspection target location.

[0012] According to these wafer visual inspection apparatus and method, even for incomplete chips whose outer edge shapes vary according to an image capturing position, dynamic mask processing can be performed according to the image capturing position to generate the inspection image, and desired inspection can be performed by comparison
5 between the inspection image and the reference image.

ADVANTAGES OF THE INVENTION

[0013] Inspection according to the complete chip can be performed even for the incomplete chip formed over the inspection region and the non-inspection region on the wafer if the
10 incomplete chip is in the inspection region of the wafer, the desired inspection result can be obtained for the entirety of the inspection region of the wafer, and an increase in the processing time can be prevented.

BRIEF DESCRIPTION OF THE DRAWINGS

15 [0014] [FIG. 1] FIG. 1 is a schematic view showing an entire configuration of one example of an embodied form of the present invention.

[FIG. 2] FIG. 2 is a conceptual diagram showing the state of image capturing in one example of the embodied form of the present invention.

[FIG. 3] FIG. 3 is a plan view showing a positional relationship among device
20 chips C in one example of the embodied form of the present invention.

[FIG. 4] FIGS. 4(a) to 4(d) are views showing an image Ps, a reference image Pf, an inspection image Pk, and a difference between the inspection image Pk and the reference image Pf in one example of the embodied form of the present invention.

[FIG. 5] FIGS. 5(a) to 5(d) are views showing the brightness value of each pixel
25 of the image Ps, the reference image Pf, and the inspection image Pk and a difference in the

brightness value between the inspection image Pk and the reference image Pf in one example of the embodied form of the present invention.

[FIG. 6] FIG. 6 is a flowchart in one example of the embodied form of the present invention.

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DESCRIPTION OF EMBODIMENTS

[0015] Hereinafter, an embodiment of the present invention will be described with reference to the drawings. Note that in description below, three axes of an orthogonal coordinate system are X, Y, and Z, the horizontal direction is expressed as an X-direction and a Y-direction, and a direction (i.e., the direction of the force of gravity) perpendicular to an XY plane is expressed as a Z-direction. Of the Z-direction, a direction against the force of gravity is expressed as an upper side, and a direction in which the force of gravity works is expressed as a lower side. Moreover, a rotation direction about the Z-direction is referred to as a θ -direction.

15 [0016] FIG. 1 is a schematic view showing an entire configuration of one example of an embodied form of the present invention. FIG. 1 schematically shows each portion forming a wafer visual inspection apparatus 1 according to the present invention.

[0017] The wafer visual inspection apparatus 1 captures an image of an inspection target location of a repeated visual pattern of device chips C formed on a wafer W, thereby
20 comparing the image with a reference image Pf to inspect the device chip C.

[0018] Specifically, the wafer visual inspection apparatus 1 captures, while sequentially changing an image capturing location, an image Ps of the inspection target location to generate an inspection image Pk by processing of the captured image Ps, thereby comparing the inspection image Pk and the reference image Pf with each other to perform desired
25 inspection, such as whether or not there are short-circuit, disconnection, etc. in a circuit

pattern of the device chip C or whether or not there are a foreign substance, a scratch, etc. in the circuit pattern of the device chip C, across the entire surface of the wafer W.

The wafer visual inspection apparatus 1 includes, for example, a wafer holding unit 2, an image capturing unit 3, a relative movement unit 4, a chip layout registration unit 5, a reference image registration unit 6, an image processing unit 7, and a control unit CN.

[0019] The wafer holding unit 2 holds the wafer W.

Specifically, the wafer holding unit 2 supports the wafer W from a lower side while holding the wafer W in a horizontal state. More specifically, the wafer holding unit 2 includes a mount 20 whose upper surface is horizontal.

10 A groove and a hole are provided at part of the mount 20 which is to contact the wafer W, and are connected to a negative pressure generation section such as a vacuum pump through a switching valve, for example. The wafer holding unit 2 switches the groove and the hole to a negative pressure state or a vented state, thereby holding or releasing the wafer W.

15 [0020] The image capturing unit 3 captures the image Ps including the inspection target location. The image Ps including the inspection target location as described herein is a captured image including part or the entirety of the repeated visual pattern of the device chips C targeted for inspection, and indicates divided images of the inspection target location of each device chip C or an image of a wide area (an image capturing region F) including the
20 inspection target locations of one or more device chips C.

[0021] Specifically, the array (e.g., the number of chips and a pitch) of the device chips C, a required inspection accuracy, etc. vary according to the type of product to be inspected, and therefore, the size, position, interval, etc. of the area (i.e., an image capturing area) whose image is to be captured by the image capturing unit 3 are registered corresponding to each
25 product to be inspected.

More specifically, the image capturing unit 3 includes, for example, a lens barrel 30, an illumination unit 31, a half mirror 32, multiple objective lenses 33a, 33b, a revolver mechanism 34, and an image capturing camera 35.

[0022] The lens barrel 30 fixes the illumination unit 31, the half mirror 32, the objective
5 lenses 33a, 33b, the revolver mechanism 34, the image capturing camera 35, etc. to predetermined postures, thereby guiding illumination light or observation light. The lens barrel 30 is attached to an apparatus frame 1f through, e.g., a coupling metal fitting (not shown).

[0023] The illumination unit 31 emits illumination light L1 necessary for image capturing.
10 Specifically, examples of the illumination unit 31 may include a laser diode, a metal halide lamp, a xenon lamp, and an LED lamp.

[0024] The half mirror 32 reflects the illumination light L1 emitted from the illumination unit 31 to irradiate the wafer W with the illumination light L1, and allows light (reflected light, scattered light) L2 entering from a wafer W side to pass toward an image capturing
15 camera 35 side.

[0025] The objective lenses 33a, 33b form, with different predetermined observation magnifications, the image of the image capturing area on the wafer W on an image capturing element 36 of the image capturing camera 35.

[0026] The revolver mechanism 34 makes such switching for using either one of the
20 objective lenses 33a, 33b. Specifically, the revolver mechanism 34 rotates by a predetermined angle and stops manually or based on signal control made from the outside.

[0027] The image capturing camera 35 captures the image of the image capturing region F on the wafer W, thereby acquiring the image Ps formed on the image capturing element 36. The acquired image Ps is output as a video signal or video data to the outside, and is
25 processed in the image processing unit 7 for generation of the inspection image Pk.

[0028] The relative movement unit 4 moves the wafer holding unit 2 and the image capturing unit 3 relative to each other.

Specifically, the relative movement unit 4 includes an X-axis slider 41, a Y-axis slider 42, and a rotation mechanism 43.

5 [0029] The X-axis slider 41 is attached onto the apparatus frame 1f, and moves the Y-axis slider 42 in the X-direction at an optional speed and stops the Y-axis slider 42 at an optional position. Specifically, the X-axis slider 41 includes a pair of rails extending in the X-direction, a slider unit moving on these rails, and a slider drive unit configured to move and stop the slider unit. The slider drive unit may include, for example, a combination of a ball
10 screw mechanism with a servo motor or a pulse motor rotated and stopped by signal control made by the control unit CN, and a linear motor mechanism. Moreover, the X-axis slider 41 includes an encoder for detecting the current position and/or movement amount of the slider unit. Note that examples of the encoder may include one configured such that fine recessed and raised portions are formed at predetermined pitches at a linear member called a linear
15 scale, and a rotary encoder configured to detect the rotation angle of a motor for rotating a ball screw.

[0030] The Y-axis slider 42 moves, based on a control signal output from the control unit CN, the rotation mechanism 43 in the Y-direction at an optional speed and stops the rotation mechanism 43 at an optional position. Specifically, the Y-axis slider 42 includes a pair of
20 rails extending in the Y-direction, a slider unit moving on these rails, and a slider drive unit configured to move and stop the slider unit. The slider drive unit may include, for example, a combination of a ball screw mechanism with a servo motor or a pulse motor rotated and stopped by signal control made by the control unit CN, and a linear motor mechanism. Moreover, the Y-axis slider 42 includes an encoder for detecting the current position and/or
25 movement amount of the slider unit. Note that examples of the encoder may include one

configured such that fine recessed and raised portions are formed at predetermined pitches at a linear member called a linear scale, and a rotary encoder configured to detect the rotation angle of a motor for rotating a ball screw.

5 [0031] The rotation mechanism 43 rotates the mount 20 in the θ -direction at an optional speed, and stops the mount 20 at an optional angle. Specifically, examples of the rotation mechanism 43 may include one configured to rotate/stop at an optional angle by signal control made by external equipment, such as a direct drive motor. The mount 20 of the wafer holding unit 2 is attached onto a rotation-side member of the rotation mechanism 43.

10 [0032] Since the relative movement unit 4 has such a configuration, the relative movement unit 4 can move the wafer W at predetermined speed and angle or stop the wafer W at optional position and angle relative to the image capturing unit 3 in the XY θ direction independently or in combination while holding the wafer W targeted for inspection.

[0033] FIG. 2 is a conceptual diagram showing the state of image capturing in one example of the embodied form of the present invention.

15 FIG. 2 shows such a state that while the image capturing camera 35 of the image capturing unit 3 is being moved relative to the wafer W in a direction indicated by an arrow Vs, the image of the inspection target location is captured for the sequentially-changed image capturing locations of the multiple device chips C(2, 2) to C(5, 2) arranged apart from each other on the wafer W. Note that FIG. 2 currently shows such a state that the image of the image capturing region F including the inspection target location of the device chip C(4, 2) is
20 captured by the image capturing camera 35.

[0034] FIG. 3 is a plan view showing a positional relationship among the device chips C in one example of the embodied form of the present invention. FIG. 3 shows an image of arrangement of the repeated visual pattern of the device chips C formed on the wafer W as a
25 certain type of product to be inspected, and as an example, shows such a state that complete

chips C_n formed in an inspection region R_i of the wafer W and incomplete chips C_b formed over the inspection region R_i and a non-inspection region R_n are arranged.

[0035] The chip layout registration unit 5 registers a chip layout for defining positional information on the inspection region R_i and the non-inspection region R_n of the wafer W and
5 arrangement information on the device chips C with respect to the reference posture and position of the wafer W.

[0036] Note that, e.g., the radius position of the outer edge (i.e., a boundary with the non-inspection region R_n) of the inspection region R_i in millimeters (i.e., the positional information) and information on the matrix array, pitch, and offset of the repeated visual
10 pattern of the device chips C (i.e., the arrangement information) are defined as the chip layout, taking the state of a notch W_k of the wafer W facing immediately downward as the reference posture and taking the center of the wafer W in this posture as the reference position (also referred to as an origin) in the XY direction.

[0037] Specifically, the chip layout registration unit 5 registers data for defining the chip
15 layout for each type of product to be inspected.

[0038] The reference image registration unit 6 registers the reference image P_f.

[0039] Note that the reference image P_f shows a reference in a state in which the repeated visual pattern of the device chips C formed on the wafer W is normal. Specifically, the reference image P_f serves as a reference for determining, as compared to the captured
20 inspection image P_k, that the inspection image P_k is normal if, e.g., a brightness value difference or a variance value for each pixel or pixel group is within a preset range and determining that the inspection image P_k is abnormal if such a value is outside the range. More specifically, examples of the reference image P_f may include a single image representing a pre-selected good-quality image, one obtained in such a manner that multiple
25 good-quality images are selected in advance and averaged, and one generated based on a

good-quality product learning method.

[0040] Specifically, the reference image registration unit 6 registers data on the reference image Pf for each type of product to be inspected.

[0041] FIGS. 4(a) to 4(d) are views showing the image Ps, the reference image Pf, the inspection image Pk, and a difference between the inspection image Pk and the reference image Pf in one example of the embodied form of the present invention.

FIG. 4(a) shows, as an example, the captured image Ps of the incomplete chip Cb, and the image Ps includes the circuit pattern and a defect X targeted for detection.

FIG. 4(b) shows, as an example, the reference image Pf.

FIG. 4(c) shows, as an example, the inspection image Pk.

FIG. 4(d) shows, as an example, the difference between the inspection image Pk and the reference image Pf.

Note that as an example, each image Ps, Pf, Pk includes pixels in a matrix of 7×7 . Moreover, a foreign substance adhering onto the circuit pattern is shown as an example of the defect X.

[0042] FIGS. 5(a) to 5(d) are views showing the brightness value of each pixel of the image Ps, the reference image Pf, and the inspection image Pk and a difference in the brightness value between the inspection image Pk and the reference image Pf in one example of the embodied form of the present invention. Note that each image of FIGS. 4(a) to 4(d) is in a positional relationship corresponding to associated ones of the brightness values of the pixels shown in FIGS. 5(a) to 5(d).

FIG. 5(a) shows, as an example, the brightness value of each pixel of the captured image Ps (including the circuit pattern and the defect X targeted for detection) of the incomplete chip Cb.

FIG. 5(b) shows, as an example, the brightness value of each pixel of the reference

image Pf.

FIG. 5(c) shows, as an example, the brightness value of each pixel of the inspection image Pk.

FIG. 5(d) shows, as an example, the difference in the brightness value between the inspection image Pk and the reference image Pf.

[0043] The image processing unit 7 processes the image Ps captured by the image capturing unit 3.

Specifically, the image processing unit 7 includes, for example, a dynamic mask processing unit 71 and a comparison inspection unit 72.

[0044] The dynamic mask processing unit 71 replaces the brightness values of ones, which are the pixels corresponding to the non-inspection region Rn (indicated by a dashed line Y), the pixels forming the captured image Ps of the incomplete chip Cb formed over the inspection region Ri and the non-inspection region Rn, with the brightness values of the reference image Pf based on positional information on the wafer W for which the image Ps has been captured and the chip layout, thereby generating the inspection image Pk.

[0045] Specifically, the relative positions of the wafer W and the image capturing unit 3 when the image Ps is captured are acquired, and by checking such positional information against the chip layout, it is determined whether each pixel in the captured image Ps is a pixel in the inspection region Ri or a pixel in the non-inspection region Rn. Then, the brightness value of each pixel (indicated by the dashed line Y) in the non-inspection region Rn is replaced with the brightness value of the pixel corresponding to that of the reference image Pf, and in this manner, the inspection image Pk is generated. At this point, the brightness value of each pixel (also referred to as an inspection target pixel) which is not in the non-inspection region Rn of the image Ps is taken over to the inspection image Pk. That is, if such an inspection target pixel includes the defect X, a brightness value indicating that an

image with the defect X is captured is reflected on the inspection image Pk.

[0046] The comparison inspection unit 72 compares the inspection image Pk generated by the dynamic mask processing unit 71 with the reference image Pf, thereby inspecting the inspection target location.

5 Specifically, the comparison inspection unit 72 compares the pixels of the inspection image Pk including the inspection target location of the repeated visual pattern of the device chips C with the corresponding pixels of the reference image Pf, thereby determining that the inspection image Pk is normal if, e.g., the brightness value difference or the variance value for each pixel or pixel group is within the preset range and determining that
10 the inspection image Pk is abnormal if such a value is outside the range.

[0047] Thus, the defect X can be detected in such a manner that the processing of comparing the inspection image Pk and the reference image Pf with each other is performed by the comparison inspection unit 72 and the location where the brightness value difference is outside the reference range is extracted.

15 [0048] Note that in addition to the above-described functions, the image processing unit 7 has, as necessary, the functions of connecting divided images, extracting (also referred to as trimming) a location necessary for inspection from an entire image including a margin, correcting the brightness value of each pixel, correcting distortion of the image Ps, and performing arithmetic processing, for example.

20 [0049] The reference image registration unit 6, the chip layout registration unit 5, and the image processing unit 7 according to the present invention are implemented by a computer CP (i.e., hardware) having an image processing function and an execution program thereof (i.e., software).

 More specifically, the chip layout registration unit 5 and the reference image
25 registration unit 6 are implemented by part of the computer CP, such as a storage unit (e.g., a

register or a memory) or a recording medium (e.g., an HDD or an SSD), and the image processing unit 7 is implemented by an image processing unit (a so-called GPU) of the computer CP.

[0050] The computer CP has, for example, the following functions and roles:

5 registration of information (a so-called inspection procedure) on an image capturing magnification, an image capturing position, an image capturing route T, an image capturing interval (a pitch, an interval), a feed rate, etc. for each type of product to be inspected;

registration of inspection conditions (e.g., the normal range of the brightness value or the variance value for the inspection target location) for each type of product to be
10 inspected;

input/output of various types of information via connection with a user interface (e.g., a keyboard, a SW, or a monitor); and

input/output of signals and data via connection with the control unit CN or an external host computer.

15 Note that the inspection procedure and the inspection conditions for each type of product to be inspected are also referred to as recipe information or an inspection recipe.

[0051] The control unit CN has, for example, the following functions and roles:

output of a signal for holding/releasing the wafer W to the wafer holding unit 2;

control of the revolver mechanism 34 for switching the objective lens (the image
20 capturing magnification) to be used;

output of a light emission trigger to the illumination unit 31;

output of an image capturing trigger to the image capturing camera 35;

drive control of the relative movement unit 4: outputting a drive signal while
monitoring the current positions of the X-axis slider 41, the Y-axis slider 42, and the rotation
25 mechanism 43;

output of current positional information on the relative movement unit 4 (the X-axis slider 41, the Y-axis slider 42, and the rotation mechanism 43) to the computer CP; and

control of each unit based on the inspection recipe.

[0052] Note that output of the image capturing trigger from the control unit CN to the
5 image capturing unit 3 includes the following techniques as examples:

the technique of emitting the illumination light L1 for an extremely-short period of time (so-called electronic flash) in every movement by a predetermined distance during scanning in the X-direction; and

the technique of capturing an image by irradiation with the illumination light L1
10 after movement to and stop at a predetermined position (a so-called step-and-repeat technique).

[0053] The image capturing trigger means an image intake instruction or an illumination light L1 emission instruction for the image capturing camera 35 or the image processing unit 7, for example. Specifically, as the image capturing trigger, (Case 1) the illumination light
15 L1 is electronically flashed during such a time (a so-called exposure time) that an image can be captured by the image capturing camera 35, or (Case 2) an image is captured within the time of irradiation with the illumination light L1. Alternatively, the image capturing trigger is not limited to the instruction for the image capturing camera 35, and may be (Case 3) an image intake instruction for an image processing apparatus for acquiring an image. This
20 configuration is also adoptable to a form in which a video signal or video data is sequentially output from the image capturing camera 35.

[0054] More specifically, the control unit CN is implemented by a computer or a programmable logic controller (i.e., hardware) and an execution program thereof (i.e., software), for example.

25 [0055] [Inspection Flow]

FIG. 6 is a flowchart in one example of the embodied form of the present invention.

FIG. 6 shows, as a series of flow, each step of capturing the images of the inspection region Ri and the non-inspection region Rn of the device chip C arranged on the wafer W and inspecting these images by means of the wafer visual inspection apparatus 1.

5 [0056] In advance of inspection, the chip layout for defining the inspection region Ri and the non-inspection region Rn of the wafer W with respect to the reference posture and position of the wafer W is registered in advance (a step s11), and the reference image Pf is registered in advance (a step s12).

In addition, the inspection recipe is set, and the mode and order of inspection of the
10 wafer W are determined (a step s13).

[0057] Next, the wafer W is placed on the mount 20 of the wafer visual inspection apparatus 1 (a step s21), and is moved to a position, at which a reference mark (not shown) formed on the wafer W is read, and is aligned (a step s22).

[0058] While the wafer W and the image capturing unit 3 are being moved relative to each
15 other, the image Ps including the inspection target location is captured (a step s23), and the subsequent processing is performed for the captured image Ps.

[0059] First, for the captured image Ps of the incomplete chip Cb formed over the inspection region Ri and the non-inspection region Rn, the brightness values of ones, which are the pixels corresponding to the non-inspection region Rn, of the pixels forming the image
20 Ps are replaced with the brightness values of the reference image Pf based on the positional information on the wafer W for which the image Ps has been captured and the chip layout. In this manner, the inspection image Pk is generated (a step s31).

[0060] Then, the inspection target location is inspected by comparison between the inspection image Pk and the reference image Pf (a step s32). Specifically, the corresponding
25 pixels of the inspection image Pk and the reference image Pf are compared with each other,

and it is determined that the inspection image P_k is normal if, e.g., the brightness value difference or the variance value for each pixel or pixel group is within the preset range and it is determined that the inspection image P_k is abnormal if such a value is outside the range. Then, the location where the brightness value difference is outside the reference range is extracted, and the defect X is detected accordingly.

[0061] Then, it is determined whether or not image capturing/inspection has completed for the entirety of the preset inspection target location (a step s41). If not completed yet, image capturing/inspection is continued. On the other hand, if image capturing/inspection has completed, the wafer W is fed out of the apparatus (a step s42).

[0062] Then, it is determined whether or not there is a next wafer W (a step s43). If there is the next wafer W to be inspected, the above-described steps s21 to s43 are repeated. On the other hand, if there is no next wafer W , a series of flow ends.

[0063] According to the wafer visual inspection apparatus 1 and the inspection method of the present invention, even if there is, on the wafer W , the incomplete chip C_b formed over the inspection region R_i and the non-inspection region R_n , the inspection image P_k can be generated by the dynamic mask processing according to the image capturing position, and the desired inspection can be performed by comparison between the inspection image P_k and the reference image P_f . At this point, if the incomplete chip C_b is in the inspection region R_i of the wafer W , inspection according to the complete chip C_n can be performed even for such an incomplete chip C_b , and a desired inspection result for the entirety of the inspection region R_i of the wafer W can be obtained. Moreover, special processing for a false defect does not need to be performed. That is, regardless of whether the device chip C is the complete chip C_n or the incomplete chip C_b , the desired inspection result for the entirety of the inspection region R_i of the wafer W can be obtained, and an increase in a processing time can be prevented.

[0064] [Variations]

Note that the configuration/procedure for detecting the defect X as the foreign substance adhering onto the circuit pattern has been described as a specific example of inspection. However, for embodying the present invention, it may only be required that not only adherence of the foreign substance targeted for inspection but also items such as the presence of short-circuit or disconnection and the presence of a scratch are determined as necessary and image capturing conditions, the inspection conditions, etc. are determined.

Note that as the steps of embodying the present invention, the registration/setting steps have been, as an example, described above with reference to FIG. 6 in the order of registration of the chip layout (the step s11), registration of the reference image Pf (the step s12), and setting of the inspection recipe (the step s13). However, these steps may be executed in a different order. For example, registration of the reference image Pf may be performed before registration of the chip layout, or setting of the inspection recipe may be performed before registration of the chip layout.

[0065] Note that the example where the image capturing area of the image capturing camera 35 of the image capturing unit 3 is set to the image capturing region F including the inspection target location of one device chip C has been described above. However, the image capturing area of the image capturing camera 35 may be set to divided inspection target locations of each device chip C or a wide area including the inspection target locations of multiple ones of the device chips C.

DESCRIPTION OF REFERENCE CHARACTERS

[0066]

- | | |
|----|-----------------------------------|
| 1 | Wafer Visual Inspection Apparatus |
| 25 | 2 Wafer Holding Unit |

	3	Image Capturing Unit
	4	Relative Movement Unit
	5	Chip Layout Registration Unit
	6	Reference Image Registration Unit
5	7	Image Processing Unit
	1f	Apparatus Frame
	20	Mount
	30	Lens Barrel
	31	Illumination Unit
10	32	Half Mirror
	33a, 33b	Objective Lens
	34	Revolver Mechanism
	35	Image Capturing Camera
	41	X-Axis Slider
15	42	Y-Axis Slider
	43	Rotation Mechanism
	71	Dynamic Mask Processing Unit
	72	Comparison Inspection Unit
	CN	Control Unit
20	W	Wafer
	C	Device Chip
	Cn	Complete Chip
	Cb	Incomplete Chip
	F	Image Capturing Region (Field of View)
25	Ri	Inspection Region

	Rn	Non-Inspection Region
	Ps	Inspection Image (Pre-Processed)
	Pk	Inspection Image (Post-Processed)
	Pf	Reference Image
5	L1	Illumination Light
	L2	Light Having Entered from Wafer Side (Reflected Light, Scattered Light)
	T	Image Capturing Route

CLAIMS

1. A wafer visual inspection apparatus for capturing an image of an inspection target location of a repeated visual pattern of a device chip formed on a wafer to inspect the device chip by comparison with a reference image, comprising:
- a wafer holding unit configured to hold the wafer;
 - an image capturing unit configured to capture an image including the inspection target location;
 - a relative movement unit configured to move the wafer holding unit and the image capturing unit relative to each other;
 - a chip layout registration unit configured to register a chip layout for defining positional information on an inspection region and a non-inspection region of the wafer and arrangement information on the device chip with respect to reference posture and position of the wafer;
 - a reference image registration unit configured to register the reference image; and
 - an image processing unit configured to process the image captured by the image capturing unit,
- wherein the image processing unit includes
- a dynamic mask processing unit configured to replace a brightness value of at least one, which is a pixel corresponding to the non-inspection region, of pixels forming a captured image of an inspection target location of an incomplete chip formed over the inspection region and the non-inspection region, with a brightness value of the reference image based on positional information on the wafer for which the image has been captured and the chip layout, thereby generating an inspection image, and
 - a comparison inspection unit configured to compare the inspection image

generated by the dynamic mask processing unit with the reference image, thereby inspecting the inspection target location.

2. A wafer visual inspection method for capturing an image of an inspection
5 target location of a repeated visual pattern of a device chip formed on a wafer to inspect the device chip by comparison with a reference image, comprising:

registering, in advance, a chip layout for defining an inspection region and a non-inspection region of the wafer with respect to reference posture and position of the wafer;

registering the reference image in advance;

10 capturing an image including the inspection target location while moving the wafer and an image capturing section relative to each other; and

processing the image,

wherein the processing the image includes

replacing a brightness value of at least one, which is a pixel
15 corresponding to the non-inspection region, of pixels forming a captured image of an incomplete chip formed over the inspection region and the non-inspection region, with a brightness value of the reference image based on positional information on the wafer for which the image has been captured and the chip layout, thereby generating an inspection image, and

20 comparing the inspection image with the reference image, thereby inspecting the inspection target location.