

WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:
  - a substrate;
  - a plurality of memory cell transistors vertically stacked on the substrate;
  - a first conductive line connected to a source region of at least one of the plurality of memory cell transistors;
  - a second conductive line connected to a plurality of gate electrodes of the plurality of memory cell transistors; and
  - a data storage element connected to a drain region of the at least one of the plurality of memory cell transistors,
    - wherein the data storage element comprises a first electrode that extends horizontally from the drain region in a first direction parallel to a top surface of the substrate,
    - wherein a first one of the first conductive line or the second conductive line extends horizontally in a second direction that intersects the first direction, and
    - wherein a second one of the first conductive line or the second conductive line extends vertically in a third direction that is perpendicular to the top surface of the substrate.
2. The semiconductor memory device of claim 1,
  - wherein the at least one of the plurality of memory cell transistors comprises a semiconductor pattern comprising the source region, the drain region, and a channel region that is between the source region and the drain region, and
  - wherein the semiconductor pattern extends from the first conductive line in the first direction.
3. The semiconductor memory device of claim 2,
  - wherein the semiconductor pattern and the first electrode comprise respective surfaces that are coplanar, and
  - wherein the semiconductor pattern and the first electrode comprise respective extension axes that are parallel to the first direction and are coaxial.
4. The semiconductor memory device of claim 1, wherein the second conductive line defines a perimeter around a plurality of channel regions of the plurality of memory cell

transistors.

5. The semiconductor memory device of claim 1,  
wherein the data storage element comprises a first capacitor that is adjacent the second  
conductive line,

wherein the first capacitor comprises the first electrode and further comprises:

a dielectric layer on the first electrode; and

a second electrode on the dielectric layer, and

wherein the semiconductor memory device further comprises a second capacitor that  
is adjacent the second conductive line and that overlaps the first capacitor in the third direction.

6. The semiconductor memory device of claim 1,  
wherein the first electrode comprises a first end portion that is adjacent and connected  
to the drain region,

wherein the first electrode further comprises a second end portion that is opposite the  
first end portion, and

wherein an axis that extends through the first end portion and the second end portion  
is parallel to the first direction.

7. The semiconductor memory device of claim 6, further comprising a first  
supporting layer that is connected to the second end portion of the first electrode and is  
configured to structurally support the first electrode.

8. The semiconductor memory device of claim 7, further comprising a second  
supporting layer that is between the first end portion and the second end portion of the first  
electrode and is configured to structurally support the first electrode.

9. The semiconductor memory device of claim 1, further comprising a back-gate  
line that is adjacent a plurality of channel regions of the plurality of memory cell transistors  
and that extends in parallel with the second conductive line.

10. A semiconductor memory device comprising:  
a substrate;

a vertical stack comprising a plurality of layers on the substrate; and  
a first conductive line that is penetrated by the vertical stack and that extends in a vertical direction perpendicular to a top surface of the substrate,  
wherein each of the plurality of layers of the vertical stack comprises:  
a first extended portion that extends horizontally in a first direction parallel to the top surface of the substrate; and  
a second extended portion that extends horizontally from the first extended portion in a second direction parallel to the top surface of the substrate and crossing the first direction,  
wherein the first extended portion comprises a second conductive line,  
wherein the second extended portion comprises a semiconductor pattern and an electrode that is connected to the semiconductor pattern,  
wherein the semiconductor pattern is between the second conductive line and the electrode, and  
wherein the first conductive line is on a top surface and a bottom surface of the semiconductor pattern.

11. The semiconductor memory device of claim 10,  
wherein the semiconductor pattern comprises a first impurity region, a second impurity region, and a channel region that is between the first impurity region and the second impurity region,  
wherein the second conductive line is connected to the first impurity region, and  
wherein the electrode is connected to the second impurity region.

12. The semiconductor memory device of claim 10,  
wherein, in each of the plurality of layers in the vertical stack, the second extended portion comprises one among a plurality of second extended portions,  
wherein the plurality of second extended portions are connected in common to the first extended portion, and  
wherein the plurality of second extended portions are spaced apart from each other in the first direction.

13. The semiconductor memory device of claim 10, further comprising a supporting layer that is configured to structurally support the plurality of layers,

wherein the electrode comprises a first electrode of a capacitor,  
wherein the capacitor further comprises:  
    a dielectric layer on the first electrode; and  
    a second electrode on the dielectric layer, and  
wherein the first conductive line is on opposite side surfaces of the semiconductor  
pattern.