FIG. 1

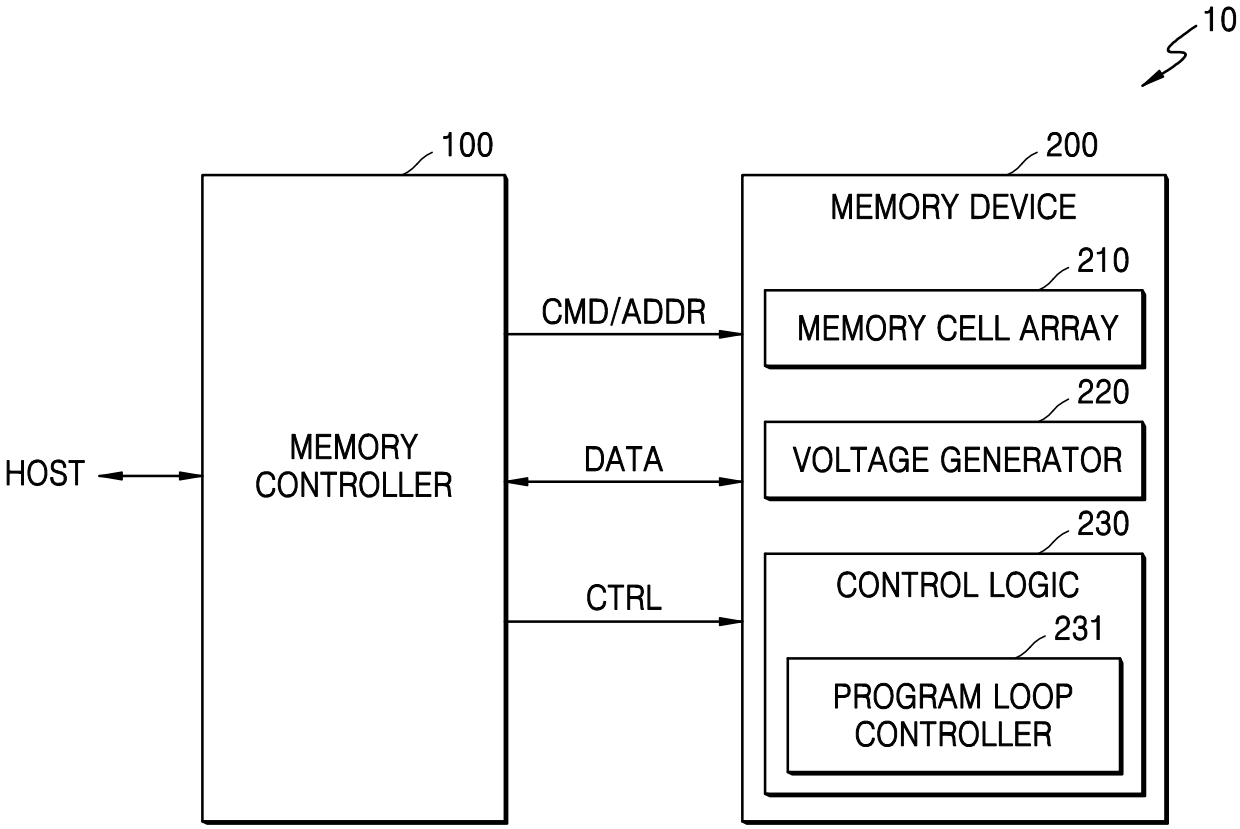

10
100
200
MEMORY DEVICE
210
MEMORY CELL ARRAY
220
VOLTAGE GENERATOR
230
CONTROL LOGIC
231
PROGRAM LOOP CONTROLLER
HOST
MEMORY CONTROLLER
CMD/ADDR
DATA
CTRL

FIG. 2

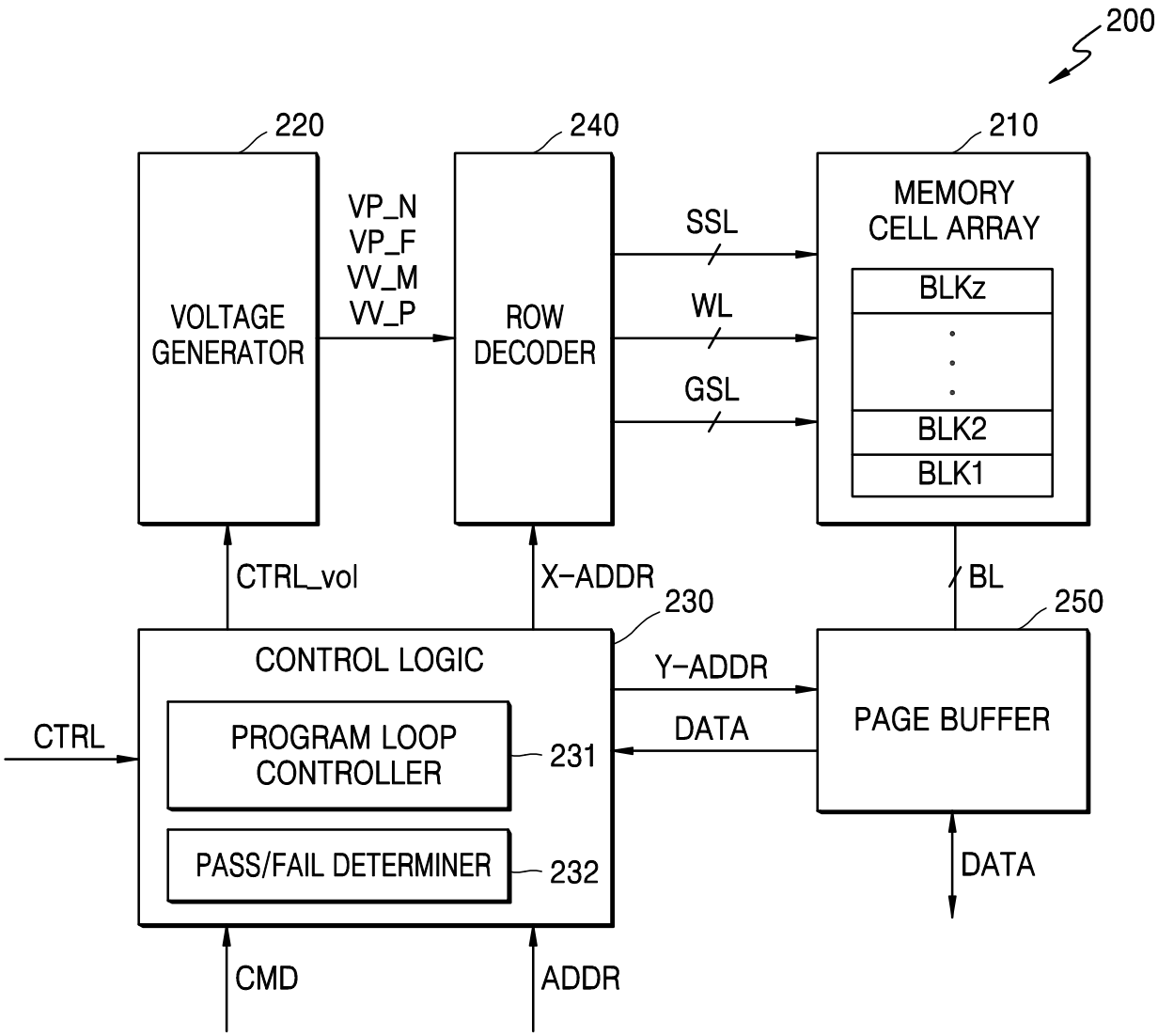

200
220
240
210
VOLTAGE GENERATOR
VP_N
VP_F
VV_M
VV_P
ROW DECODER
SSL
WL
GSL
MEMORY CELL ARRAY
BLKz
BLK2
BLK1
CTRL_vol
X-ADDR
BL
230
250
CONTROL LOGIC
Y-ADDR
DATA
PAGE BUFFER
CTRL
PROGRAM LOOP CONTROLLER
231
PASS/FAIL DETERMINER
232
DATA
CMD
ADDR

FIG. 3

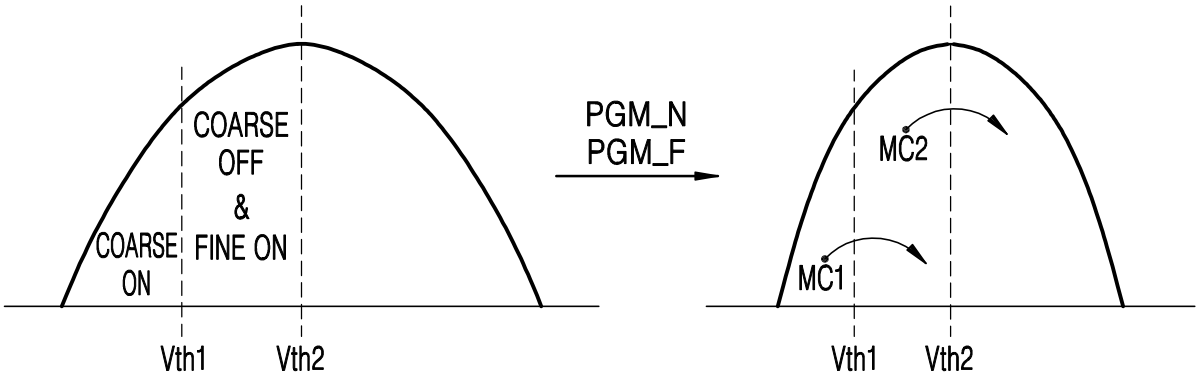

COARSE
ON
COARSE
OFF
&
FINE ON
Vth1
Vth2
PGM_N
PGM_F
MC1
MC2
Vth1
Vth2

FIG. 4

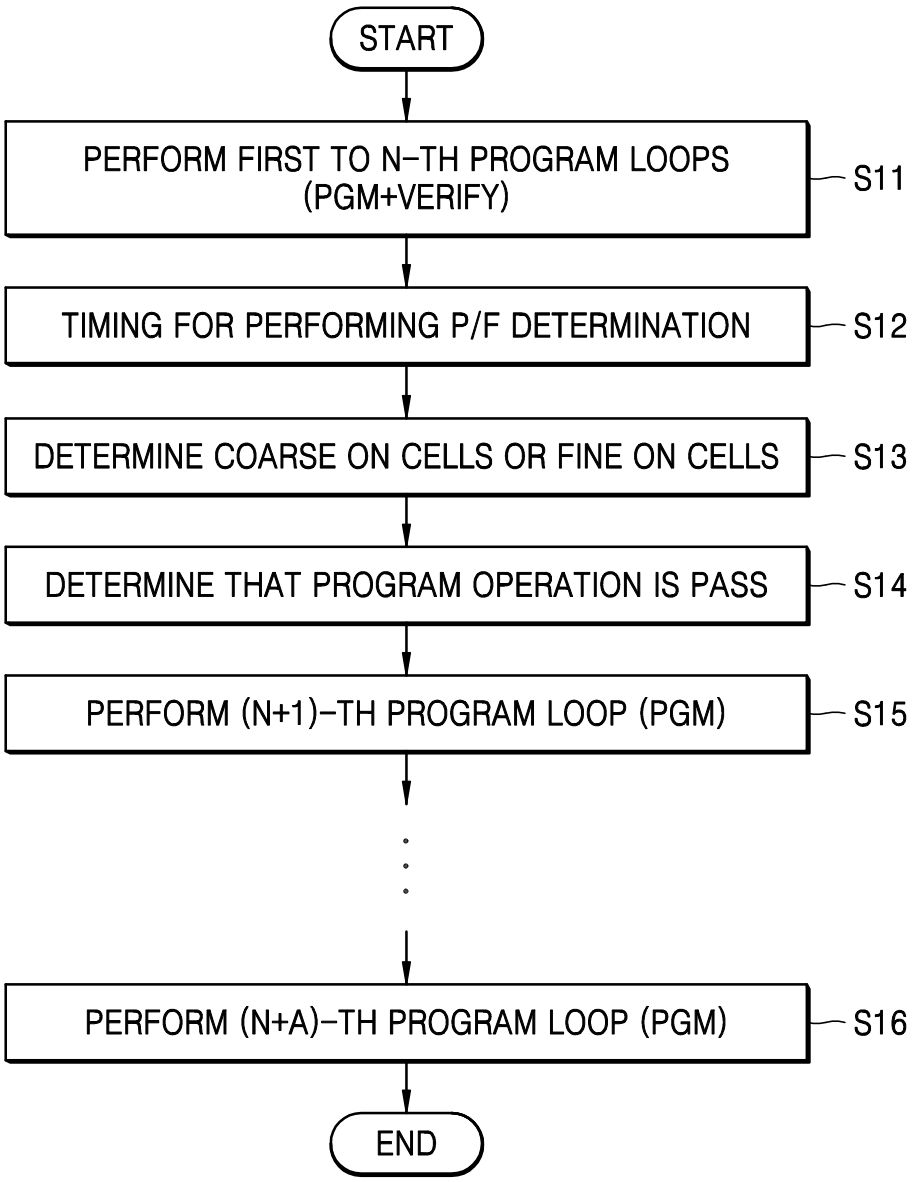

START
PERFORM FIRST TO N-TH PROGRAM LOOPS (PGM+VERIFY)
S11
TIMING FOR PERFORMING P/F DETERMINATION
S12
DETERMINE COARSE ON CELLS OR FINE ON CELLS
S13
DETERMINE THAT PROGRAM OPERATION IS PASS
S14
PERFORM (N+1)-TH PROGRAM LOOP (PGM)
S15
PERFORM (N+A)-TH PROGRAM LOOP (PGM)
S16
END

FIG. 5

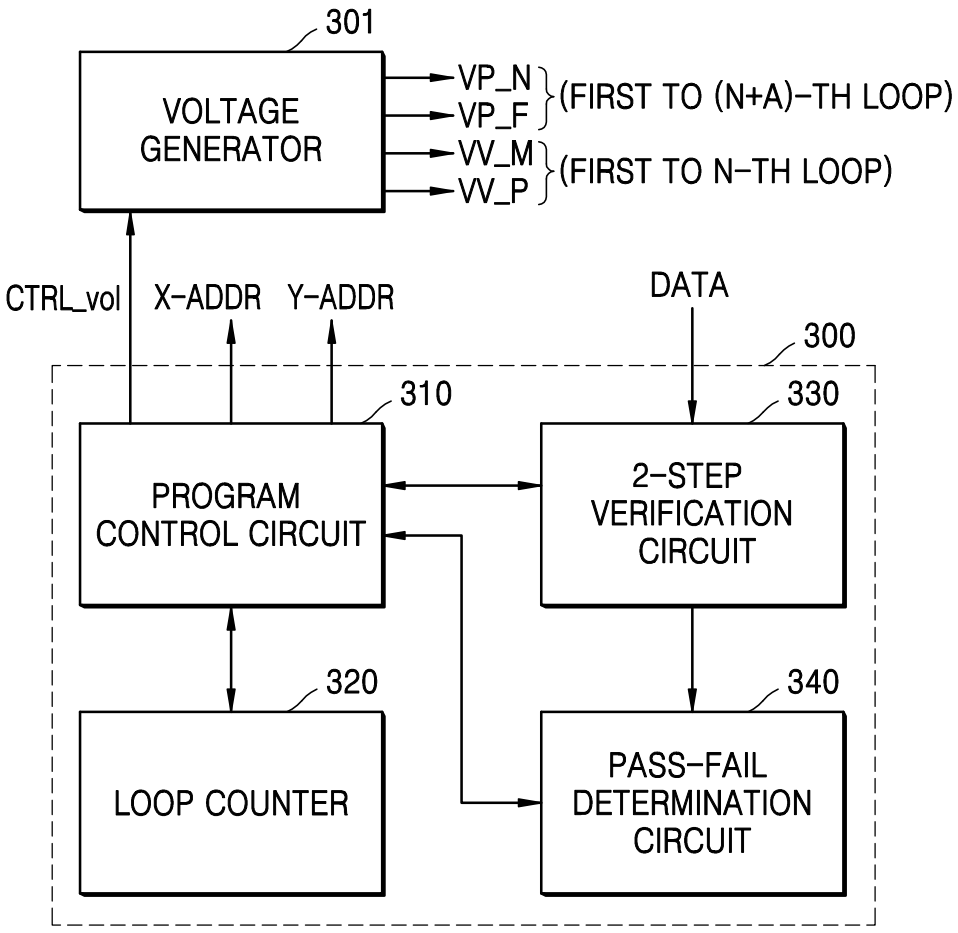

301
VOLTAGE GENERATOR
VP_N
VP_F
(FIRST TO (N+A)-TH LOOP)
VV_M
VV_P
(FIRST TO N-TH LOOP)
CTRL_vol
X-ADDR
Y-ADDR
DATA
300
310
330
PROGRAM CONTROL CIRCUIT
2-STEP VERIFICATION CIRCUIT
320
340
LOOP COUNTER
PASS-FAIL DETERMINATION CIRCUIT

FIG. 6

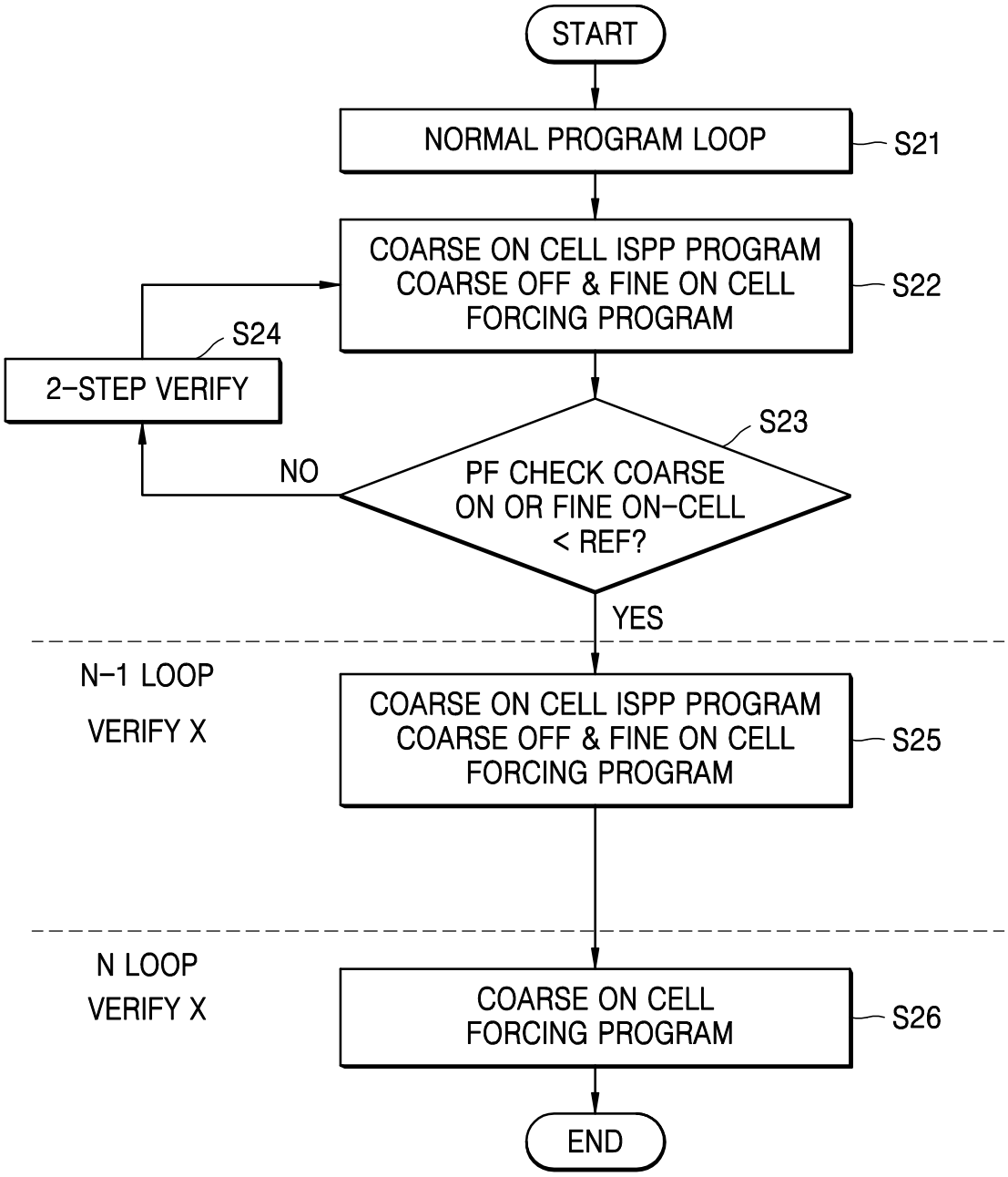

START
NORMAL PROGRAM LOOP
S21
COARSE ON CELL ISPP PROGRAM
COARSE OFF & FINE ON CELL
FORCING PROGRAM
S22
S24
2-STEP VERIFY
S23
NO
PF CHECK COARSE
ON OR FINE ON-CELL
< REF?
YES
N-1 LOOP
VERIFY X
COARSE ON CELL ISPP PROGRAM
COARSE OFF & FINE ON CELL
FORCING PROGRAM
S25
N LOOP
VERIFY X
COARSE ON CELL
FORCING PROGRAM
S26
END

FIG. 7A

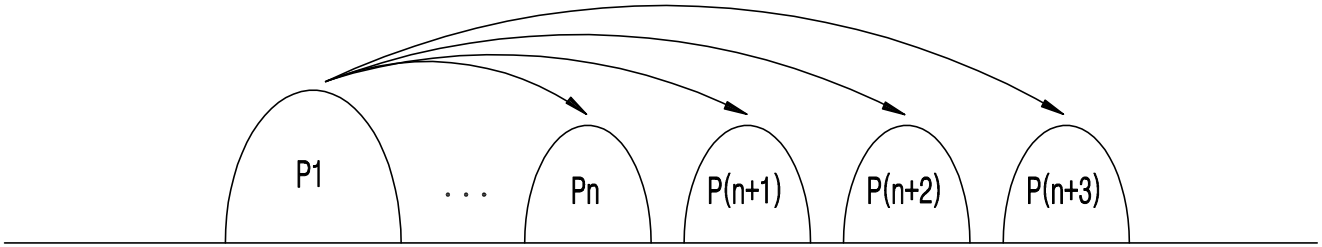


FIG. 7B

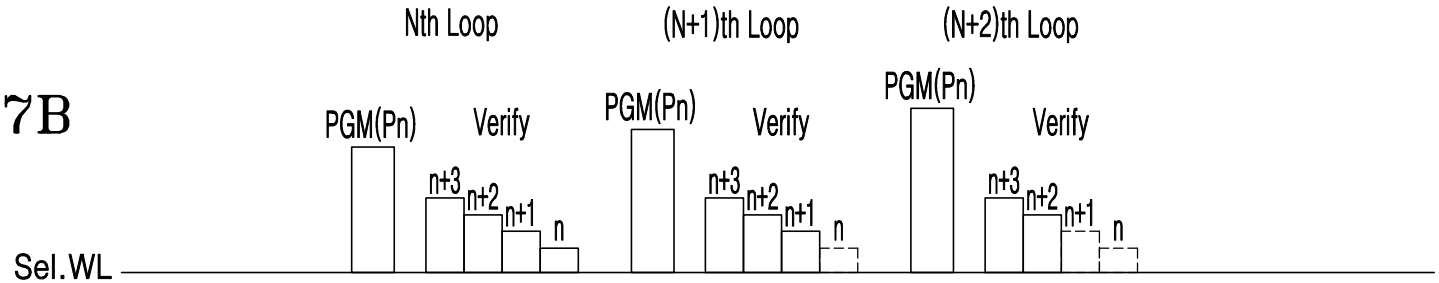


FIG. 7C

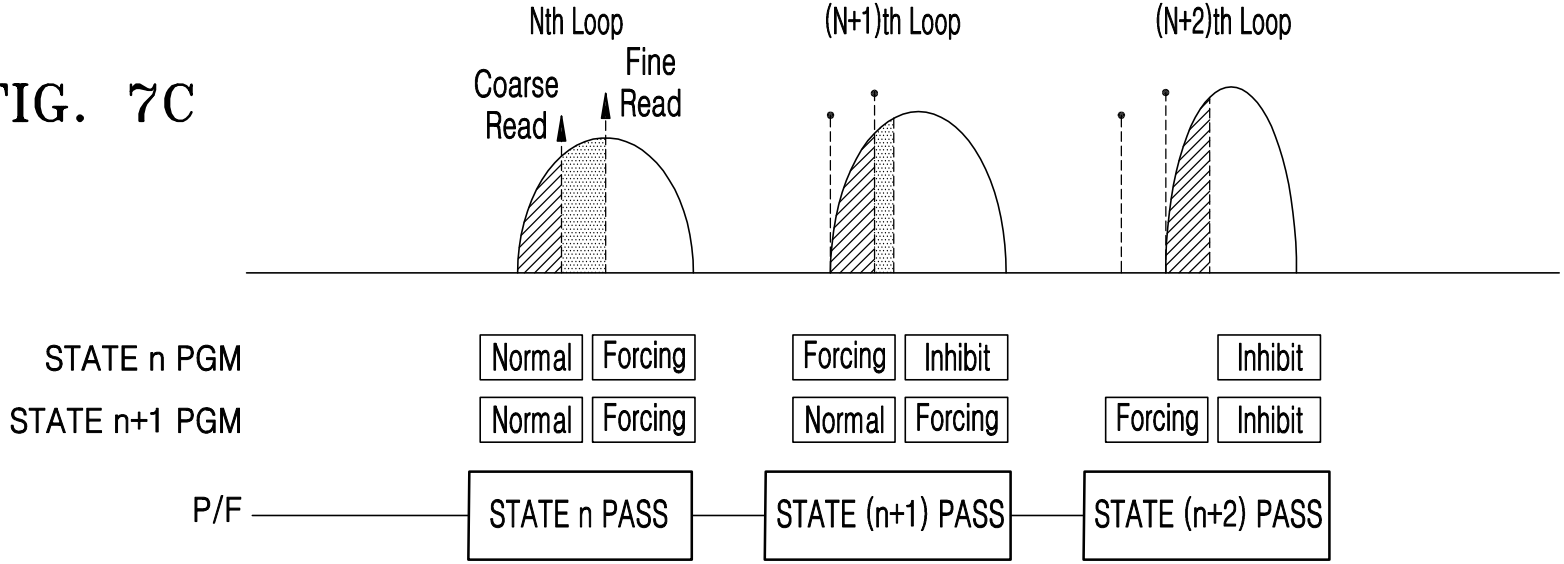


FIG. 8

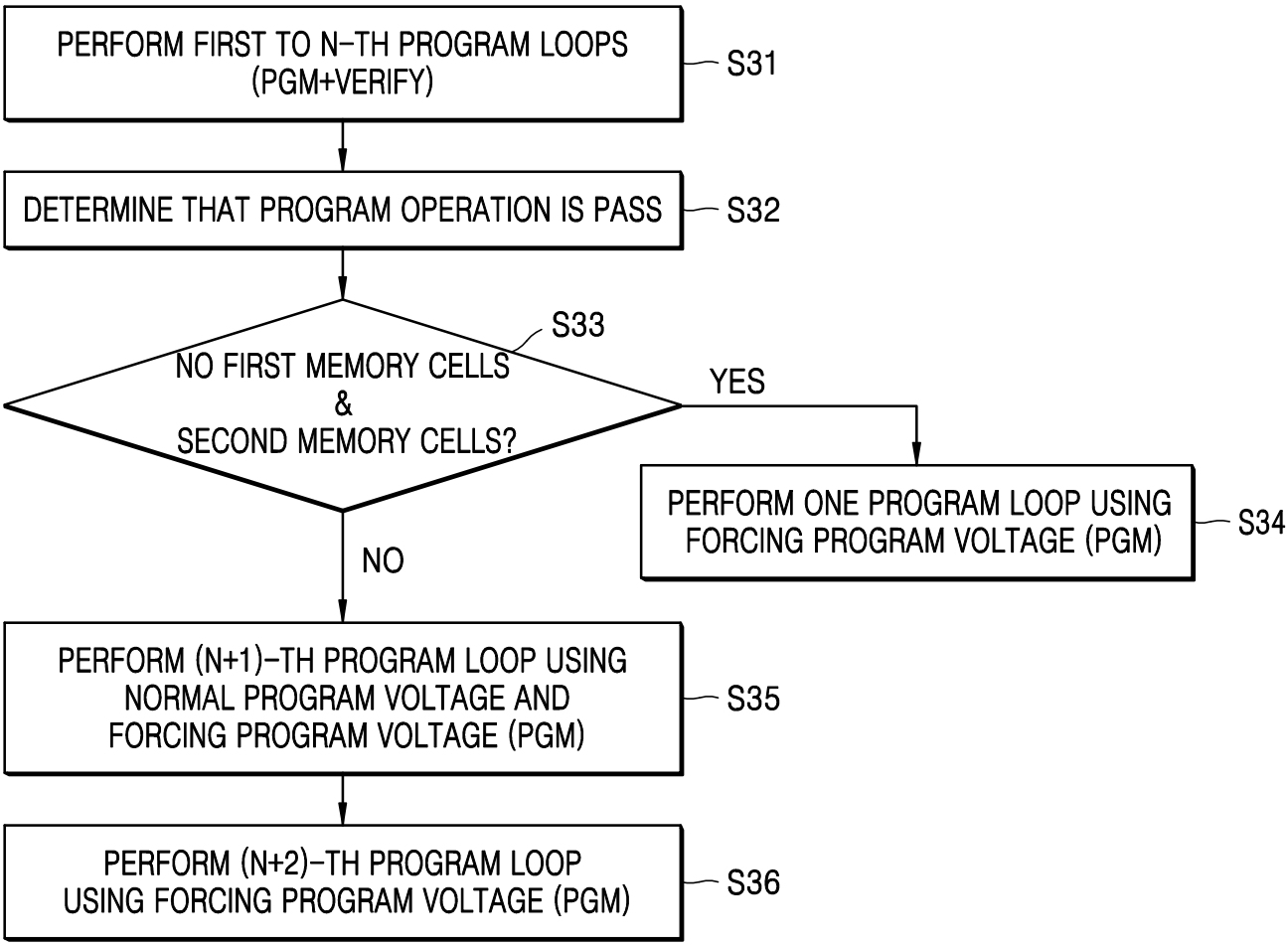

PERFORM FIRST TO N-TH PROGRAM LOOPS (PGM+VERIFY)
S31
DETERMINE THAT PROGRAM OPERATION IS PASS
S32
S33
NO FIRST MEMORY CELLS & SECOND MEMORY CELLS?
YES
PERFORM ONE PROGRAM LOOP USING FORCING PROGRAM VOLTAGE (PGM)
S34
NO
PERFORM (N+1)-TH PROGRAM LOOP USING NORMAL PROGRAM VOLTAGE AND FORCING PROGRAM VOLTAGE (PGM)
S35
PERFORM (N+2)-TH PROGRAM LOOP USING FORCING PROGRAM VOLTAGE (PGM)
S36

FIG. 9A

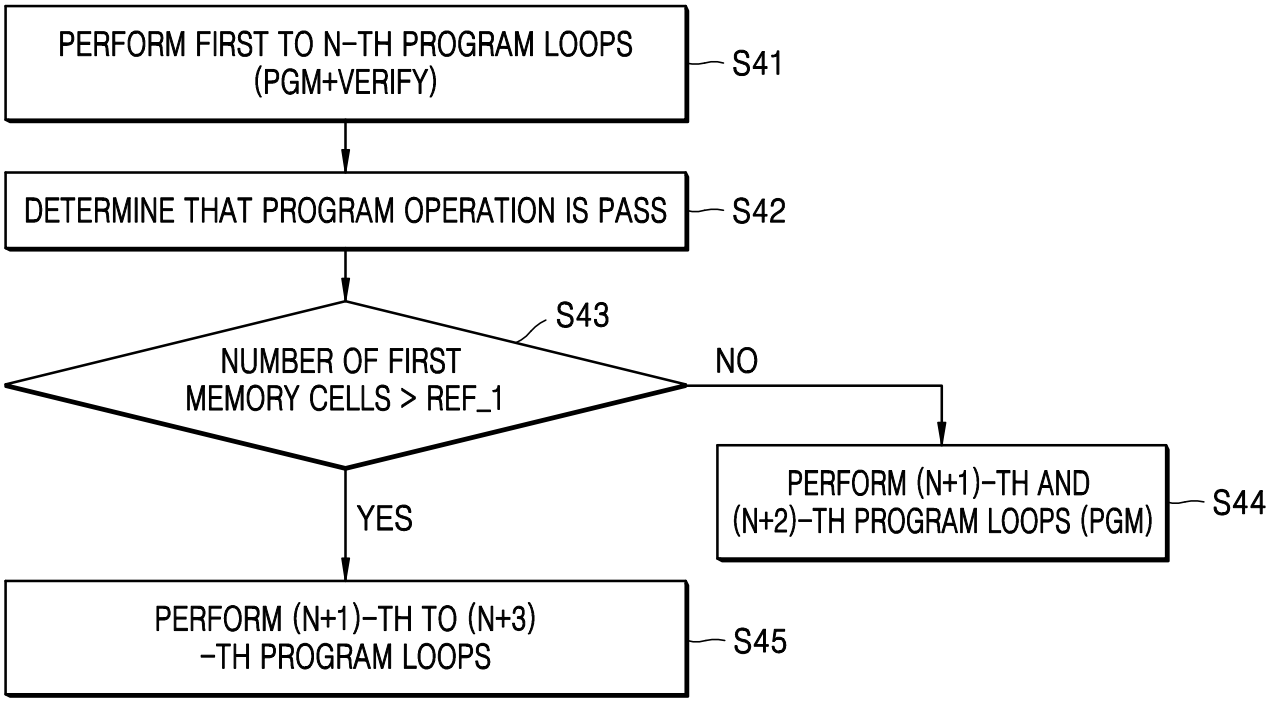

PERFORM FIRST TO N-TH PROGRAM LOOPS (PGM+VERIFY)
S41
DETERMINE THAT PROGRAM OPERATION IS PASS
S42
S43
NUMBER OF FIRST MEMORY CELLS > REF_1
NO
YES
PERFORM (N+1)-TH AND (N+2)-TH PROGRAM LOOPS (PGM)
S44
PERFORM (N+1)-TH TO (N+3) -TH PROGRAM LOOPS
S45

FIG. 9B

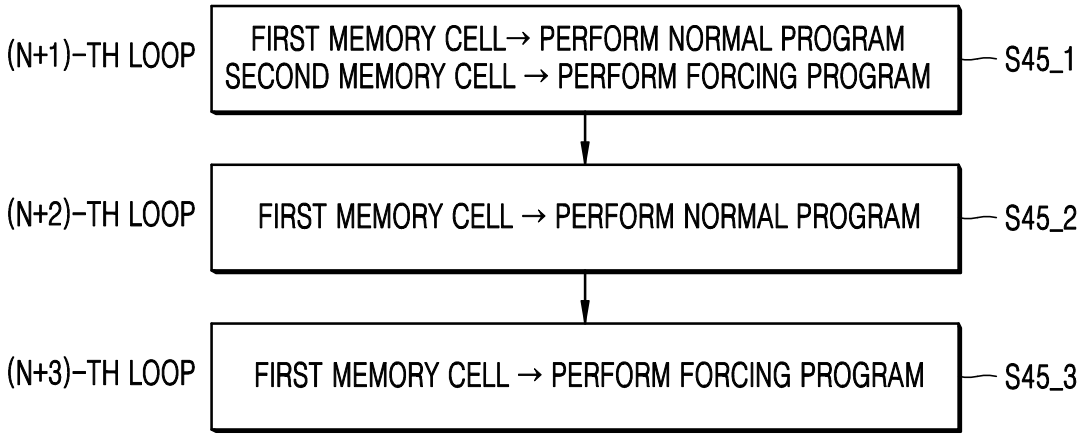

(N+1)-TH LOOP
FIRST MEMORY CELL→ PERFORM NORMAL PROGRAM
SECOND MEMORY CELL → PERFORM FORCING PROGRAM
S45_1
(N+2)-TH LOOP
FIRST MEMORY CELL → PERFORM NORMAL PROGRAM
S45_2
(N+3)-TH LOOP
FIRST MEMORY CELL → PERFORM FORCING PROGRAM
S45_3

FIG. 10

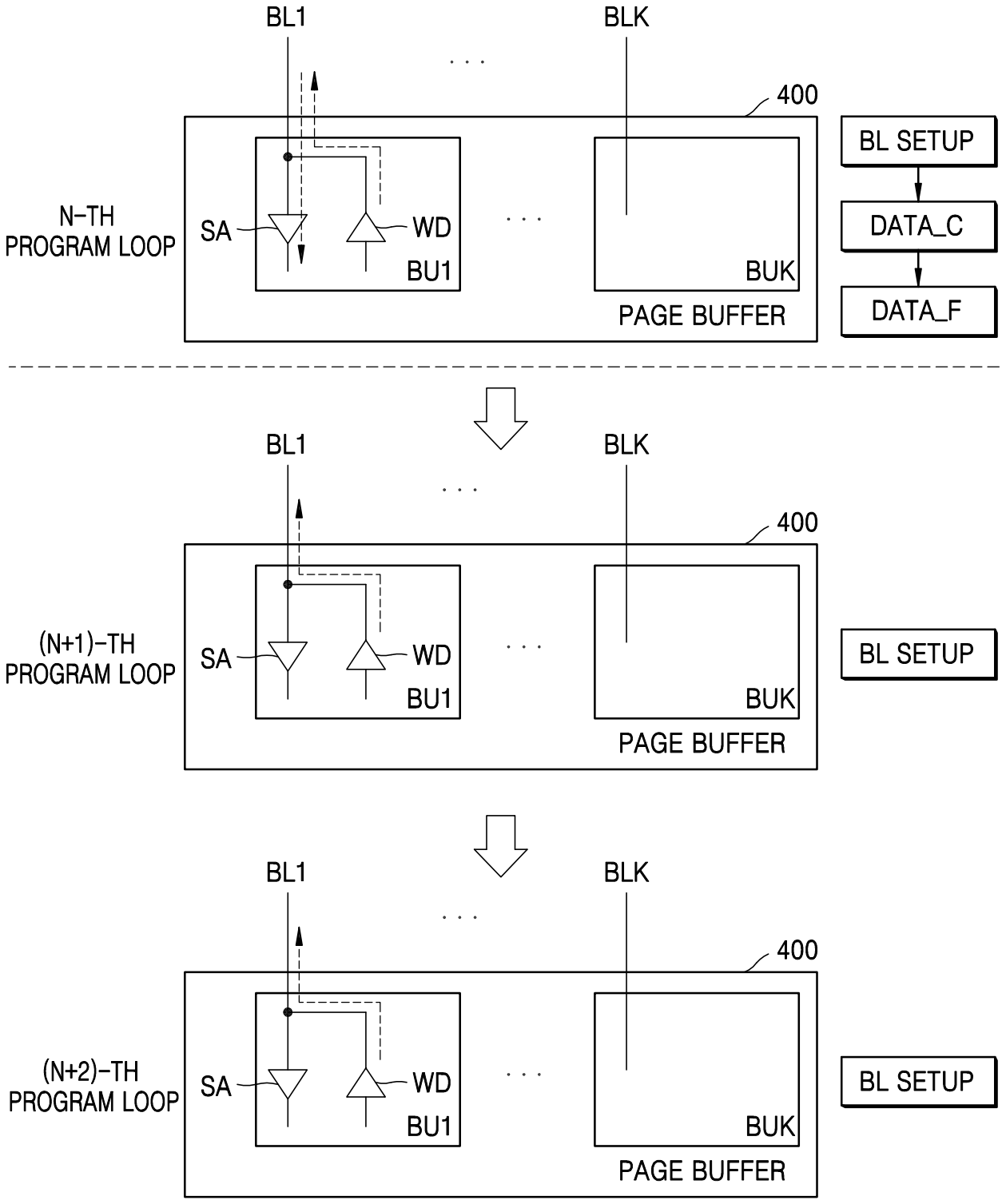

BL1
BLK
400
N-TH
PROGRAM LOOP
SA
WD
BU1
BUK
PAGE BUFFER
BL SETUP
DATA_C
DATA_F
(N+1)-TH
PROGRAM LOOP
BL SETUP
(N+2)-TH
PROGRAM LOOP
BL SETUP

FIG. 11

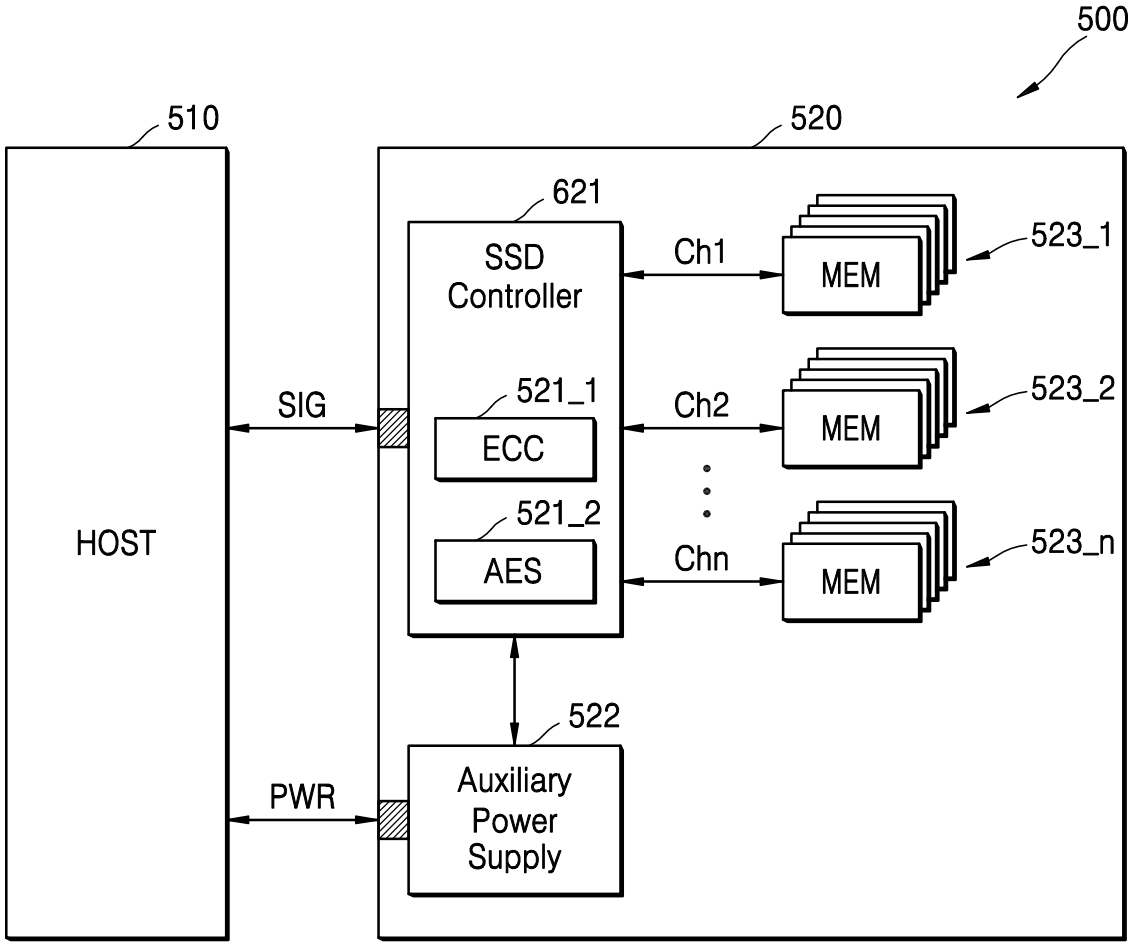

500
510
520
621
SSD
Controller
Ch1
MEM
523_1
521_1
ECC
Ch2
MEM
523_2
SIG
HOST
521_2
AES
Chn
MEM
523_n
522
Auxiliary
Power
Supply
PWR

FIG. 12

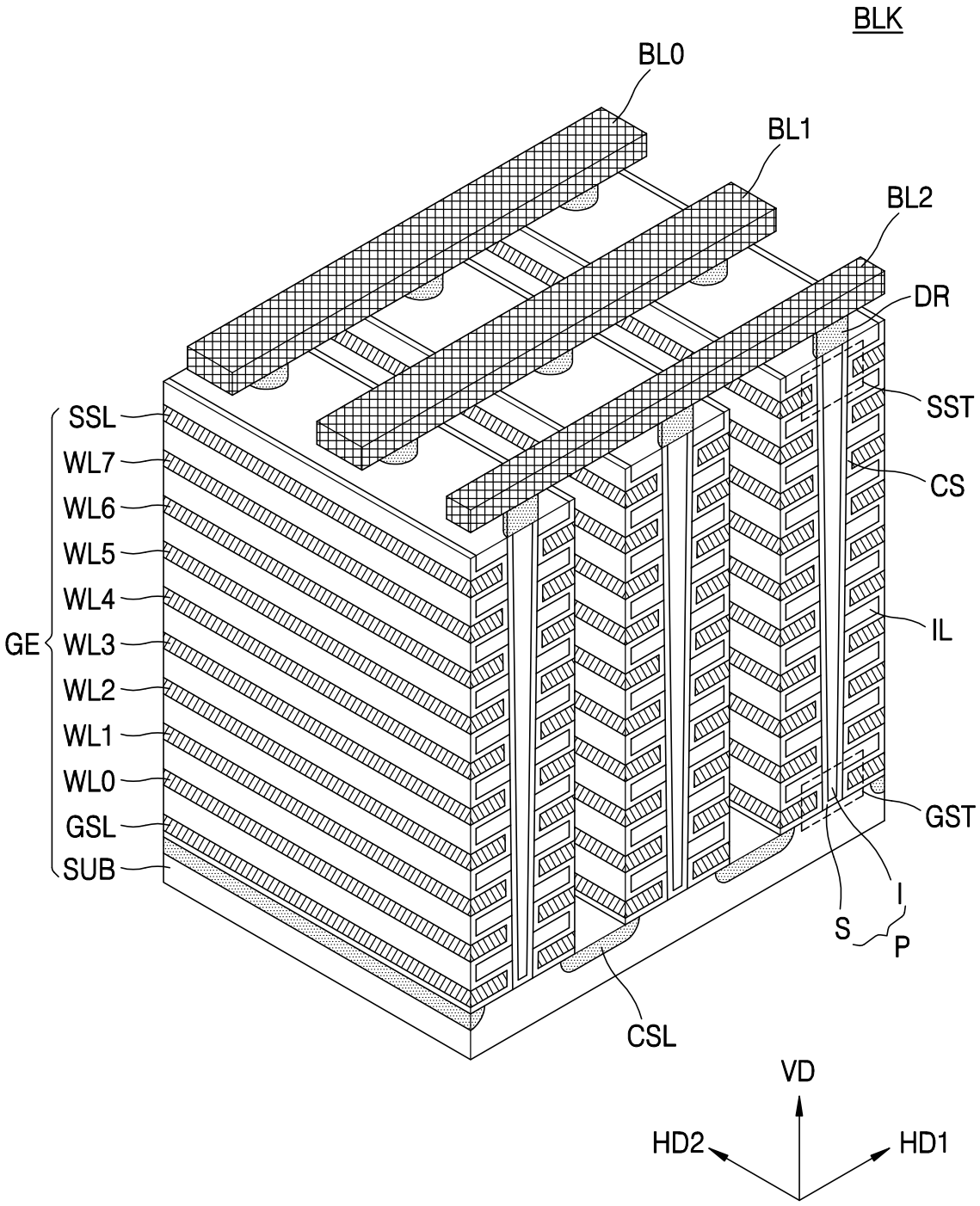
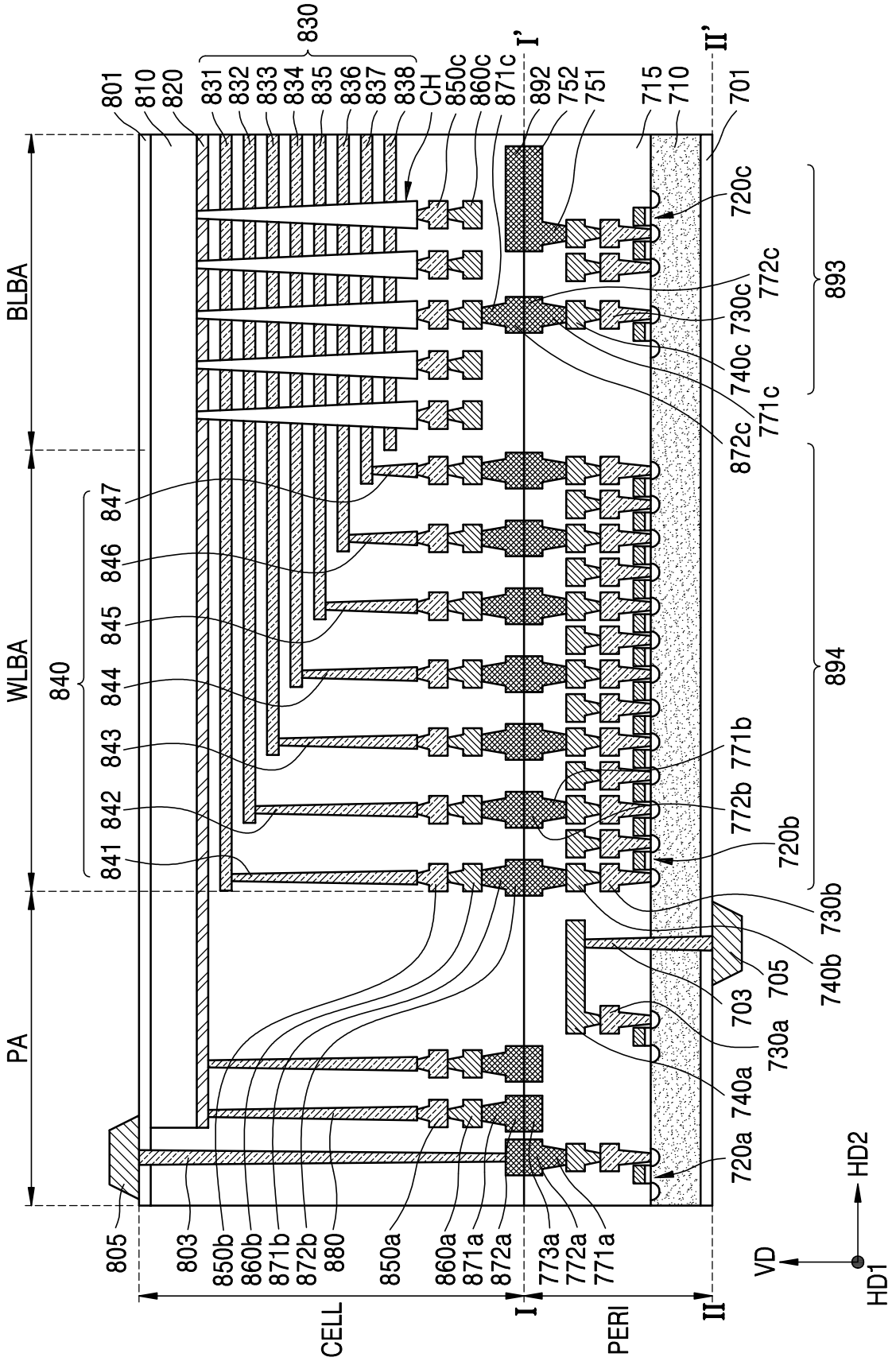

BLK
BL0
BL1
BL2
DR
SST
CS
IL
GST
I
S
P
CSL
SSL
WL7
WL6
WL5
WL4
WL3
WL2
WL1
WL0
GSL
SUB
GE
VD
HD2
HD1

FIG. 13


600
BLBA
WLBA
PA
CELL
PERI
I
I'
II
II'
801
810
820
830
831
832
833
834
835
836
837
838
CH
850c
860c
871c
892
752
751
715
710
701
720c
772c
730c
740c
771c
872c
893
847
846
845
844
843
842
841
840
894
771b
772b
720b
730b
740b
705
703
730a
740a
720a
805
803
850b
860b
871b
872b
880
850a
860a
871a
872a
773a
772a
771a
VD
HD1
HD2