

S101

When a semiconductor memory is in a preset test mode, if a Data Mask Pin (DM) is selected as a test object, control the impedance of the DM to be a first impedance parameter through a first Model Register (MR); or, if the DM is not the test object, control the impedance of the DM to be a second impedance parameter through a second MR

FIG. 1

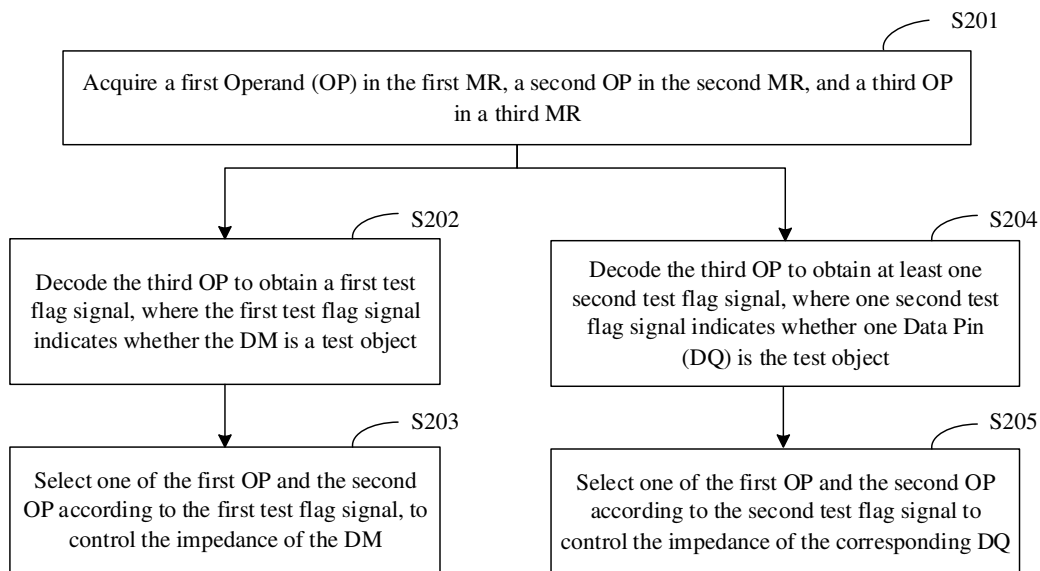


FIG. 2

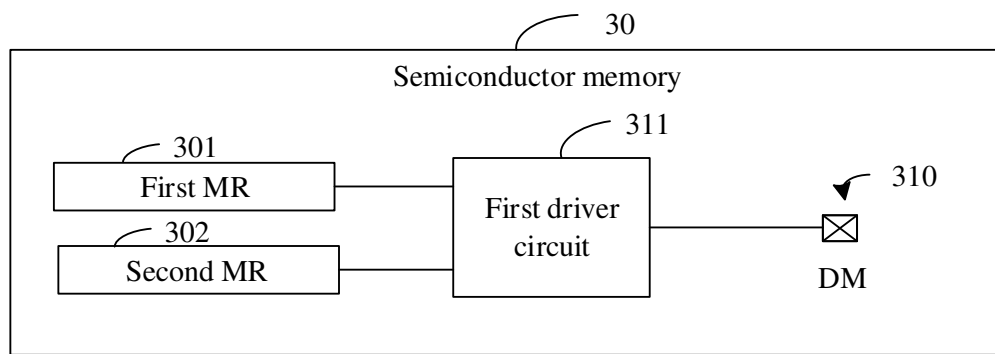


FIG. 3

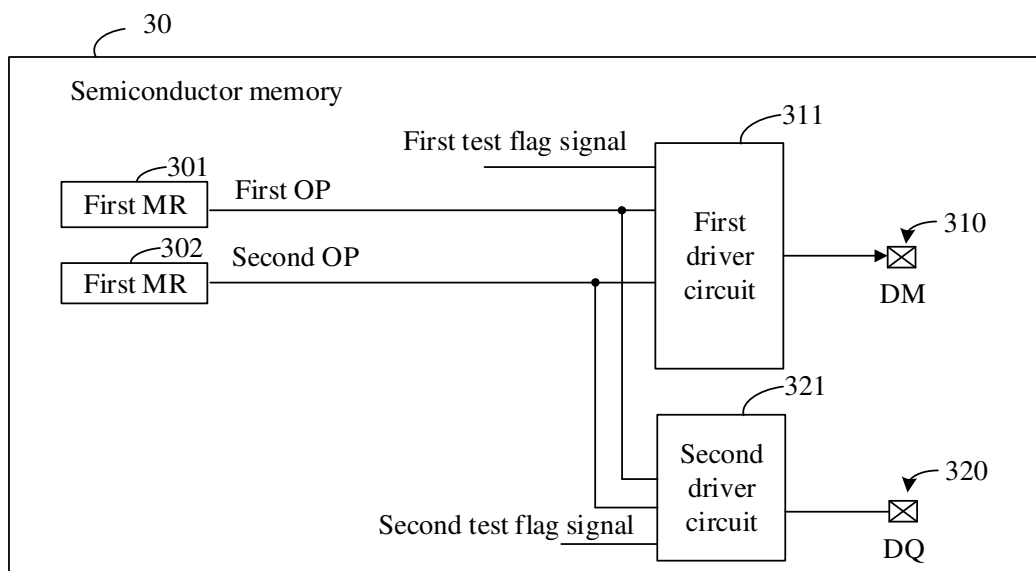


FIG. 4A

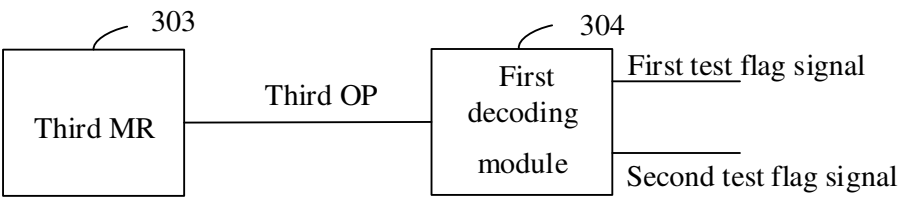


FIG. 4B

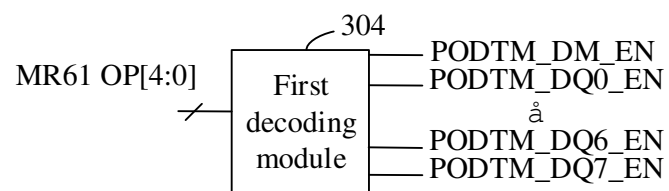


FIG. 5

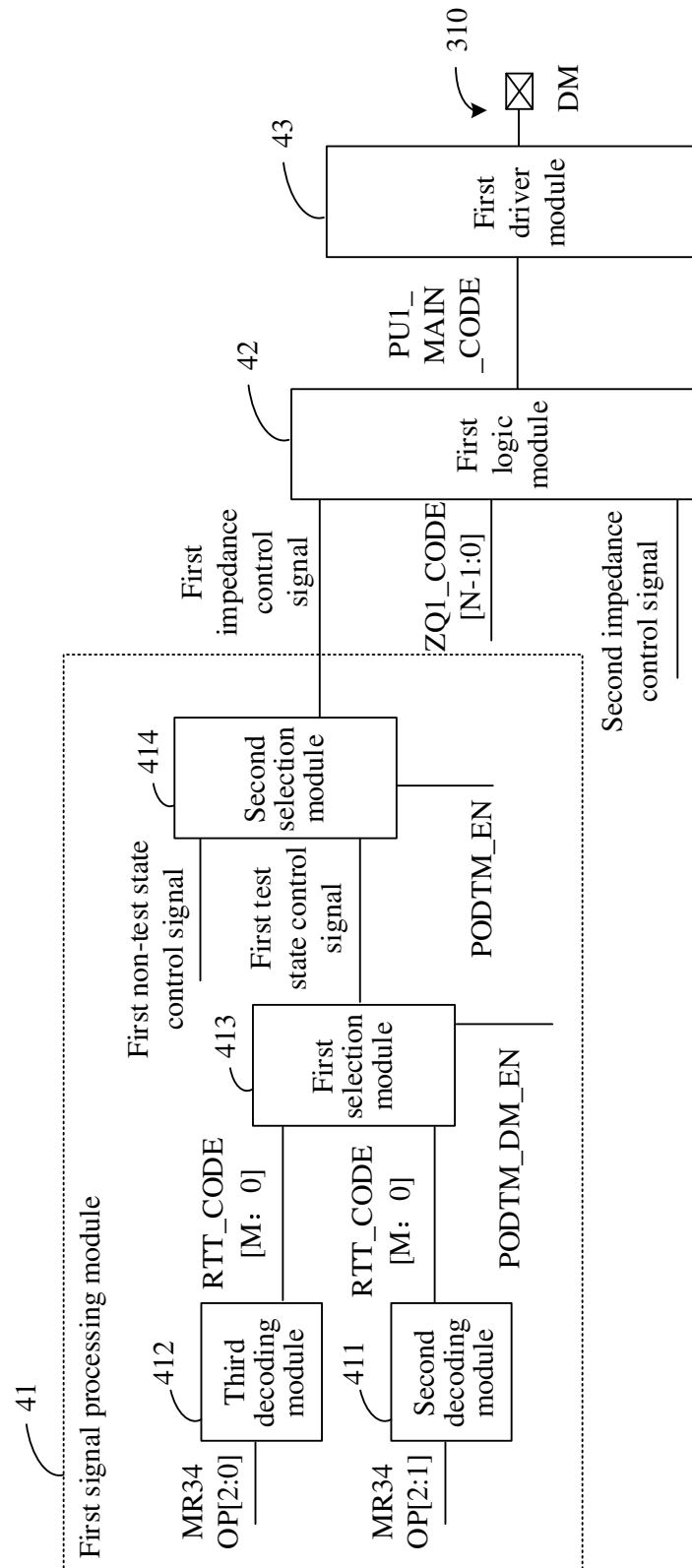


FIG. 6

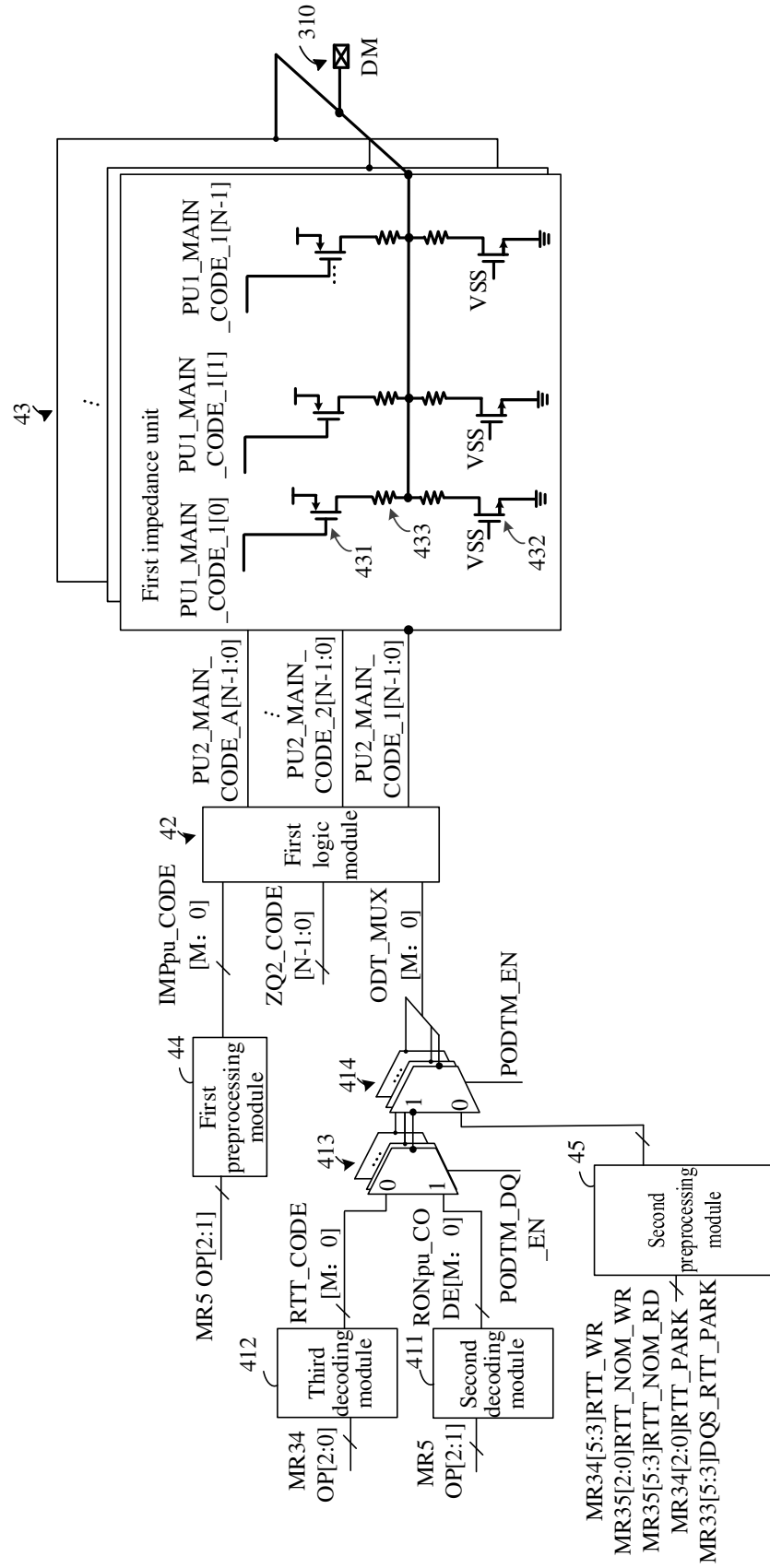


FIG. 7

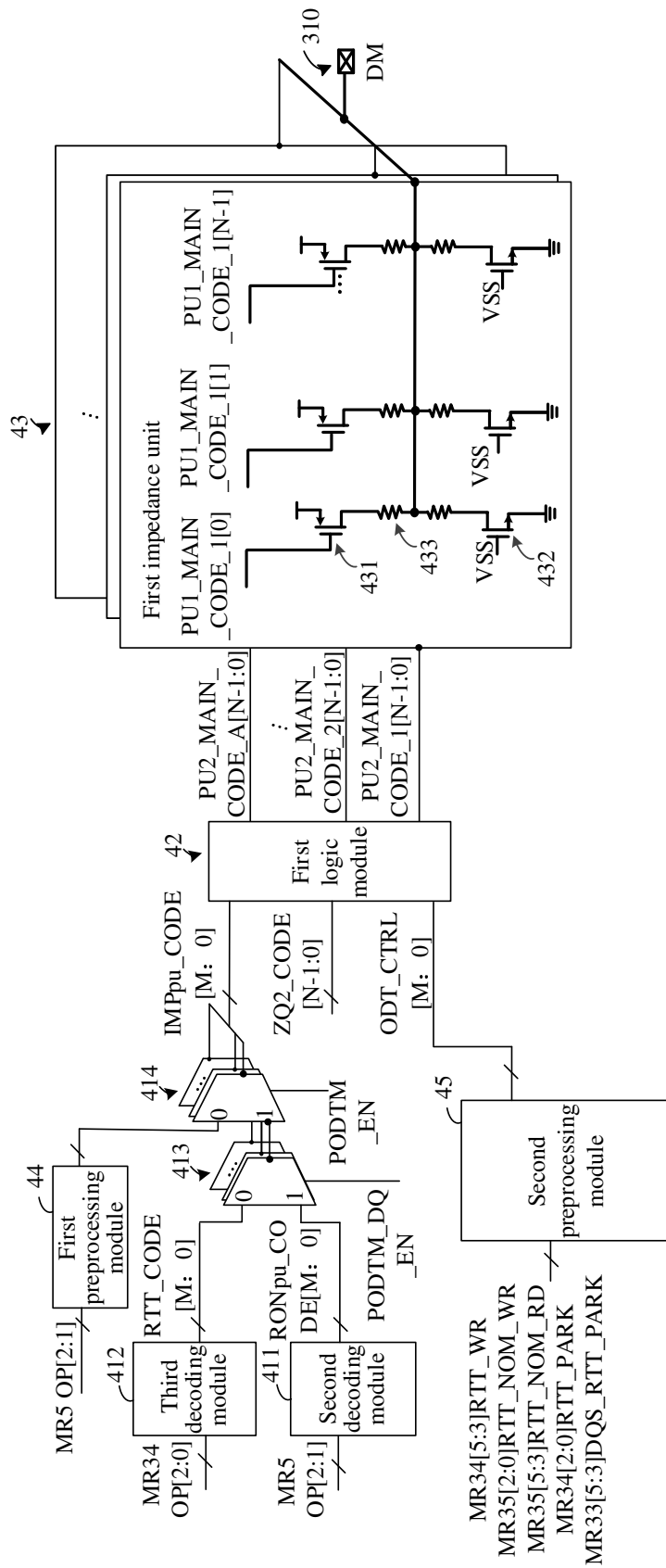


FIG. 8

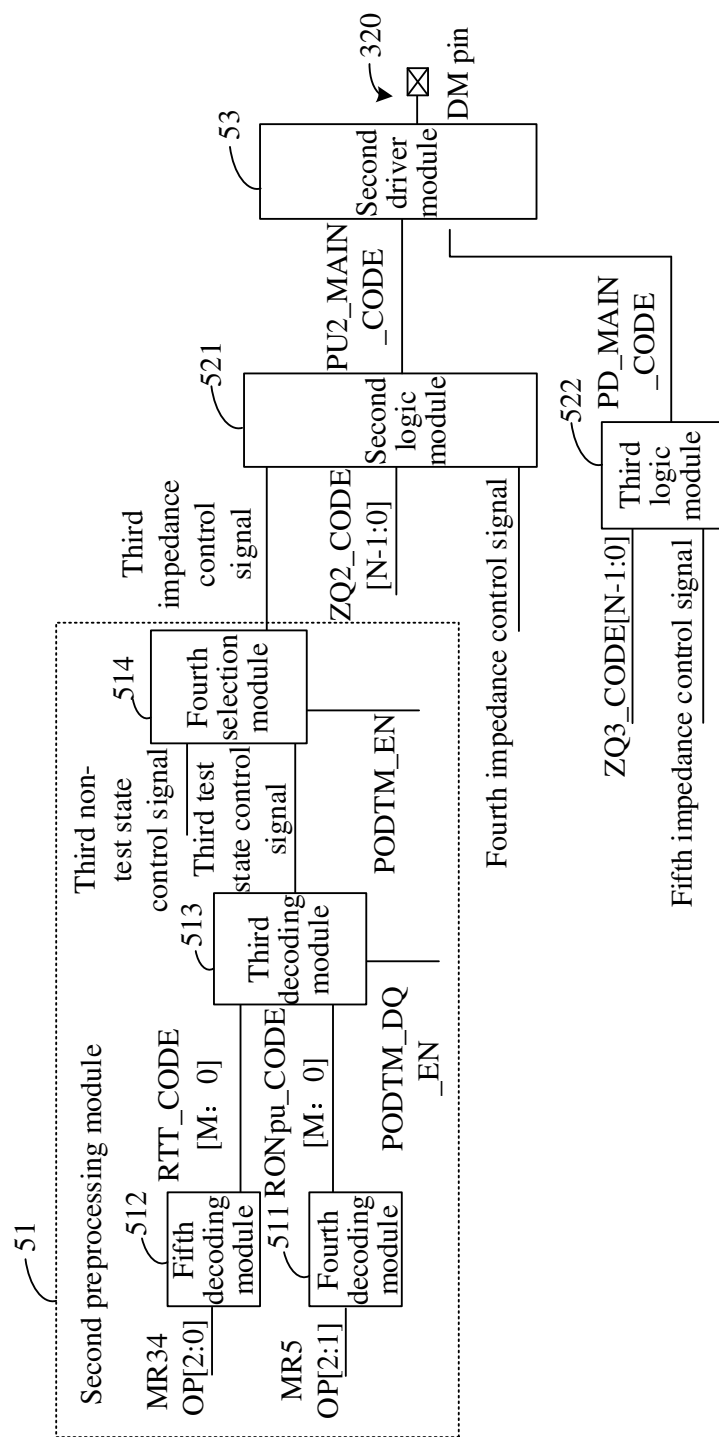


FIG. 9

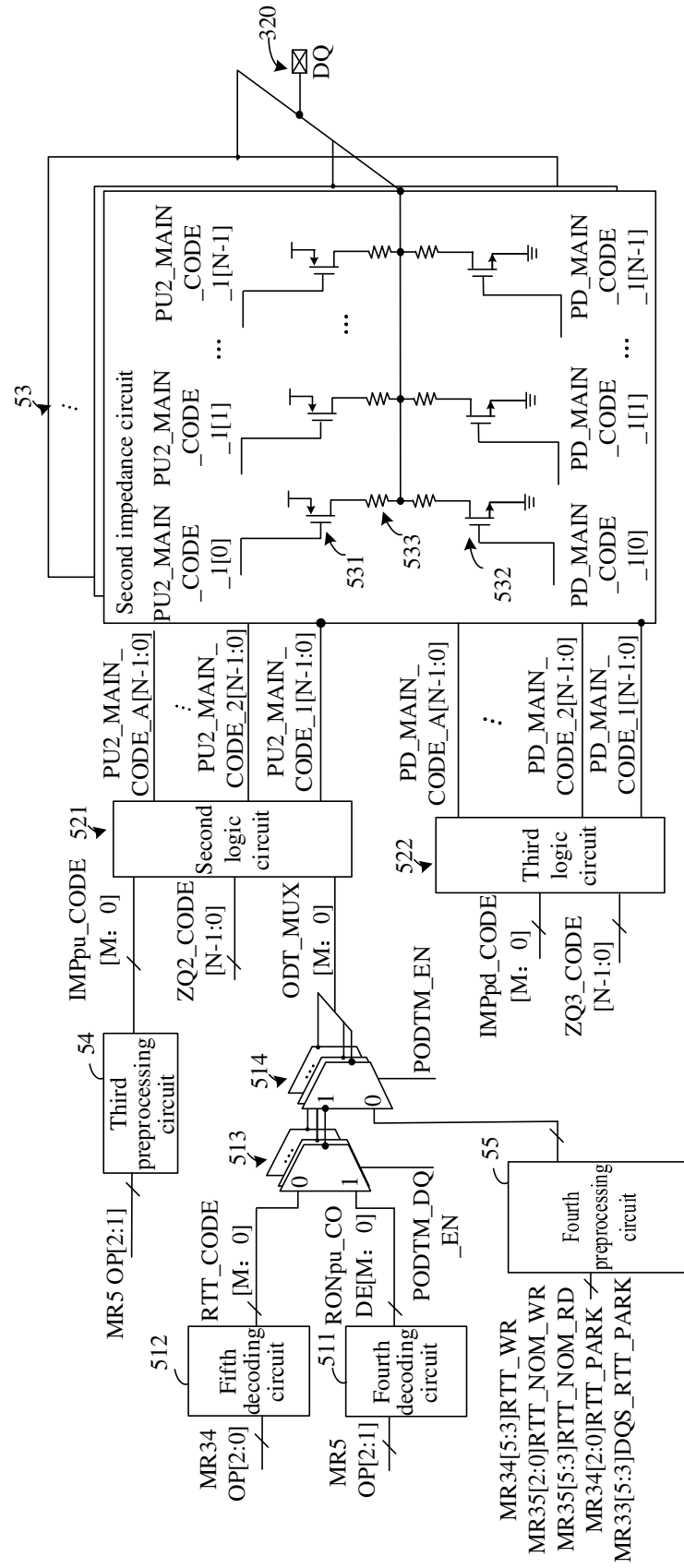


FIG. 10

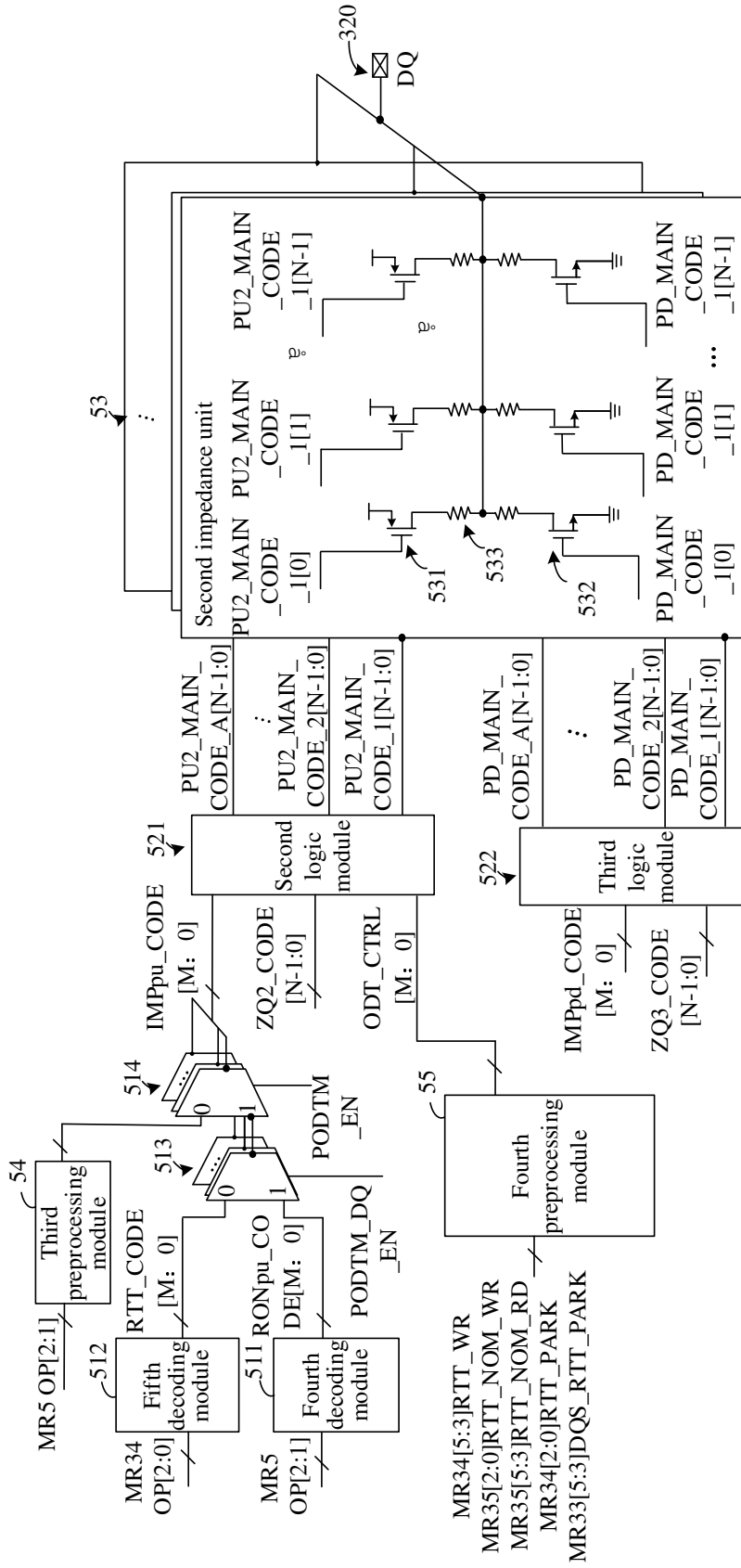


FIG. 11

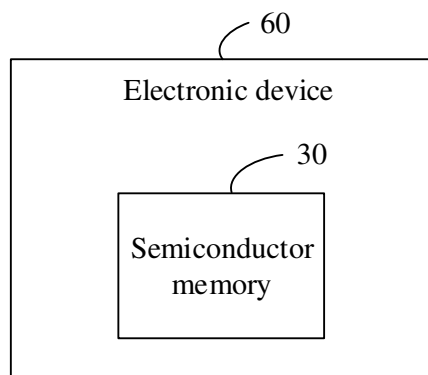


FIG. 12