CLAIMS

What is claimed is:

1. A method for video decoding, comprising:

receiving, by a decoder, a Sequence Parameter Set (SPS) reversed coordinates of the last significant coefficient enabled flag, that indicates whether a slice header (SH) reversed coordinates of the last significant coefficient enabled flag is present in slice header syntax structure referring to the SPS.

2. The method for video decoding of claim 1, further comprising:

in response to determining that a value of the SPS reversed coordinates of the last significant coefficient enabled flag equals to 1, determining, by the decoder, that the SH reversed coordinates of the last significant coefficient enabled flag is present in the slice header syntax structure referring to the SPS; and

in response to determining that the value of the SPS reversed coordinates of the last significant coefficient enabled flag equals to 0, determining, by the decoder, that the SH reversed coordinates of the last significant coefficient enabled flag is not present in the slice header syntax structure referring to the SPS.

3. The method for video decoding of claim 1, further comprising:

receiving, by the decoder, a general constraint information (GCI) reversed coordinates of the last significant coefficient enabled flag in GCI syntax to provide general control of the SPS reversed coordinates of the last significant coefficient enabled flag.

4. The method for video decoding of claim 3, further comprising:

in response to determining that a value of the GCI reversed coordinates of the last significant coefficient enabled flag equals to 1, determining that a value of the SPS reversed coordinates of the last significant coefficient enabled flag equals to 0.

5. A method for video decoding, comprising:

receiving, by a decoder, a Sequence Parameter Set (SPS) extended precision enabled flag that indicates whether an extended dynamic range is used for transform coefficients and transform processing.

6. The method for video decoding of claim 5, further comprising:

in response to determining that a value of the SPS extended precision enabled flag equals to 1, determining, by the decoder, that the extended dynamic range is used for transform coefficients and transform processing.

7. The method for video decoding of claim 5, further comprising:

receiving, by the decoder, a general constraint information (GCI) extended precision enabled flag in GCI syntax to provide general control of the SPS extended precision enabled flag.

8. The method for video decoding of claim 7, further comprising:

in response to determining that a value of the GCI extended precision enabled flag equals to 1, determining that a value of the SPS extended precision enabled flag equals to 0.

9. A method for video decoding, comprising:

receiving, by a decoder, a Sequence Parameter Set (SPS) high throughout flag that indicates whether syntax elements in residual coding are coded through bypass mode; and

in response to determining that a value of the SPS high throughout flag equals to 1, determining, by the decoder, that all syntax elements in the residual coding, except last significant coefficient position in regular residual coding (RRC), are coded through the bypass mode, and alignment is performed after the last significant coefficient position in RRC and at beginning of a transform block (TB) in transform skip residual coding (TSRC).

10. The method for video decoding of claim 9, further comprising:

receiving, by the decoder, a general constraint information (GCI) high throughout flag in GCI syntax to provide general control of the SPS high throughout flag.

11. The method for video decoding of claim 10, further comprising:

in response to determining that a value of the GCI high throughout flag equals to 1, determining that a value of the SPS high throughout flag equals to 0.

12. An apparatus for video decoding, comprising:

one or more processors; and

a memory configured to store instructions executable by the one or more processors; wherein the one or more processors, upon execution of the instructions, are configured to perform the method in any of claims 1-11.

13. A non-transitory computer-readable storage medium for video decoding storing computer-executable instructions that, when executed by one or more computer processors, cause the one or more computer processors to store a bitstream and to perform the method in any of claims 1-11 with the bitstream.

14. A computer program product comprising a plurality of programs for execution by a computing device having one or more processors, wherein the plurality of programs, when executed by the one or more processors, cause the computing device to perform the method of any of claims 1-11.

15. A computer readable storage medium storing a bitstream to be decoded by the method according to any of claims 1-11.